

## CMOS single-chip 8-bit microcontrollers

## 83C51FC/87C51FC

## DESCRIPTION

The 83C51FC/87C51FC (hereafter collectively called 8XC51FC) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC51FC has the same instruction set as the 80C51.

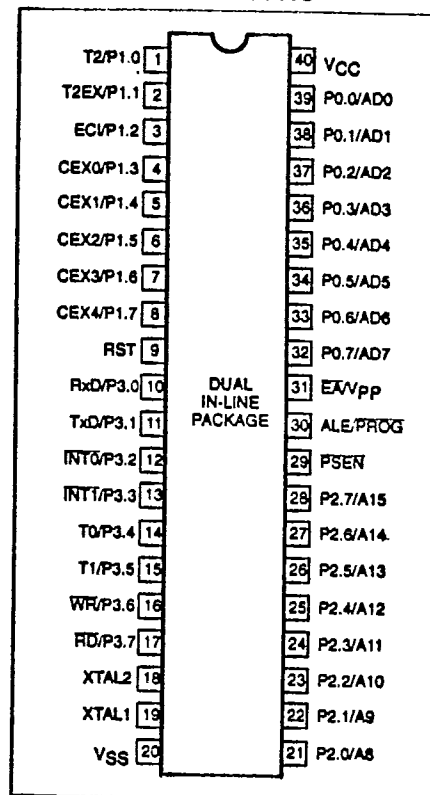
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 87C51FC contains 32k x 8 EPROM memory, the 83C51FC contains 32k x 8 ROM memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, three 16-bit timer/event counters, a Programmable Counter Array (PCA), a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC51FC can be expanded using standard TTL compatible memories and logic.

Its added features make it an even more powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multiprocessor communications.

## FEATURES

- 80C51 central processing unit
- 32k x 8 EPROM expandable externally to 64k bytes (87C51FC)
  - Quick Pulse programming algorithm
  - Two level program security system
- 32k x 8 ROM (83C51FC)
- 256 x 8 RAM, expandable externally to 64k bytes
- Three 16-bit timer/counters
  - T2 is an up/down counter
- Programmable Counter Array (PCA)
  - High speed output
  - Capture/compare
  - Pulse Width Modulator
  - Watchdog Timer
- Four 8-bit I/O ports
- Full-duplex enhanced UART
  - Framing error detection
  - Automatic address recognition
- Power control modes
  - Idle mode
  - Power-down mode
- Once (On Circuit Emulation) Mode
- Five package styles
- OTP package available

## PIN CONFIGURATIONS



## ORDERING INFORMATION

ROM	EPROM		TEMPERATURE RANGE °C AND PACKAGE <sup>1</sup>	FREQUENCY	DRAWING NUMBER
S83C51FC-4N40	S87C51FC-4N40	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	3.5 to 16MHz	0415C
	S87C51FC-4F40	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 16MHz	0590B
S83C51FC-4A44	S87C51FC-4A44	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	3.5 to 16MHz	0403G
	S87C51FC-4K44	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 16MHz	1472A
S83C51FC-4B44	S87C51FC-4B44	OTP	0 to +70, 44-Pin Plastic Quad Flat Pack	3.5 to 16MHz	1118D
S83C51FC-5N40	S87C51FC-5N40	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	3.5 to 16MHz	0415C
	S87C51FC-5F40	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 16MHz	0590B
S83C51FC-5A44	S87C51FC-5A44	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	3.5 to 16MHz	0403G
	S87C51FC-5K44	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 16MHz	1472A
S83C51FC-5B44	S87C51FC-5B44	OTP	0 to +70, 44-Pin Plastic Quad Flat Pack	3.5 to 16MHz	1118D
S83C51FC-AN40	S87C51FC-AN40	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	3.5 to 24MHz	0415C
	S87C51FC-AF40	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 24MHz	0590B
S83C51FC-AA44	S87C51FC-AA44	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	3.5 to 24MHz	0403G
	S87C51FC-AK44	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 24MHz	1472A
S83C51FC-BN40	S87C51FC-BN40	OTP	0 to +70, 40-Pin Plastic Dual In-line Package	3.5 to 24MHz	0415C
	S87C51FC-BF40	UV	0 to +70, 40-Pin Ceramic Dual In-line Package w/Window	3.5 to 24MHz	0590B
S83C51FC-BA44	S87C51FC-BA44	OTP	0 to +70, 44-Pin Plastic Leaded Chip Carrier	3.5 to 24MHz	0403G
	S87C51FC-BK44	UV	0 to +70, 44-Pin Ceramic Leaded Chip Carrier w/Window	3.5 to 24MHz	1472A

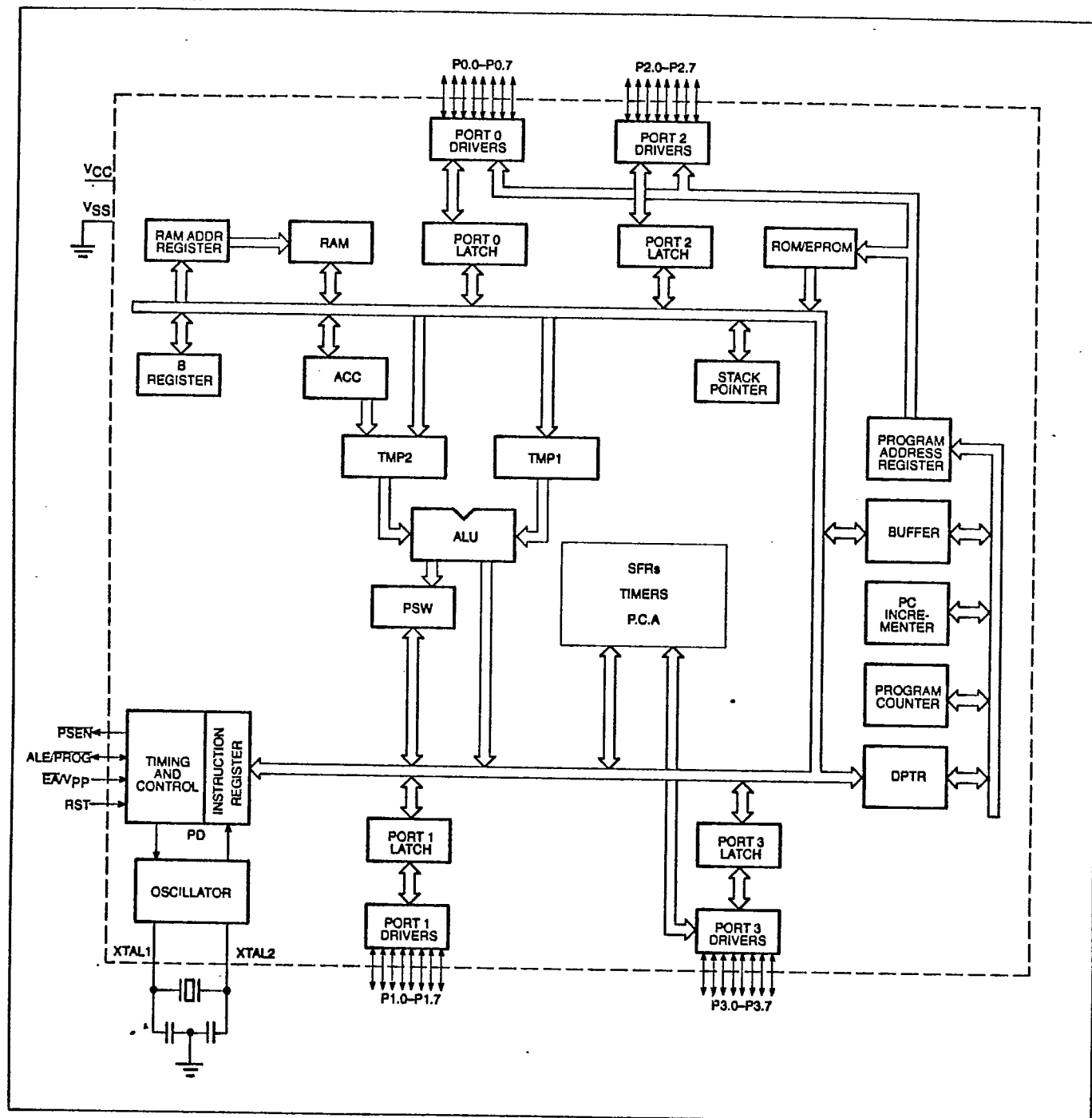
## NOTE:

1. OTP = One Time Programmable EPROM. UV = Erasable EPROM.

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### BLOCK DIAGRAM



## CMOS single-chip 8-bit microcontrollers

## 83C51FC/87C51FC

Table 1. 8XC51FC Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE								
			LSB																
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H								
AUXR#	Auxiliary	8EH	-	-	-	-	-	-	-	AO	xxxxxxx0B								
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H								
CCAP0H#	Module 0 Capture High	FAH									xxxxxxxxxB								
CCAP1H#	Module 1 Capture High	FBH									xxxxxxxxxB								
CCAP2H#	Module 2 Capture High	FCH									xxxxxxxxxB								
CCAP3H#	Module 3 Capture High	FDH									xxxxxxxxxB								
CCAP4H#	Module 4 Capture High	FEH									xxxxxxxxxB								
CCAP0L#	Module 0 Capture Low	EAH									xxxxxxxxxB								
CCAP1L#	Module 1 Capture Low	EBH									xxxxxxxxxB								
CCAP2L#	Module 2 Capture Low	ECH									xxxxxxxxxB								
CCAP3L#	Module 3 Capture Low	EDH									xxxxxxxxxB								
CCAP4L#	Module 4 Capture Low	EEH									xxxxxxxxxB								
CCAPM0#	Module 0 Mode	DAH									-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM1#	Module 1 Mode	DBH									-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B
CCAPM2#	Module 2 Mode	DCH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B								
CCAPM3#	Module 3 Mode	DDH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B								
CCAPM4#	Module 4 Mode	DEH	-	ECOM	CAPP	CAPN	MAT	TOG	PWM	ECCF	x0000000B								
CCON*#	PCA Counter Control	DAH	DF	DE	DD	DC	DB	DA	D9	D8	00x00000B								
	PCA Counter High	DBH	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0									
	PCA Counter Low	DCH										00H							
CMOD#	PCA Counter Mode	DDH	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00xxx000B								
DPTR:	Data Pointer (2 bytes)	DEH									00H								
	Data Pointer High	DEH										00H							
DPL	Data Pointer Low	DFH									00H								
IE*	Interrupt Enable	EAH	AF	AE	AD	AC	AB	AA	A9	A8	00H								
		EAH	EA	EC	ET2	ES	ET1	EX1	ET0	EX0									
IP*	Interrupt Priority	EBH	BF	BE	BD	BC	BB	BA	B9	B8	x0000000B								
		EBH	-	PPC	PT2	PS	PT1	PX1	PT0	PX0									
IPH*#	Interrupt Priority High	ECH	B7	B6	B5	B4	B3	B2	B1	B0	x0000000B								
		ECH	-	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H									
P0*	Port 0	EDH	87	86	85	84	83	82	81	80	FFH								
		EDH	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0									
P1*	Port 1	EEH	97	96	95	94	93	92	91	90	FFH								
		EEH	CEX4	CEX3	CEX2	CEX1	CEX0	EX1	T2EX	T2									
P2*	Port 2	EFH	A7	A6	A5	A4	A3	A2	A1	A0	FFH								
		EFH	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8									
P3*	Port 3	F0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH								
		F0H	RD	WR	T1	T0	INT1	INT0	TxD	RxD									
PCON	Power Control	F7H	SMOD1	SMOD0	-	POF1	GF1	GF0	PD	IDL	00xxxx00B								

\* SFRs are bit addressable.

# SFRs are modified from or added to the 80C51 SFRs.

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Table 1. 8XC51FC Special Function Registers (Continued)

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION								RESET VALUE							
			MSB							LSB								
PSW*	Program Status Word	D0H	D7	D6	D5	D4	D3	D2	D1	D0	00H							
			CY	AC	F0	RS1	RS0	OV	-	P								
RACAP2H#	Timer 2 Capture High	CBH									00H							
RACAP2L#	Timer 2 Capture Low	CAH									00H							
											00H							
SADDR#	Slave Address	A9H									00H							
SADEN#	Slave Address Mask	B9H									00H							
SBUF	Serial Data Buffer	99H									xxxxxxx0B							
SCON*	Serial Control	98H									9F	9E	9D	9C	9B	9A	99	98
SP	Stack Pointer	81H									SM0	SM1	SM2	REN	TB8	RB8	TI	RI
TCON*	Timer Control	88H									00H							
											8F	8E	8D	8C	8B	8A	89	88
											TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
T2CON*	Timer 2 Control	C8H									00H							
											CF	CE	CD	CC	CB	CA	C9	C8
											TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
T2MOD#	Timer 2 Mode Control	C9H	-	-	-	-	-	-	-	DCEN	xxxxxxx0B							
TH0	Timer High 0	8CH									00H							
TH1	Timer High 1	8DH									00H							
TH2#	Timer High 2	CDH									00H							
TL0	Timer Low 0	8AH									00H							
TL1	Timer Low 1	8BH									00H							
TL2#	Timer Low 2	CCH									00H							
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H							
			C7	C6	C5	C4	C3	C2	C1	C0								

\* SFRs are bit addressable

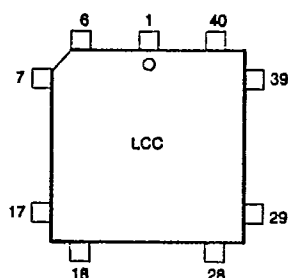
\* SFRs are bit addressable.

# SFRs are modified from or added to the 80C51 SFRs.

1. Reset value depends on reset source.

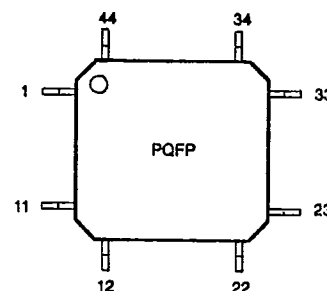
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CERAMIC AND PLASTIC LEADED CHIP CARRIER  
PIN FUNCTIONS

Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0/T2	24	P2.0/A8
3	P1.1/T2EX	25	P2.1/A9
4	P1.2/ECI	26	P2.2/A10
5	P1.3/CEX0	27	P2.3/A11
6	P1.4/CEX1	28	P2.4/A12
7	P1.5/CEX2	29	P2.5/A13
8	P1.6/CEX3	30	P2.6/A14
9	P1.7/CEX4	31	P2.7/A15
10	RST	32	PSEN
11	P3.0/RxD	33	ALE/PROG
12	NC	34	NC
13	P3.1/TxD	35	EA/Vpp
14	P3.2/INT0	36	P0.7/AD7
15	P3.3/INT1	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/WR	40	P0.3/AD3
19	P3.7/RD	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	VSS	44	VCC

## PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5/CEX2	23	P2.5/A13
2	P1.6/CEX3	24	P2.6/A14
3	P1.7/CEX4	25	P2.7/A15
4	RST	26	PSEN
5	P3.0/RxD	27	ALE/PROG
6	NC	28	NC
7	P3.1/TxD	29	EA/Vpp
8	P3.2/INT0	30	P0.7/AD7
9	P3.3/INT1	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/WR	34	P0.3/AD3
13	P3.7/RD	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	VSS	38	VCC
17	NC	39	NC
18	P2.0/A8	40	P1.0/T2
19	P2.1/A9	41	P1.1/T2EX
20	P2.2/A10	42	P1.2/ECI
21	P2.3/A11	43	P1.3/CEX0
22	P2.4/A12	44	P1.4/CEX1

## PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
Vss	20	22	16	I	Ground: 0V reference.
Vcc	40	44	38	I	<b>Power Supply:</b> This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	<b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and receives code bytes during EPROM programming. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include: <b>T2 (P1.0):</b> Timer/Counter 2 external count input/Clockout <b>T2EX (P1.1):</b> Timer/Counter 2 Reload/Capture/Direction Control <b>ECI (P1.2):</b> External Clock Input to the PCA <b>CEX0 (P1.3):</b> Capture/Compare External I/O for PCA module 0 <b>CEX1 (P1.4):</b> Capture/Compare External I/O for PCA module 1 <b>CEX2 (P1.5):</b> Capture/Compare External I/O for PCA module 2 <b>CEX3 (P1.6):</b> Capture/Compare External I/O for PCA module 3 <b>CEX4 (P1.7):</b> Capture/Compare External I/O for PCA module 4
	1	2	40	I	
	2	3	41	I	
	3	4	42	I	
	4	5	43	I/O	
	5	6	44	I/O	
	6	7	1	I/O	
	7	8	2	I/O	
	8	9	3	I/O	

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## PIN DESCRIPTIONS (Continued)

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
P2.0–P2.7	21–28	24–31	18–25	I/O	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: $I_{IL}$ ). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address bits during EPROM programming and verification.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: $I_{IL}$ ). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	I	<b>RxD (P3.0):</b> Serial input port
	11	13	7	O	<b>TxD (P3.1):</b> Serial output port
	12	14	8	I	<b>INT0 (P3.2):</b> External interrupt
	13	15	9	I	<b>INT1 (P3.3):</b> External interrupt
	14	16	10	I	<b>T0 (P3.4):</b> Timer 0 external input
	15	17	11	I	<b>T1 (P3.5):</b> Timer 1 external input
	16	18	12	O	<b>WR (P3.6):</b> External data memory write strobe
	17	19	13	O	<b>RD (P3.7):</b> External data memory read strobe
RST	9	10	4	I	<b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC}$ .
ALE/PROG	30	33	27	I/O	<b>Address Latch Enable/Program Pulse:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.
PSEN	29	32	26	O	<b>Program Store Enable:</b> The read strobe to external program memory. When the 8XC51FC is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
EA/V <sub>PP</sub>	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> EA must be externally held low to enable the device to fetch code from external program memory locations 0000H and 7FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 7FFFH. This pin also receives the 12.75V programming supply voltage ( $V_{PP}$ ) during EPROM programming. If security bit 1 is programmed, EA will be internally latched on Reset.
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier.

## NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than  $V_{CC} + 0.5V$  or  $V_{SS} - 0.5V$ , respectively.

## TIMER 2

This is a 16-bit up or down counter, which can be operated as either a timer or event counter. It can be operated in one of three different modes (autoreload, capture or as the baud rate generator for the UART).

In the autoreload mode the Timer can be set to count up or down by setting or clearing the bit DCEN in the T2CON Special Function Register. The SFR's RCAP2H and RCAP2L are used to reload the Timer upon overflow or a 1-to-0 transition on the T2EX input (P1.1).

In the Capture mode Timer 2 can either set TF2 and generate an interrupt or capture its value. To capture Timer 2 in response to a 1-to-0 transition on the T2EX input, the EXEN2 bit in the T2CON must be set. Timer 2 is then captured in SFR's RCAP2H and RCAP2L.

As the baud rate generator, Timer 2 is selected by setting TCLK and/or RCLK in T2CON. As the baud rate generator Timer 2 is incremented at  $1/2$  the oscillator frequency.

## POWER OFF FLAG

The Power Off Flag (POF) is set by on-chip circuitry when the  $V_{CC}$  level on the 8XC51FC rises from 0 to 5V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after powerdown. The  $V_{CC}$  level must remain above 3V for the POF to remain unaffected by the  $V_{CC}$  level.

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### OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

#### Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V<sub>CC</sub> and RST must come up at the same time for a proper start-up.

#### Idle Mode

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

#### Power-Down Mode

To save even more power, a Power Down mode can be invoked by software. In this

mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the 8XC51FC either a hardware reset or external interrupt can use an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V<sub>CC</sub> is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

#### Design Consideration

- When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

#### ONCE™ Mode

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems

using the 8XC51FC without the 8XC51FC having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and PSEN is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and PSEN are weakly pulled high. The oscillator circuit remains active. While the 8XC51FC is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

#### Programmable Clock-Out

The 8XC51FC has a new feature. A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed (1) to input the external clock for Timer/Counter 2 or (2) to output a 50% duty cycle clock ranging from 61Hz to 4MHz at a 16MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/T2 (in T2CON) must be cleared and bit T2OE in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

$$\frac{\text{OscillatorFrequency}}{4 \times (65536 - \text{RCAP2H}, \text{RCAP2L})}$$

In the Clock-Out mode Timer 2 roll-overs will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

Table 2. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

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### Programmable Counter Array (PCA)

The Programmable Counter Array is a special Timer that has five 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture, software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to P1.3(CEX0), module 1 to P1.4(CEX1), etc. The basic PCA configuration is shown in Figure 1.

The PCA timer is a common time base for all five modules and can be programmed to run at: 1/12 the oscillator frequency, 1/4 the oscillator frequency, the Timer 0 overflow, or the input on the ECI pin (P1.2). The timer count source is determined from the CPS1 and CPS0 bits in the CMOD SFR as follows (see Figure 4):

CPS1	CPS0	PCA Timer Count Source
0	0	1/12 oscillator frequency
0	1	1/4 oscillator frequency
1	0	Timer 0 overflow
1	1	External Input at ECI pin

In the CMOD SFR are three additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, WDTE which enables or disables the watchdog function on module 4, and ECF

which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows. These functions are shown in Figure 2.

The watchdog timer function is implemented in module 4 (see Figure 12).

The CCON SFR contains the run control bit for the PCA and the flags for the PCA timer (CF) and each module (refer to Figure 5). To run the PCA the CR bit (CCON.6) must be set by software. The PCA is shut off by clearing this bit. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF bit in the CMOD register is set. The CF bit can only be cleared by software. Bits 0 through 4 of the CCON register are the flags for the modules (bit 0 for module 0, bit 1 for module 1, etc.) and are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software. The PCA interrupt system shown in Figure 3.

Each module in the PCA has a special function register associated with it. These registers are: CCAPM0 for module 0, CCAPM1 for module 1, etc. (see Figure 6). The registers contain the bits that control the mode that each module will operate in. The ECCF bit (CCAPMn.0 where n=0, 1, 2, 3, or 4 depending on the module) enables the CCF flag in the CCON SFR to generate an

interrupt when a match or compare occurs in the associated module. PWM (CCAPMn.1) enables the pulse width modulation mode. The TOG bit (CCAPMn.2) when set causes the CEX output associated with the module to toggle when there is a match between the PCA counter and the module's capture/compare register. The match bit MAT (CCAPMn.3) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module's capture/compare register.

The next two bits CAPN (CCAPMn.4) and CAPP (CCAPMn.5) determine the edge that a capture input will be active on. The CAPN bit enables the negative edge, and the CAPP bit enables the positive edge. If both bits are set both edges will be enabled and a capture will occur for either transition. The last bit in the register ECOM (CCAPMn.6) when set enables the comparator function. Figure 7 shows the CCAPMn settings for the various PCA functions.

There are two additional registers associated with each of the PCA modules. They are CCAPnH and CCAPnL and these are the registers that store the 16-bit count when a capture occurs or a compare should occur. When a module is used in the PWM mode these registers are used to control the duty cycle of the output.

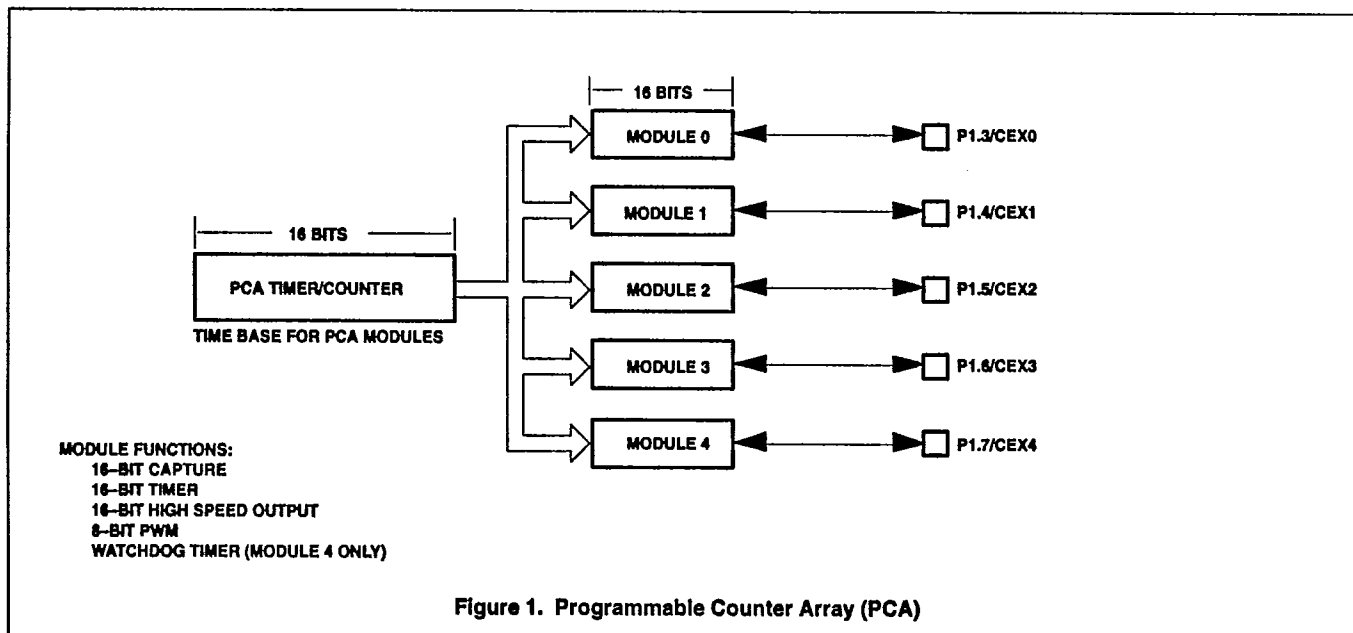
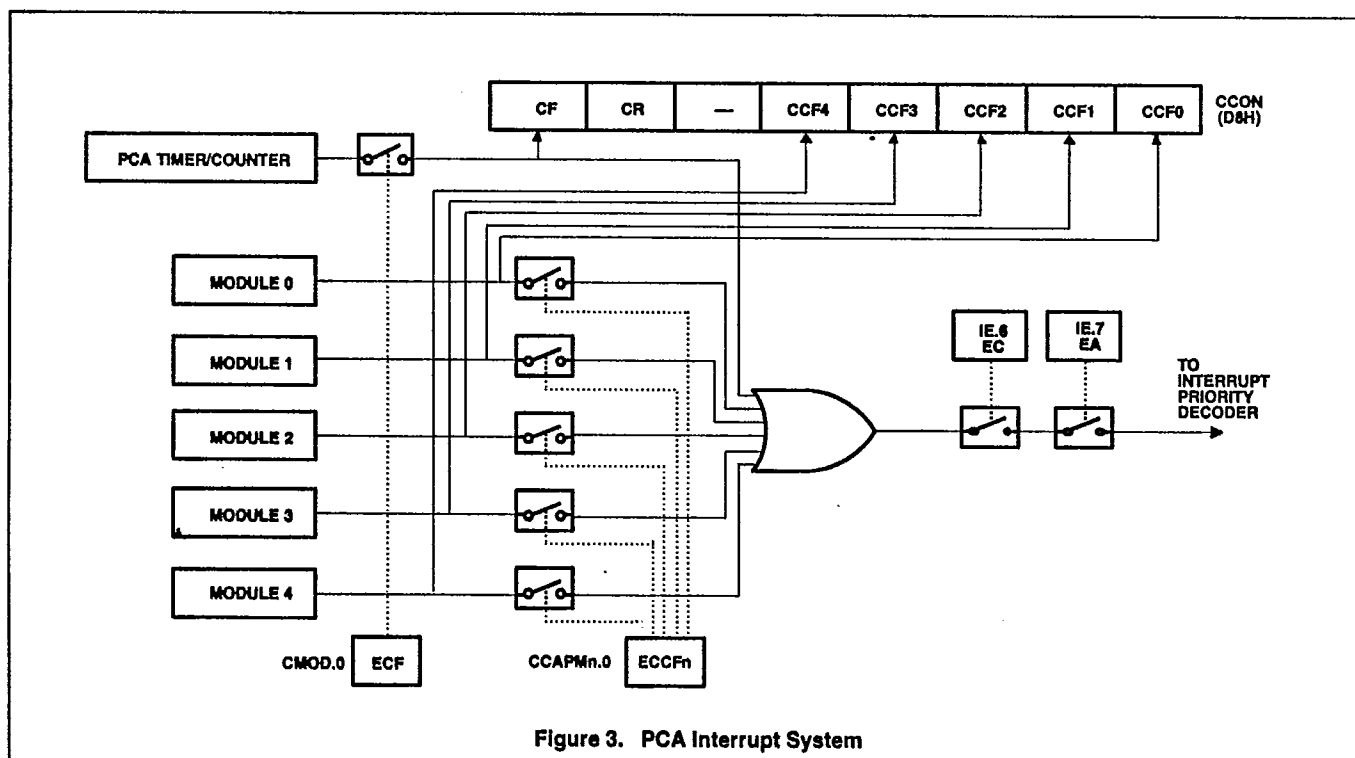
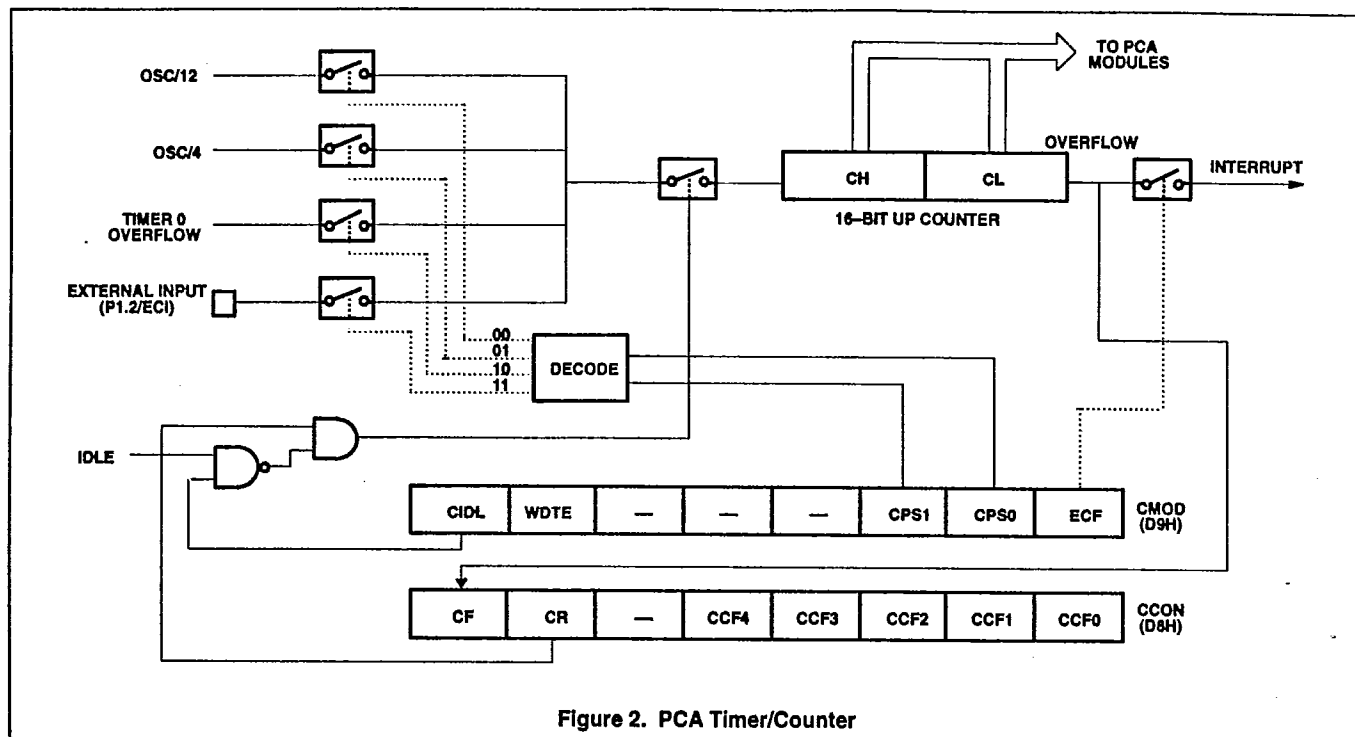


Figure 1. Programmable Counter Array (PCA)



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**CMOD** Address = 0D9H

Reset Value = 00XX X000B

Bit Addressable

	CIDL	WDTE	—	—	—	CPS1	CPS0	ECF
Bit:	7	6	5	4	3	2	1	0

**Symbol**      **Function**

- CIDL**      Counter Idle control: CIDL = 0 programs the PCA Counter to continue functioning during idle Mode. CIDL = 1 programs it to be gated off during idle.
- WDTE**      Watchdog Timer Enable: WDTE = 0 disables Watchdog Timer function on PCA Module 4. WDTE = 1 enables it.
- Not implemented, reserved for future use.\*
- CPS1**      PCA Count Pulse Select bit 1.
- CPS0**      PCA Count Pulse Select bit 0.
- | CPS1 | CPS0 | Selected PCA Input**   |
|------|------|--|
| 0    | 0    | 0      Internal clock, $F_{osc} + 12$                              |
| 0    | 1    | 1      Internal clock, $F_{osc} + 4$                               |
| 1    | 0    | 2      Timer 0 overflow  |
| 1    | 1    | 3      External clock at ECI/P1.2 pin (max. rate = $F_{osc} + 8$ ) |
- ECF**      PCA Enable Counter Overflow interrupt: ECF = 1 enables CF bit in CCON to generate an interrupt. ECF = 0 disables that function of CF.

**NOTE:**

\*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

\*\* $F_{osc}$  = oscillator frequency

**Figure 4. CMOD: PCA Counter Mode Register**

**CCON** Address = 0D8H

Reset Value = 00X0 0000B

Bit Addressable

	CF	CR	—	CCF4	CCF3	CCF2	CCF1	CCF0
Bit:	7	6	5	4	3	2	1	0

**Symbol**      **Function**

- CF**      PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.
- CR**      PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.
- Not implemented, reserved for future use\*.
- CCF4**      PCA Module 4 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
- CCF3**      PCA Module 3 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
- CCF2**      PCA Module 2 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
- CCF1**      PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.
- CCF0**      PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

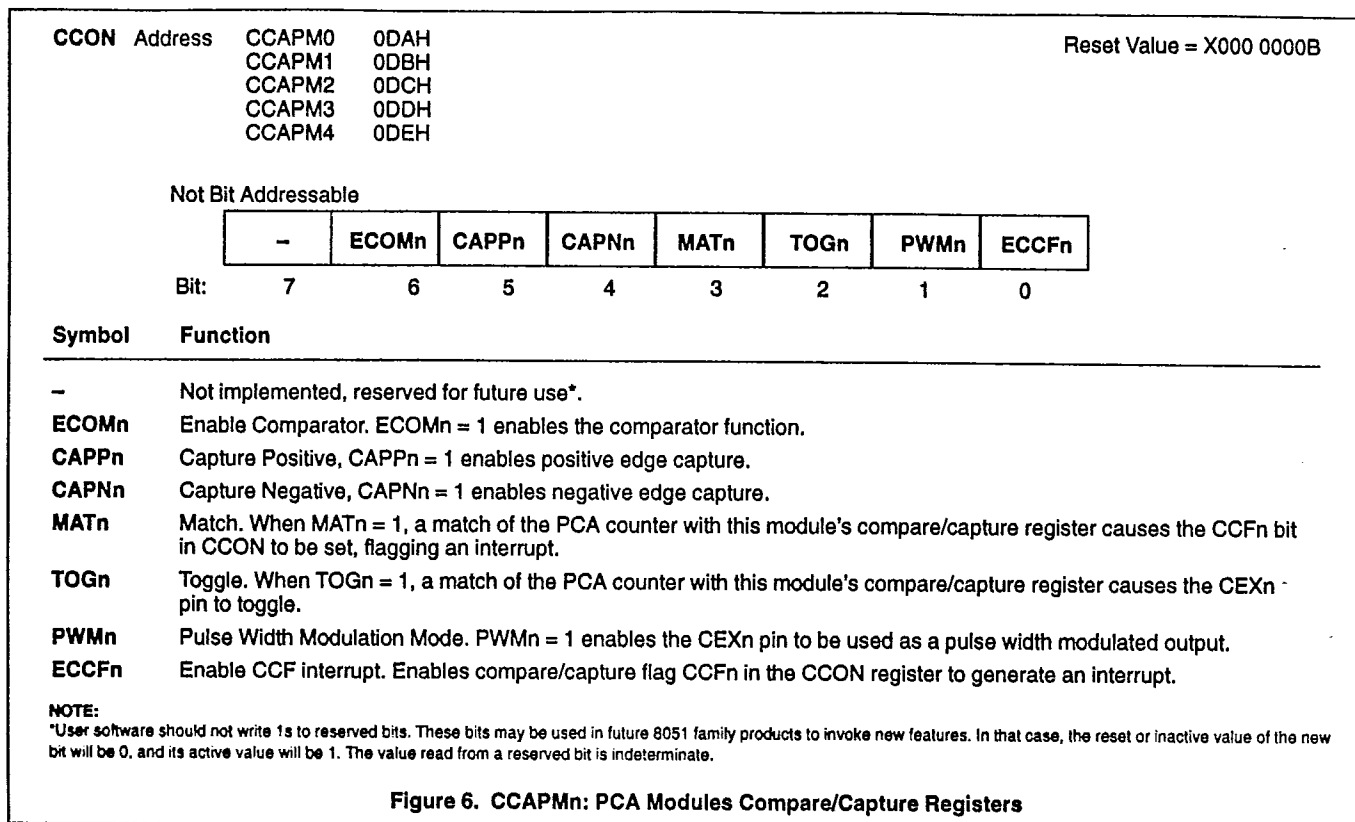
**NOTE:**

\*User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

**Figure 5. CCON: PCA Counter Control Register**

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## PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits CAPN and CAPP for that module must be set. The external CEX input for the module (on port 1) is sampled for a transition. When a valid transition occurs the PCA hardware loads the value of the PCA counter registers (CH and CL) into the module's capture registers (CCAPnL and CCAPnH). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated. Refer to Figure 8.

## 16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOM and MAT bits in the modules CCAPMn register. The PCA timer will be compared to the module's capture registers and when a match occurs an interrupt will occur if the CCFn (CCON SFR) and the ECCFn (CCAPMn SFR) bits for the module are both set (see Figure 9).

## High Speed Output Mode

In this mode the CEX output (on port 1) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module's capture registers. To activate this mode the TOG, MAT, and ECOM bits in the module's CCAPMn SFR must be set (see Figure 10).

## Pulse Width Modulator Mode

All of the PCA modules can be used as PWM outputs. Figure 11 shows the PWM function. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the PCA timer. The duty cycle of each module is independently variable using the module's capture register CCAPL<sub>n</sub>. When the value of the PCA CL SFR is less than the value in the module's CCAPL<sub>n</sub> SFR the output will be low, when it is equal to or greater than the output will be high. When CL overflows from FF to 00, CCAPL<sub>n</sub> is reloaded with the value in CCAPH<sub>n</sub>, the allows updating the PWM

without glitches. The PWM and ECOM bits in the module's CCAPMn register must be set to enable the PWM mode.

## Enhanced UART

The UART operates in all of the usual modes that are described in the first section of this book for the 80C51. In addition the UART can perform framing error detect by looking for missing stop bits, and automatic address recognition. The 8XC51FC UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0) (see Figure 13). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software. Refer to Figure 14.

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—	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	MODULE FUNCTION
X	0	0	0	0	0	0	0	No operation
X	X	1	0	0	0	0	X	16-bit capture by a positive-edge trigger on CEXn
X	X	0	1	0	0	0	X	16-bit capture by a negative trigger on CEXn
X	X	1	1	0	0	0	X	16-bit capture by a transition on CEXn
X	1	0	0	1	0	0	X	16-bit Software Timer
X	1	0	0	1	1	0	X	16-bit High Speed Output
X	1	0	0	0	0	1	0	8-bit PWM
X	1	0	0	1	X	0	X	Watchdog Timer

Figure 7. PCA Module Modes (CCAPMn Register)

**Automatic Address Recognition**

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 15.

The 8 bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "IGiven" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0    SADDR =    1100 0000  
           SADEN =    1111 1101  
           Given =    1100 00X0

Slave 1    SADDR =    1100 0000  
           SADEN =    1111 1110  
           Given =    1100 00X0

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0    SADDR =    1100 0000  
           SADEN =    1111 1001  
           Given =    1100 0XX0

Slave 1    SADDR =    1110 0000  
           SADEN =    1111 1010  
           Given =    1110 0XX0

Slave 2    SADDR =    1110 0000  
           SADEN =    1111 1100  
           Given =    1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

**Reduced EMI Mode**

The AO bit (AUXR.O) in the AUXR register when set disables the ALE output.

**8XC51FC Reduced EMI Mode****AUXR (0X8E)**

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	AO

AO: Turns off ALE output.

**Interrupt Priority Structure**

The 8XC51FC has a 7-source four-level interrupt structure. There are 3 SFRs associated with the interrupts on the 8XC51FC. They are the IE and IP which are identical in function to those on the 80C51. In addition, there is the IPH (Interrupt Priority High) register that makes the four-level interrupt structure possible. The IPH is bit addressable and is located at SFR address B7H. The structure of the IPH register and a description of its bits is shown below:

**IPH (Interrupt Priority High) (B7H)**

7	6	5	4	3	2	1	0
—	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

IPH.0    PX0H    External interrupt 0 priority high  
 IPH.1    PT0H    Timer 0 interrupt priority high  
 IPH.2    PX1H    External interrupt 1 priority high  
 IPH.3    PT1H    Timer 1 interrupt priority high  
 IPH.4    PSH    Serial Port interrupt high  
 IPH.5    PT2H    Timer 2 interrupt priority high  
 IPH.6    PPCH    PCA interrupt priority high  
 IPH.7    —    Not implemented

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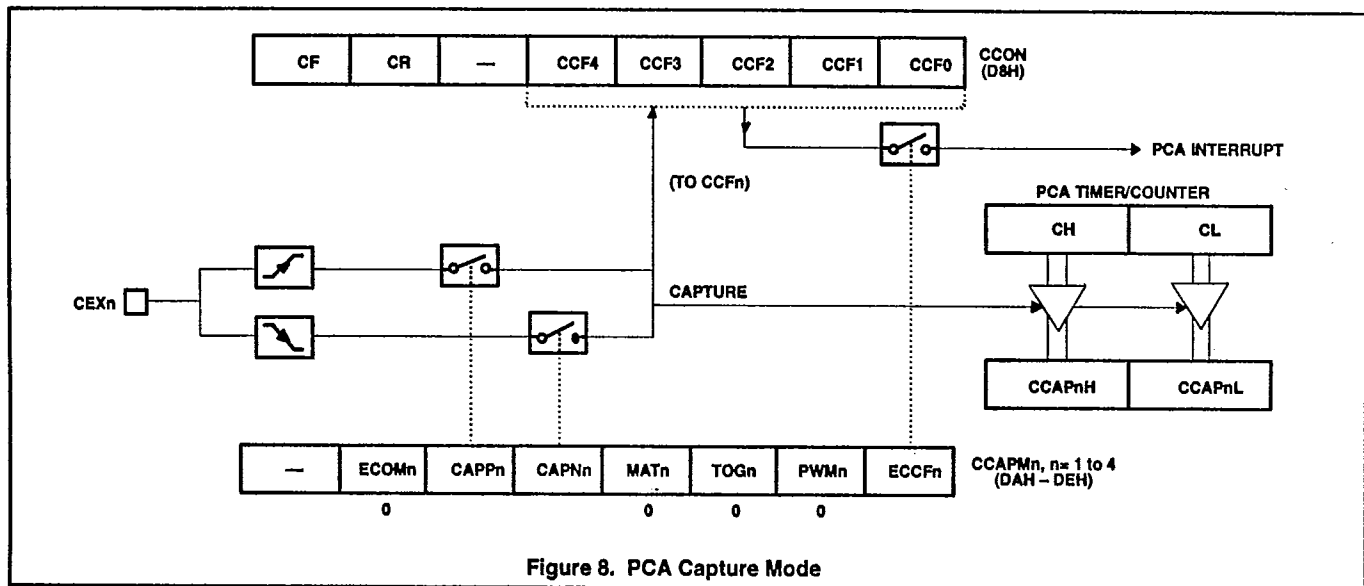
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The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

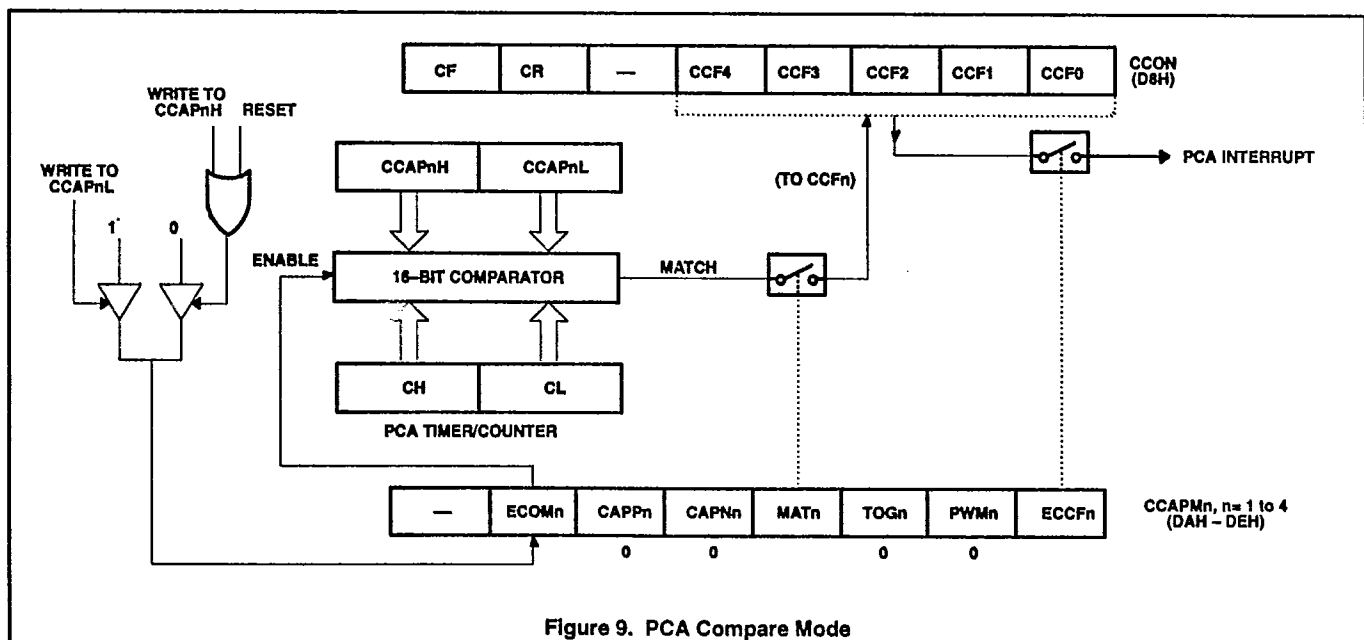
PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPH.x	IP.x	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The priority scheme for servicing the interrupts is the same as that for the 80C51, except there are four interrupt levels on the 8XC51FC rather than two as on the 80C51. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being

serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.



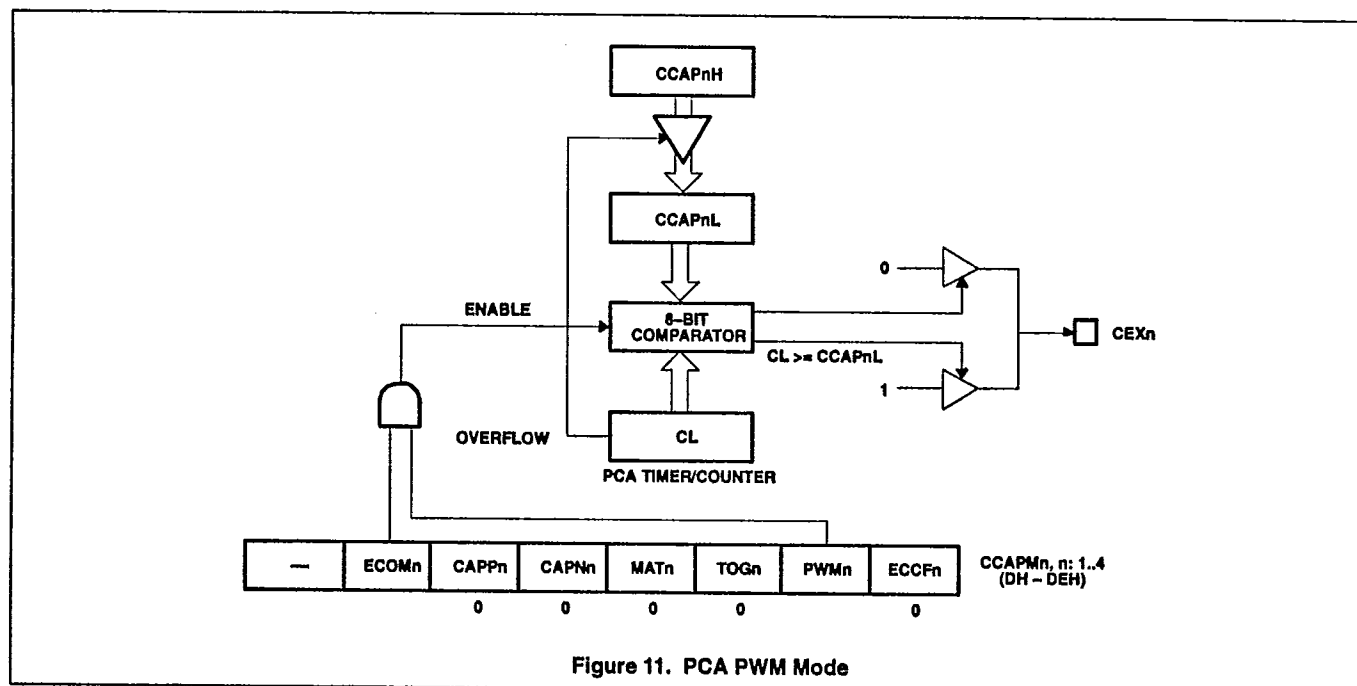
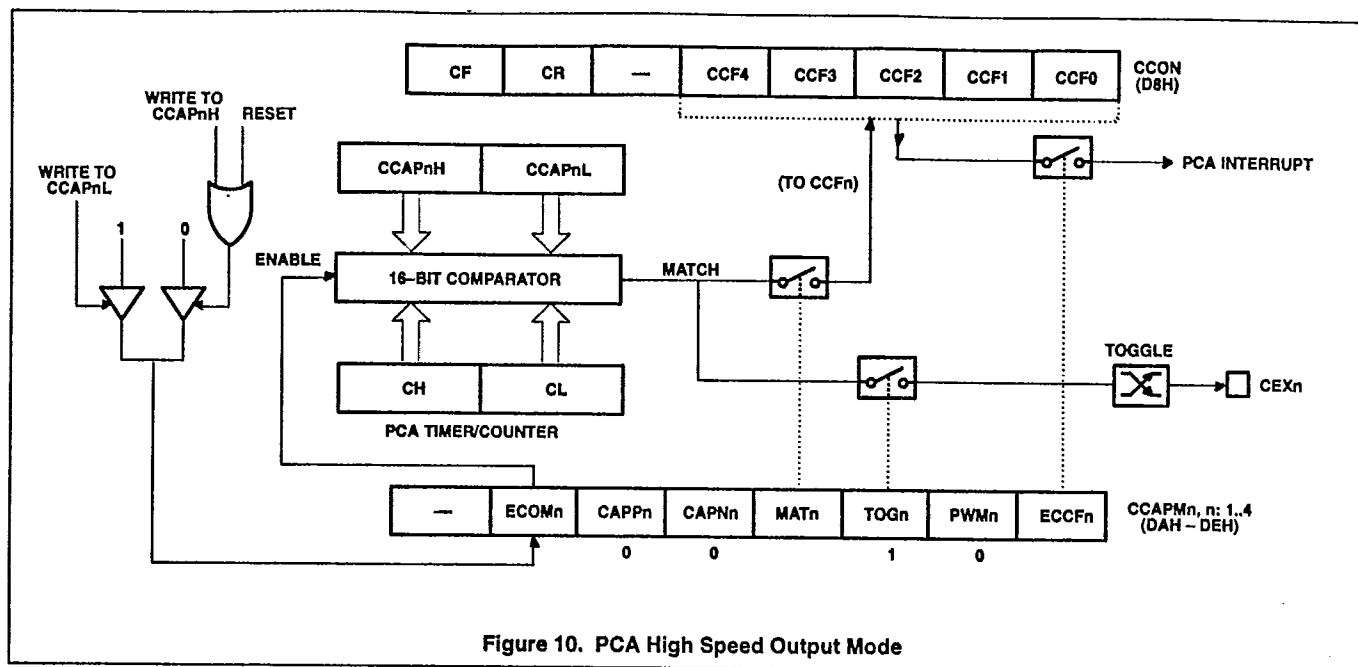
### Figure 8. PCA Capture Mode



### Figure 9. PCA Compare Mode

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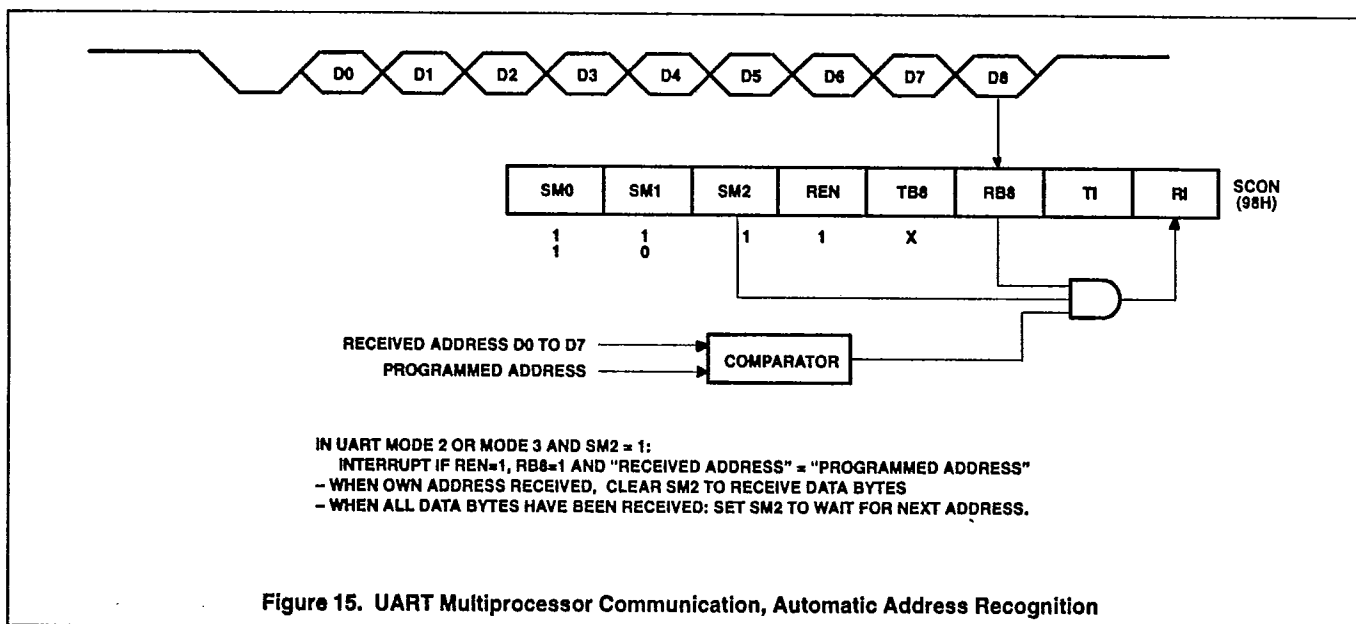
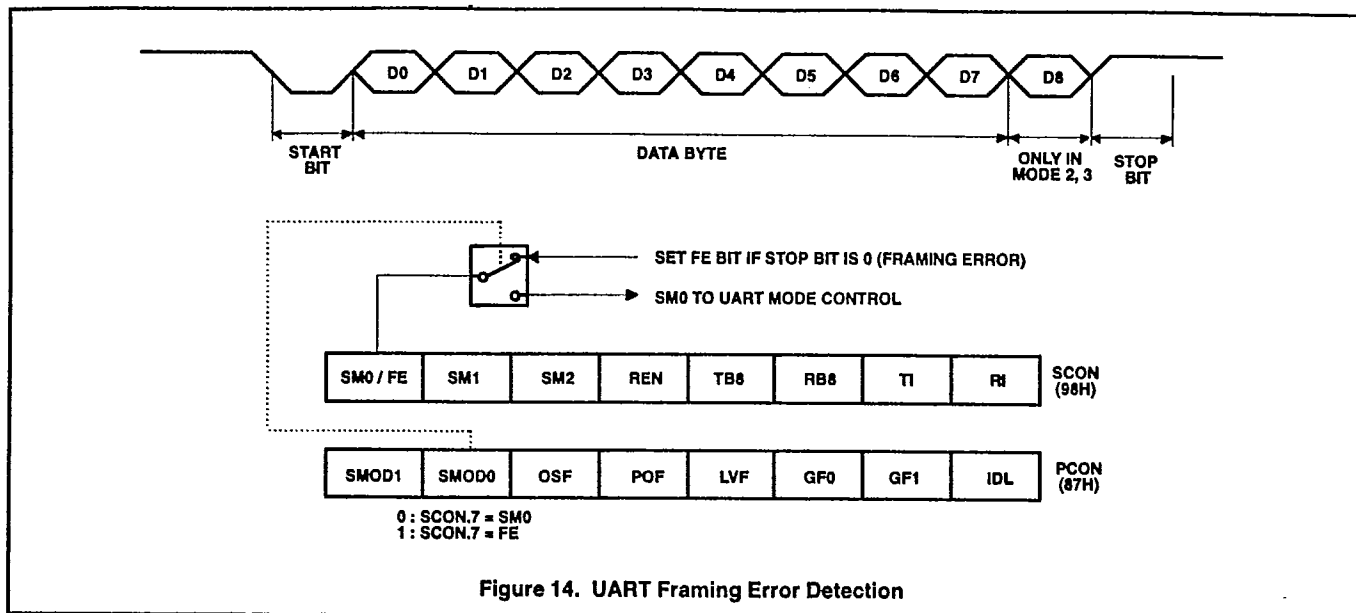
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ABSOLUTE MAXIMUM RATINGS<sup>1, 2, 3</sup>

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70 or -40 to +85	°C
Storage temperature range	-65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to $V_{SS}$	0 to +13.0	V
Voltage on any other pin to $V_{SS}$	-0.5 to +6.5	V
Maximum $I_{OL}$ per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

## NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{SS}$  unless otherwise noted.

## Electrical Deviations from Commercial Specifications for Extended Temperature Range

DC and AC parameters not included here are the same as in the commercial temperature range table.

## DC ELECTRICAL CHARACTERISTICS

 $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{IL}$	Input low voltage, except $\overline{EA}$		-0.5	$0.2V_{CC}-0.15$	V
$V_{IL1}$	Input low voltage to $\overline{EA}$		0	$0.2V_{CC}-0.35$	V
$V_{IH}$	Input high voltage, except XTAL1, RST		$0.2V_{CC}+1$	$V_{CC}+0.5$	V
$V_{IH1}$	Input high voltage to XTAL1, RST		$0.7V_{CC}+0.1$	$V_{CC}+0.5$	V
$I_{IL}$	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.45\text{V}$		-75	$\mu\text{A}$
$I_{TL}$	Logical 1-to-0 transition current, ports 1, 2, 3	$V_{IN} = 2.0\text{V}$		-750	$\mu\text{A}$
$I_{CC}$	Power supply current: Active mode Idle mode Power-down mode	$V_{CC} = 4.5-5.5\text{V}$ , Frequency range = 3.5 to 16MHz		44 12 100	mA mA $\mu\text{A}$

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### DC ELECTRICAL CHARACTERISTICS

$T_{amb} = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP <sup>i</sup>	MAX	
$V_{IL}$	Input low voltage, except EA <sup>7</sup>		-0.5		$0.2V_{CC}-0.1$	V
$V_{IL1}$	Input low voltage to EA <sup>7</sup>		0		$0.2V_{CC}-0.3$	V
$V_{IH}$	Input high voltage, except XTAL1, RST <sup>7</sup>		$0.2V_{CC}+0.9$		$V_{CC}+0.5$	V
$V_{IH1}$	Input high voltage, XTAL1, RST <sup>7</sup>		$0.7V_{CC}$		$V_{CC}+0.5$	V
$V_{OL}$	Output low voltage, ports 1, 2, 3 <sup>9</sup>	$I_{OL} = 100\mu\text{A}$ $I_{OL} = 1.6\text{mA}$ $I_{OL} = 3.5\text{mA}$			0.3 0.45 1.0	V V V
$V_{OL1}$	Output low voltage, port 0, ALE, PSEN <sup>9</sup>	$I_{OL} = 200\mu\text{A}$ $I_{OL} = 3.2\text{mA}$ $I_{OL} = 7.0\text{mA}$			0.3 0.45 1.0	V V V
$V_{OH}$	Output high voltage, ports 1, 2, 3, ALE, PSEN <sup>9</sup>	$I_{OH} = -60\mu\text{A}$ $I_{OH} = -30\mu\text{A}$ $I_{OH} = -10\mu\text{A}$	$V_{CC} - 1.5$ $V_{CC} - 0.7$ $V_{CC} - 0.3$			V V V
$V_{OH1}$	Output high voltage (port 0 in external bus mode), ALE <sup>10</sup> , PSEN <sup>9</sup>	$I_{OH} = -7.0\text{mA}$ $I_{OH} = -3.2\text{mA}$ $I_{OH} = -200\mu\text{A}$	$V_{CC} - 1.5$ $V_{CC} - 0.7$ $V_{CC} - 0.3$			V V V
$I_{IL}$	Logical 0 input current, ports 1, 2, 3 <sup>7</sup>	$V_{IN} = 0.45\text{V}$			-50	$\mu\text{A}$
$I_{TL}$	Logical 1-to-0 transition current, ports 1, 2, 3 <sup>7</sup>	See note 4			-650	$\mu\text{A}$
$I_{LI}$	Input leakage current, port 0	$0.45 V_{IN} < V_{CC} - 0.3$			$\pm 10$	$\mu\text{A}$
$I_{CC}$	Power supply current: <sup>7</sup> Active mode @ 16MHz <sup>5</sup> Idle mode @ 16MHz Power-down mode	See note 6		15 3 10	40 10 100	mA mA $\mu\text{A}$
$R_{RST}$	Internal reset pull-down resistor		50		225	k $\Omega$
$C_{IO}$	Pin capacitance <sup>11</sup> (except EA)				15	pF

#### NOTES:

- Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the  $V_{OL}$ s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading  $> 100\text{pF}$ ), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.  $I_{OL}$  can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
- Capacitive loading on ports 0 and 2 may cause the  $V_{OH}$  on ALE and PSEN to momentarily fall below the  $0.9V_{CC}$  specification when the address bits are stabilizing.
- Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when  $V_{IN}$  is approximately 2V.
- $I_{CCMAX}$  at other frequencies is given by: Active mode:  $I_{CCMAX} = 1.50 \times \text{FREQ} + 8$ ; Idle mode:  $I_{CCMAX} = 0.14 \times \text{FREQ} + 2.31$ , where FREQ is the external oscillator frequency in MHz.  $I_{CCMAX}$  is given in mA. See Figure 23.
- See Figures 24 through 27 for  $I_{CC}$  test conditions.
- These values apply only to  $T_{amb} = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ . For  $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , see table on previous page.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:  
Maximum  $I_{OL}$  per port pin: 15mA (\*NOTE: This is 85°C specification.)  
Maximum  $I_{OL}$  per 8-bit port: 26mA  
Maximum total  $I_{OL}$  for all outputs: 71mA  
If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- ALE is tested to  $V_{OH1}$ , except when ALE is off then  $V_{OH}$  is the voltage specification.
- Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except EA it is 25pF).

# CMOS single-chip 8-bit microcontrollers

## 83C51FC/87C51FC

### AC ELECTRICAL CHARACTERISTICS

T<sub>amb</sub> = 0°C to +70°C or -40°C to +85°C, V<sub>CC</sub> = 5V ±10%, V<sub>SS</sub> = 0V<sup>1, 2, 3</sup>

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
1/t <sub>CLCL</sub>	16	Oscillator frequency -4 -5 -A -B			3.5 3.5	16 24	MHz MHz
t <sub>LHLL</sub>	16	ALE pulse width	85		2t <sub>CLCL</sub> -40		ns
t <sub>AVLL</sub>	16	Address valid to ALE low	22		t <sub>CLCL</sub> -40		ns
t <sub>LLAX</sub>	16	Address hold after ALE low	32		t <sub>CLCL</sub> -30		ns
t <sub>LLIV</sub>	16	ALE low to valid instruction in		150		4t <sub>CLCL</sub> -100	ns
t <sub>LLPL</sub>	16	ALE low to PSEN low	32		t <sub>CLCL</sub> -30		ns
t <sub>PLPH</sub>	16	PSEN pulse width	142		3t <sub>CLCL</sub> -45		ns
t <sub>PLIV</sub>	16	PSEN low to valid instruction in		82		3t <sub>CLCL</sub> -105	ns
t <sub>PIXI</sub>	16	Input instruction hold after PSEN	0		0		ns
t <sub>PIXZ</sub>	16	Input instruction float after PSEN		37		t <sub>CLCL</sub> -25	ns
t <sub>AVIV</sub>	16	Address to valid instruction in		207		5t <sub>CLCL</sub> -105	ns
t <sub>PLAZ</sub>	16	PSEN low to address float		10		10	ns
<b>Data Memory</b>							
t <sub>RLRH</sub>	17, 18	RD pulse width	275		6t <sub>CLCL</sub> -100		ns
t <sub>WLWH</sub>	17, 18	WR pulse width	275		6t <sub>CLCL</sub> -100		ns
t <sub>RLDV</sub>	17, 18	RD low to valid data in		147		5t <sub>CLCL</sub> -165	ns
t <sub>RHDZ</sub>	17, 18	Data hold after RD	0		0		ns
t <sub>RHDZ</sub>	17, 18	Data float after RD		65		2t <sub>CLCL</sub> -60	ns
t <sub>LLDV</sub>	17, 18	ALE low to valid data in		350		8t <sub>CLCL</sub> -150	ns
t <sub>AVDV</sub>	17, 18	Address to valid data in		397		9t <sub>CLCL</sub> -165	ns
t <sub>LLWL</sub>	17, 18	ALE low to RD or WR low	137	237	3t <sub>CLCL</sub> -50	3t <sub>CLCL</sub> +50	ns
t <sub>AVWL</sub>	17, 18	Address valid to WR low or RD low	175		4t <sub>CLCL</sub> -75		ns
t <sub>QVWX</sub>	17, 18	Data valid to WR transition	42		t <sub>CLCL</sub> -20		ns
t <sub>WHQX</sub>	17, 18	Data hold after WR	42		t <sub>CLCL</sub> -20		ns
t <sub>QVWH</sub>	18	Data valid to WR high	287		7t <sub>CLCL</sub> -150		ns
t <sub>RLAZ</sub>	17, 18	RD low to address float		0		0	ns
t <sub>WHLH</sub>	17, 18	RD or WR high to ALE high	40	87	t <sub>CLCL</sub> -20	t <sub>CLCL</sub> +25	ns
<b>External Clock</b>							
t <sub>CHCX</sub>	20	High time	12		20		ns
t <sub>CLCX</sub>	20	Low time	12		20		ns
t <sub>CLCH</sub>	20	Rise time		20		20	ns
t <sub>CHCL</sub>	20	Fall time		20		20	ns
<b>Shift Register</b>							
t <sub>XLXL</sub>	19	Serial port clock cycle time	1		12t <sub>CLCL</sub>		μs
t <sub>QVXH</sub>	19	Output data setup to clock rising edge	492		10t <sub>CLCL</sub> -133		ns
t <sub>XHQX</sub>	19	Output data hold after clock rising edge	8		2t <sub>CLCL</sub> -117		ns
t <sub>XHDX</sub>	19	Input data hold after clock rising edge	0		0		ns
t <sub>XHDV</sub>	19	Clock rising edge to input data valid		492		10t <sub>CLCL</sub> -133	ns

#### NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- Interfacing the 8XC51FC to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

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## EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address  
C – Clock  
D – Input data  
H – Logic level high  
I – Instruction (program memory contents)  
L – Logic level low, or ALE

P – PSEN  
Q – Output data  
R – RD signal  
t – Time  
V – Valid  
W – WR signal  
X – No longer a valid logic level  
Z – Float

Examples:  $t_{AVLL}$  = Time for address valid to ALE low.  
 $t_{LLPL}$  = Time for ALE low to PSEN low.

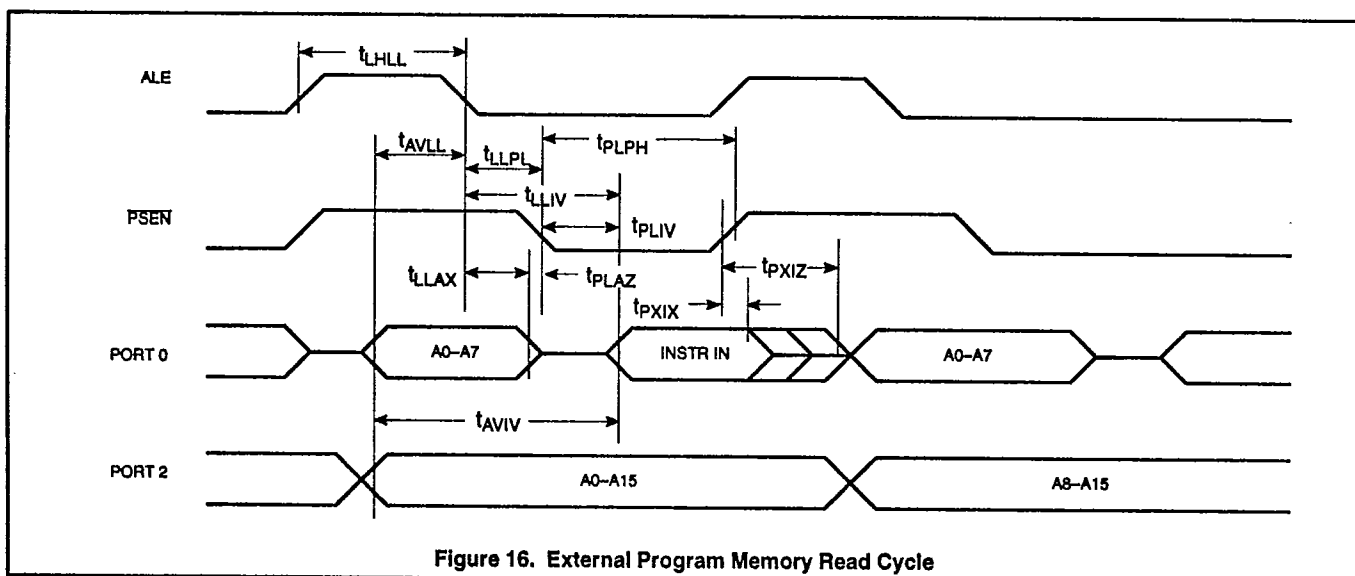


Figure 16. External Program Memory Read Cycle

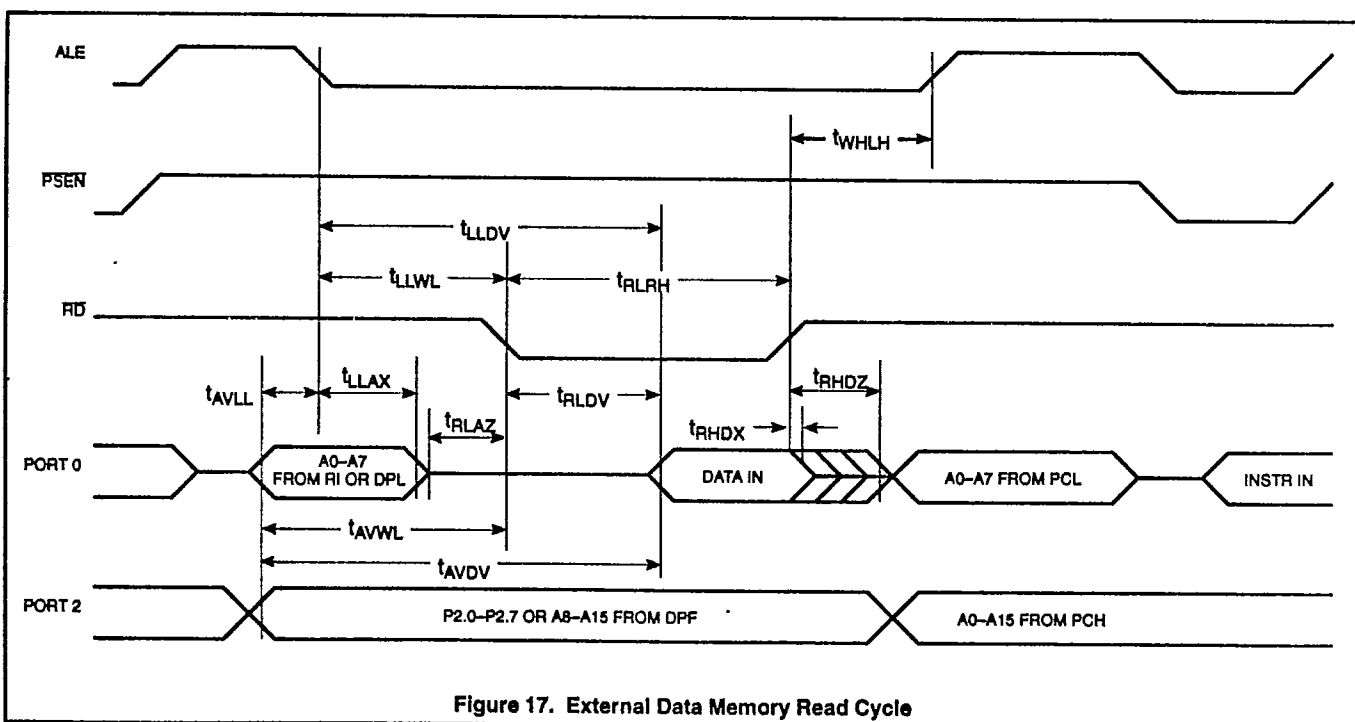


Figure 17. External Data Memory Read Cycle

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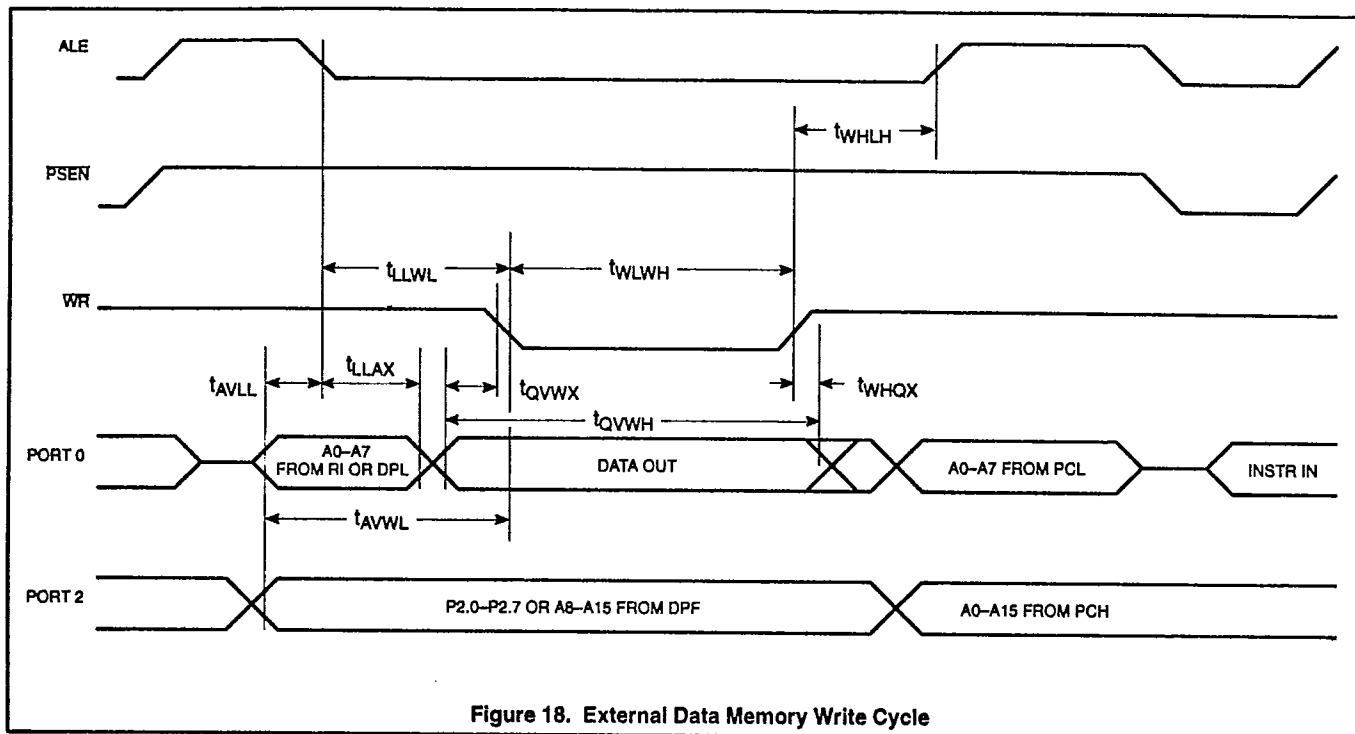


Figure 18. External Data Memory Write Cycle

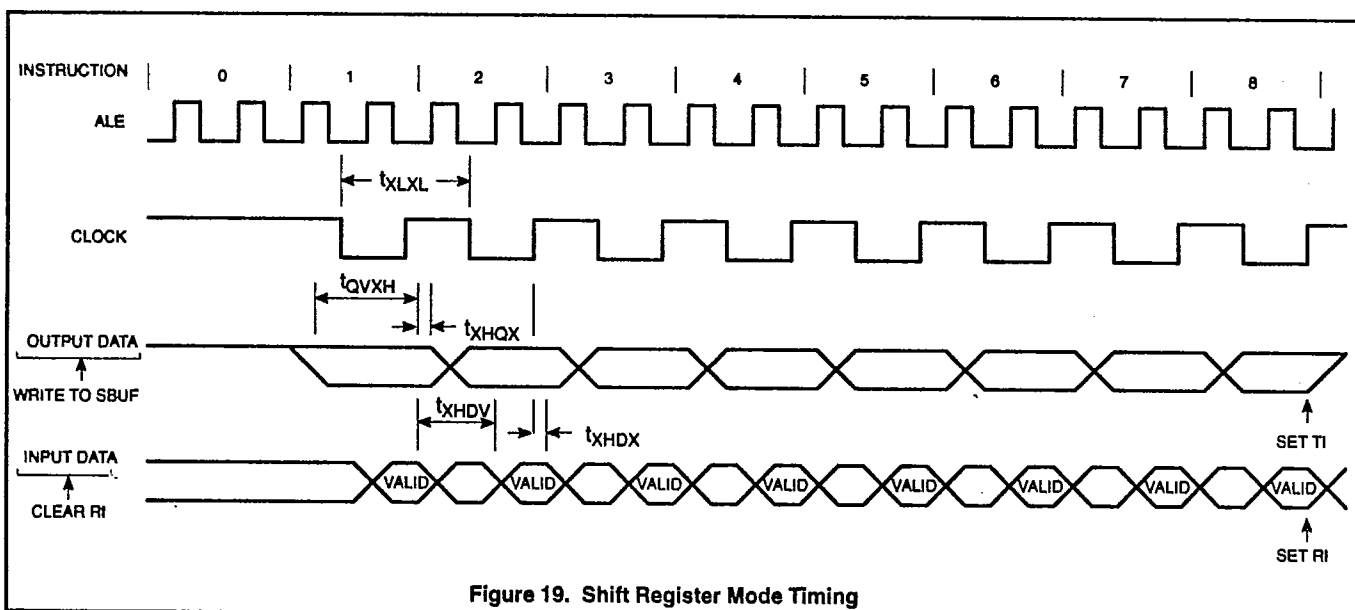


Figure 19. Shift Register Mode Timing

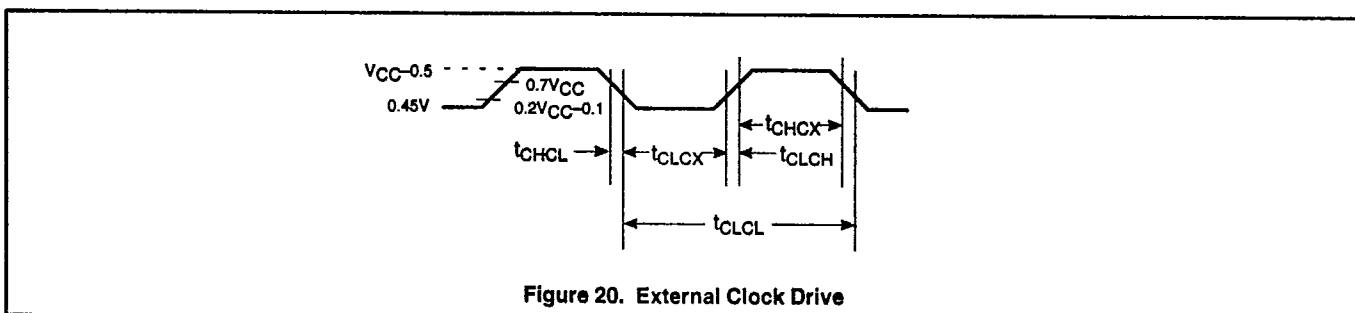


Figure 20. External Clock Drive

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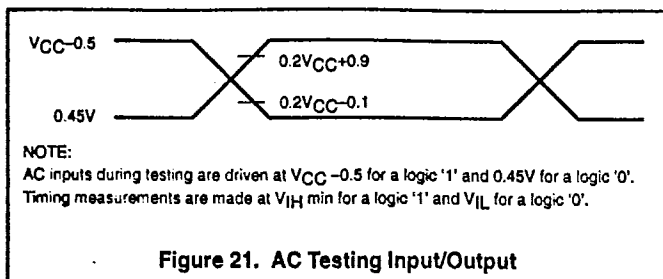


Figure 21. AC Testing Input/Output

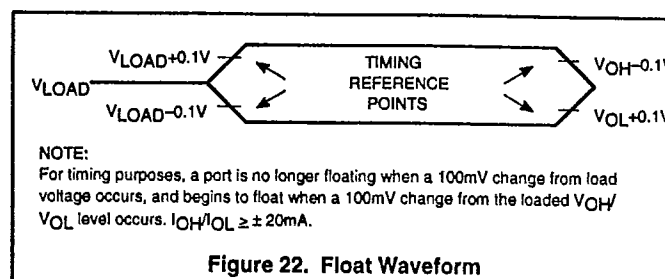
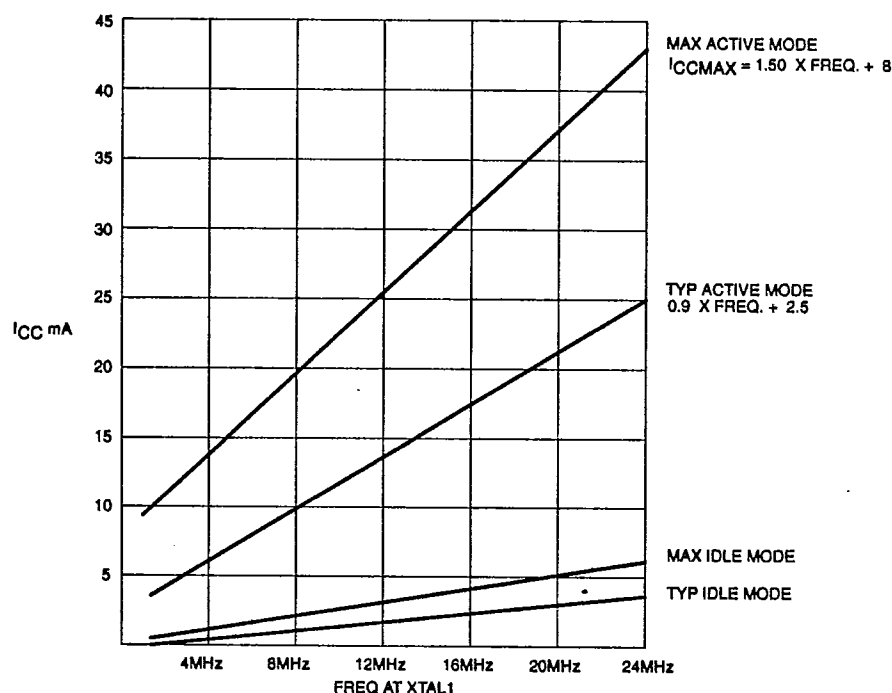
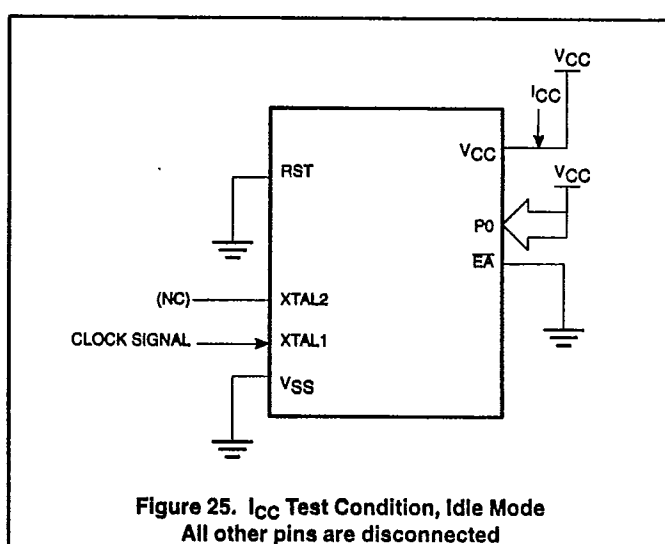
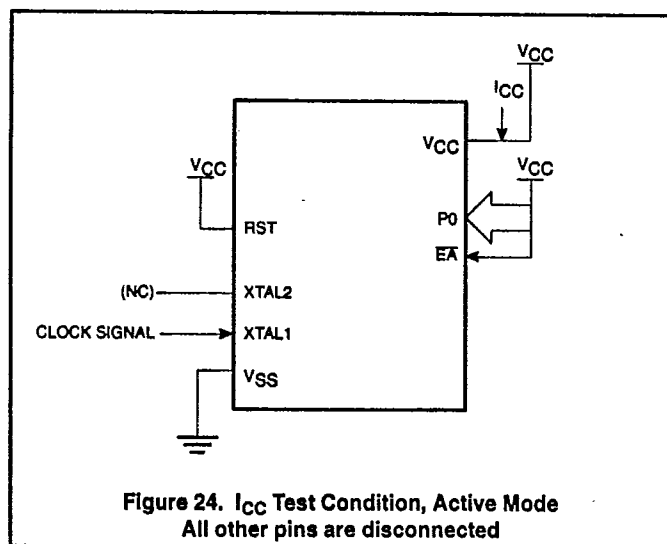


Figure 22. Float Waveform


Figure 23.  $I_{CC}$  vs. FREQ Valid only within frequency specifications of the device under test


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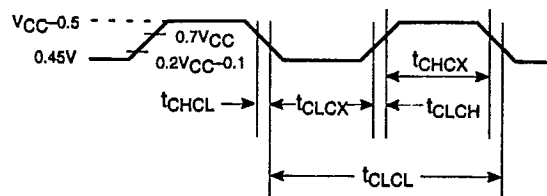


Figure 26. Clock Signal Waveform for  $I_{CC}$  Tests in Active and Idle Modes  
 $t_{CLCH} = t_{CHCL} = 5\text{ns}$

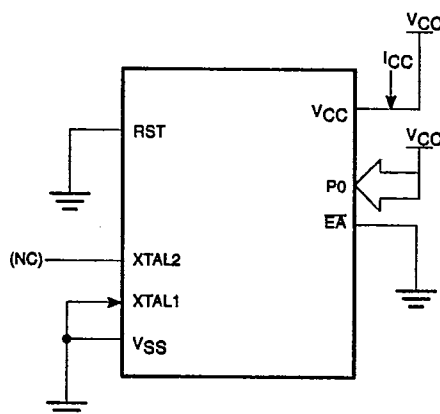


Figure 27.  $I_{CC}$  Test Condition, Power Down Mode  
All other pins are disconnected.  $V_{CC} = 2\text{V to } 5.5\text{V}$

## EPROM CHARACTERISTICS

The 87C51FC is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for  $V_{PP}$  (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C51FC contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C51FC manufactured by Philips.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 28 and 29. Figure 30 shows the circuit configuration for normal program memory verification.

## Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 28. Note that the 87C51FC is running with a 4 to 6MHz oscillator. The reason the oscillator needs to

be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 28. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 2 and 3 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3. The ALE/PROG is pulsed low 25 times as shown in Figure 29.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the 25 pulse programming sequence using the 'Pgm Security Bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed.

Note that the EA/ $V_{PP}$  pin must not be allowed to go above the maximum specified  $V_{PP}$  level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The  $V_{PP}$  source should be well regulated and free of glitches and overshoot.

## Program Verification

If security bits 2 and 3 have not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 30. The other pins are held at the 'Verify Code Data' levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the 64 byte encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

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## CMOS single-chip 8-bit microcontrollers

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**Reading the Signature Bytes**

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = B3H indicates 87C51FC

**Program/Verify Algorithms**

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

**Erase Characteristics**

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345-5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-s/cm<sup>2</sup>. Exposing the EPROM to an ultraviolet lamp of 12,000μW/cm<sup>2</sup> rating for

20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

**Security Bits**

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 is programmed, MOV<sub>C</sub> instructions executed from external program memory are disabled from fetching code bytes from the internal memory, EA is latched on Reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

**Table 3. EPROM Programming Modes**

MODE	RST	PSEN	ALE/PROG	EA/V <sub>PP</sub>	P2.7	P2.6	P3.7	P3.6	P3.3
Read signature	1	0	1	1	0	0	0	0	0
Program code data	1	0	0*	V <sub>PP</sub>	1	0	1	1	1
Verify code data	1	0	1	1	0	0	1	1	0
Pgm encryption table	1	0	0*	V <sub>PP</sub>	1	0	1	0	1
Pgm security bit 1	1	0	0*	V <sub>PP</sub>	1	1	1	1	1
Pgm security bit 2	1	0	0*	V <sub>PP</sub>	1	1	0	0	1
Pgm security bit 3	1	0	0*	V <sub>PP</sub>	0	1	0	1	1

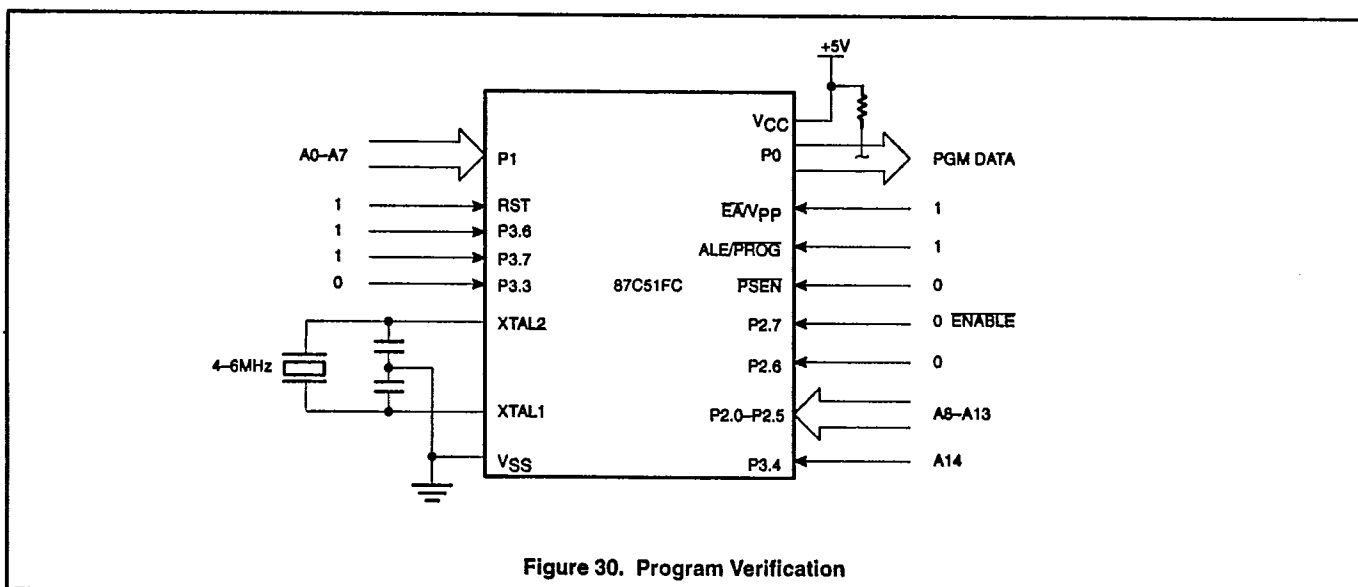
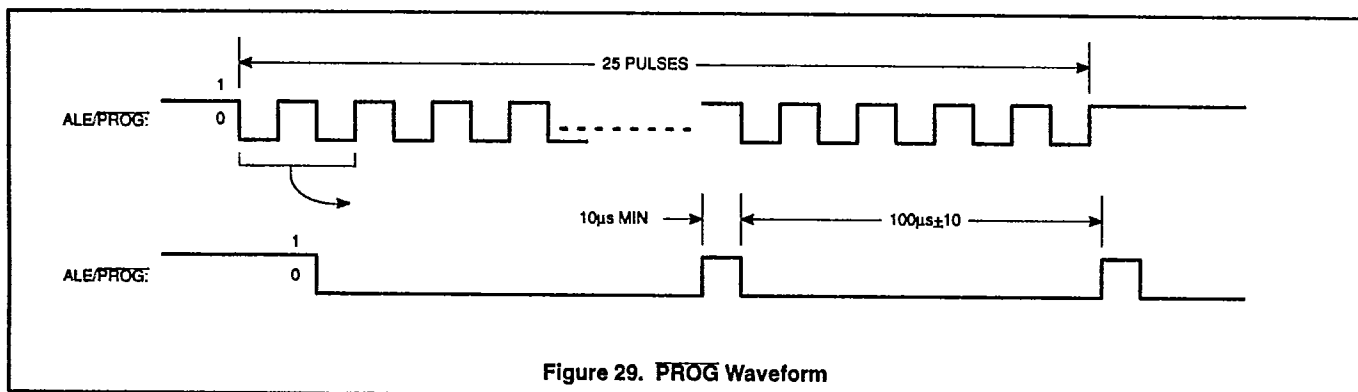
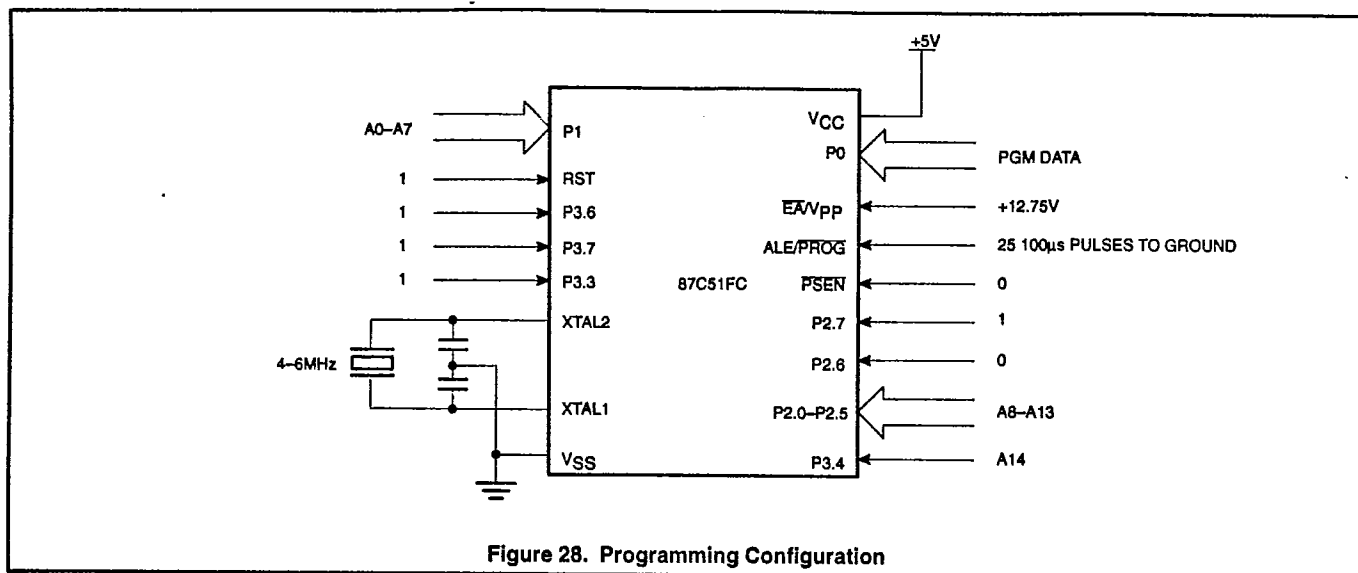
**NOTES:**

- '0' = Valid low for that pin, '1' = valid high for that pin.
- V<sub>PP</sub> = 12.75V ±0.25V.
- V<sub>CC</sub> = 5V ±10% during programming and verification.
- \* ALE/PROG receives 25 programming pulses while V<sub>PP</sub> is held at 12.75V. Each programming pulse is low for 100μs (±10μs) and high for a minimum of 10μs.



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### EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_{amb} = 21^{\circ}\text{C}$  to  $+27^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$  (See Figure 31)

SYMBOL	PARAMETER	MIN	MAX	UNIT
$V_{PP}$	Programming supply voltage	12.5	13.0	V
$I_{PP}$	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
$t_{AVGL}$	Address setup to PROG low	$48t_{CLCL}$		
$t_{GHAX}$	Address hold after PROG	$48t_{CLCL}$		
$t_{DVGL}$	Data setup to PROG low	$48t_{CLCL}$		
$t_{GHDX}$	Data hold after PROG	$48t_{CLCL}$		
$t_{EHS}$	P2.7 (ENABLE) high to $V_{PP}$	$48t_{CLCL}$		
$t_{SHGL}$	$V_{PP}$ setup to PROG low	10		$\mu\text{s}$
$t_{GHSL}$	$V_{PP}$ hold after PROG	10		$\mu\text{s}$
$t_{GLGH}$	PROG width	90	110	$\mu\text{s}$
$t_{AVQV}$	Address to data valid		$48t_{CLCL}$	
$t_{ELQZ}$	ENABLE low to data valid		$48t_{CLCL}$	
$t_{EHQZ}$	Data float after ENABLE	0	$48t_{CLCL}$	
$t_{GHGL}$	PROG high to PROG low	10		$\mu\text{s}$

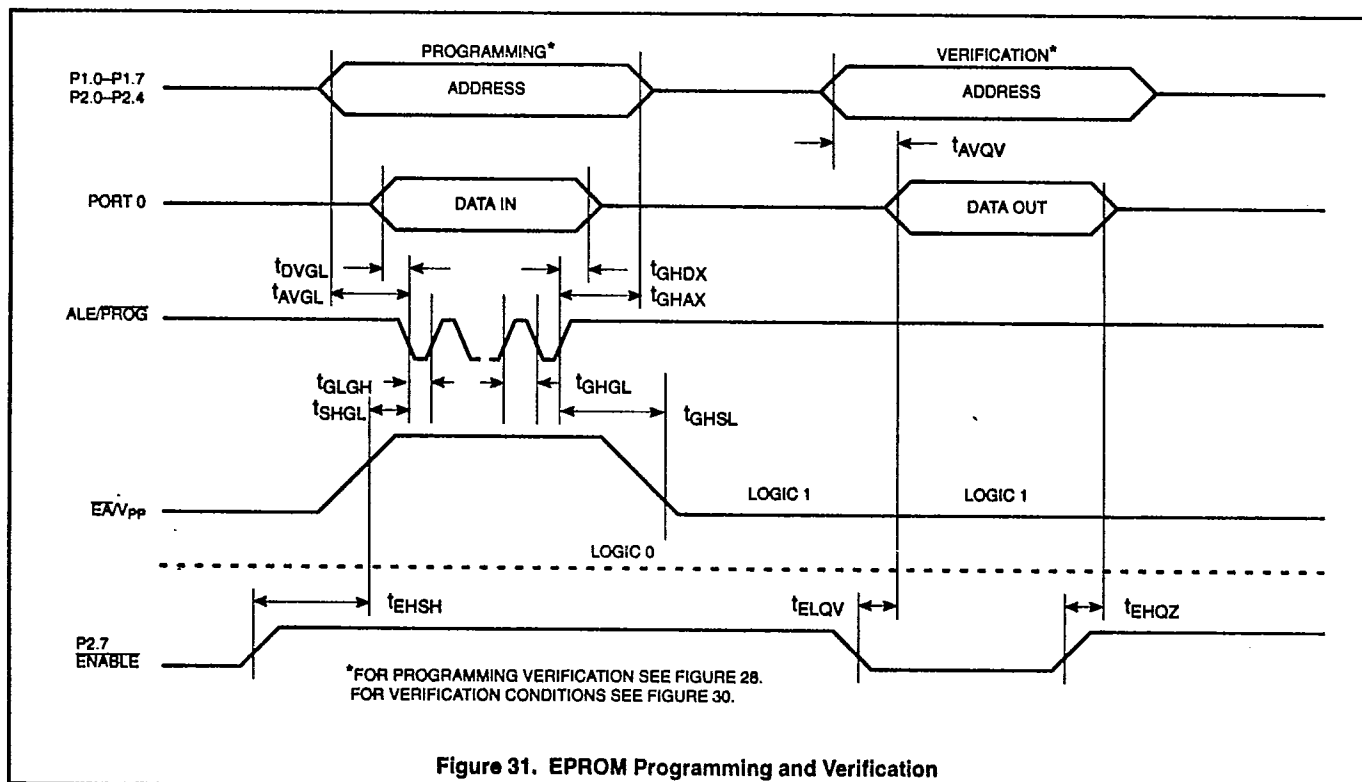


Figure 31. EPROM Programming and Verification