



### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$ .....	40V
Magnetic Amp. Source Voltage, $V_M$ .....	40V
Reset Output Voltage, $V_R$ .....	-120V
Total Current Source Voltage, $V_M - V_R$ .....	-140V
Amplifier Input Range .....	-0.3V to $V_{CC}$
Reset Input Current, $I_{DR}$ .....	-10mA
Power Dissipation at $T_A = 25^\circ\text{C}$	
Q, N, DP Package .....	2W
J, L Package .....	1W
Power Dissipation at $T$ (leads/case) = $25^\circ\text{C}$	
Q, N, DP Package .....	5W
J, L Package .....	2W
Operating Temperature Range .....	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Storage Temperature Range .....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec) .....	$300^\circ\text{C}$

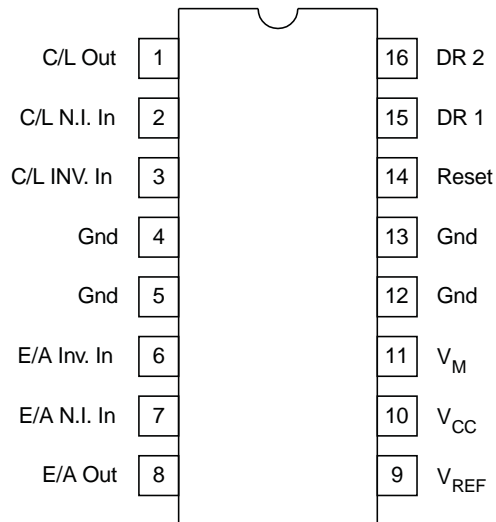
Note: All voltages are with respect to ground pins. All currents are positive into the specified terminal. Consult Packaging section of Databook for thermal limitations and considerations of package.

### ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1838AJ UC1838AL	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	Ceramic Dip CLCC
UC2838ADP UC2838AN UC2838AQ	$-20^\circ\text{C}$ to $+85^\circ\text{C}$	Power SOIC Plastic Dip PLCC
UC3838ADP UC3838AN UC3838AQ	$0^\circ\text{C}$ to $+70^\circ\text{C}$	Power SOIC Plastic Dip PLCC

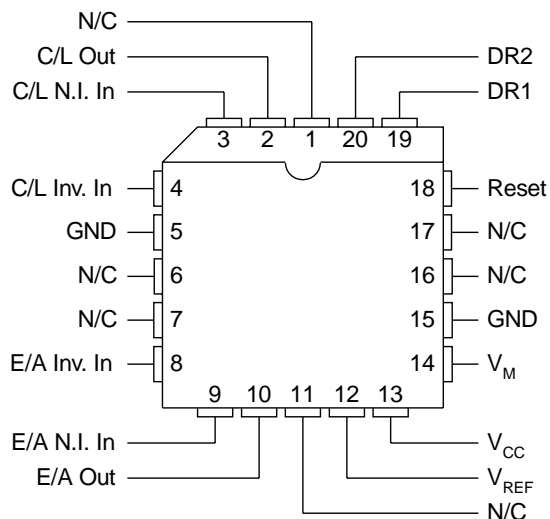
### CONNECTION DIAGRAMS

#### DIL-16, SOIC-16 (TOP VIEW) J or N Package, DP Package



Note: All four ground pins must be connected to a common ground

#### PLCC-20, LCC-20 (TOP VIEW) Q, L Packages

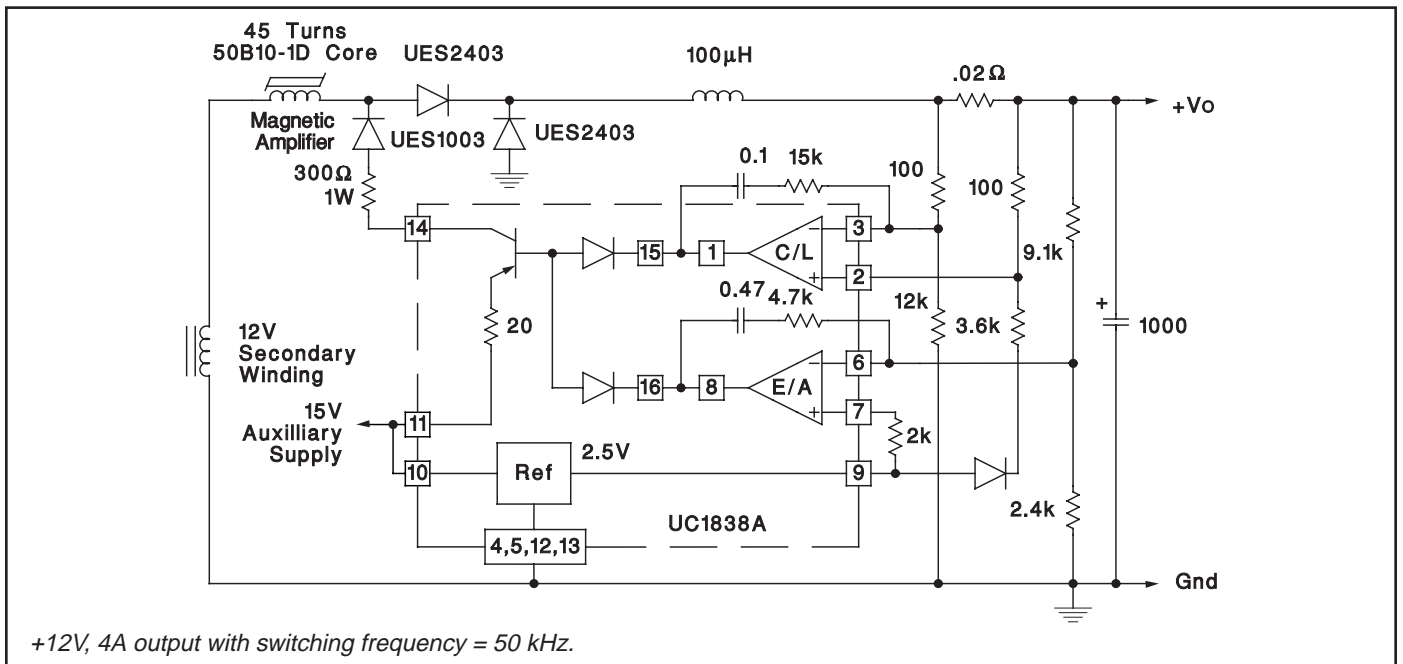


**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1838A,  $-20^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2838A, and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3838A,  $V_{CC} = 20\text{V}$ ,  $V_M = 5\text{V}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1838A / UC2838A			UC3838A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Reference Section</b>								
Supply Current	$V_{CC} = V_M = 40\text{V}$		4	8		4	8	mA
Reference Output	$T_A = 25^\circ\text{C}$	2.47	2.5	2.53	2.45	2.5	2.55	V
Line Regulation	$V_{CC} = 5$ to $30\text{V}$		1	5		1	10	mV
Load Regulation	$I_O = 0$ to $-2\text{mA}$		5	20		5	20	mV
Short Circuit Current	$V_{REF} = 0\text{V}$		-30	-60		-30	-60	mA
Temperature Stability*	Over Operating Temp. Range		15	25		10	25	mV
<b>Amplifier Section (Each Amplifier)</b>								
Offset Voltage	$V_{CM} = 2.5\text{V}$			5			10	mV
Input Bias Current	$V_{IN} = 0\text{V}$			-1			-1	$\mu\text{A}$
Input Offset Current				100			100	nA
Minimum Output Swing		0.4		18	0.4		18	V
Output Sink Current	$V_O = 5\text{V}$	1	10	30	1	10	30	mA
Output Source Current	$V_O = 0\text{V}$	-1	-10	-20	-1	-10	-20	mA
$A_{VOL}$	$V_O = 1$ to $11\text{V}$	100	120		100	120		dB
CMRR	$V_{IN} = 1$ to $11\text{V}$	70	80		70	80		dB
PSRR	$V_{CC} = 10$ to $20\text{V}$	70	100		70	100		dB
Gain Bandwidth*		0.6	0.8		0.6	0.8		MHz
<b>Reset Drive Section</b>								
Input Leakage	$V_{DR} = 40\text{V}$			10			10	$\mu\text{A}$
Output Leakage	$V_R = -120\text{V}$			-100			-100	$\mu\text{A}$
Input Current	$I_R = -50\text{mA}$		-1	-2		-1	-2	mA
Maximum Reset Current	$I_{DR} = -3\text{mA}$	-100	-120	-200	-100	-120	-200	mA
Transconductance	$I_R = -10$ to $-50\text{mA}$	.03	.042	.055	.03	.042	.055	A/V

\* These parameters are guaranteed by design but not 100% tested in production.

**TYPICAL APPLICATION**



APPLICATION INFORMATION

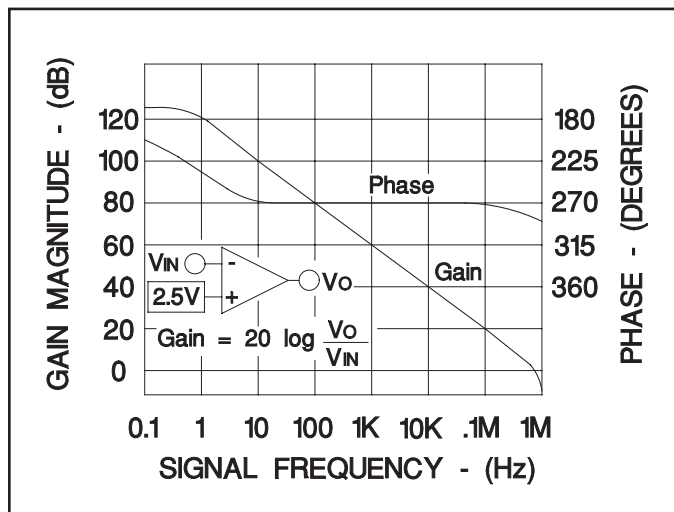


Figure 1. Amplifier open loop response.

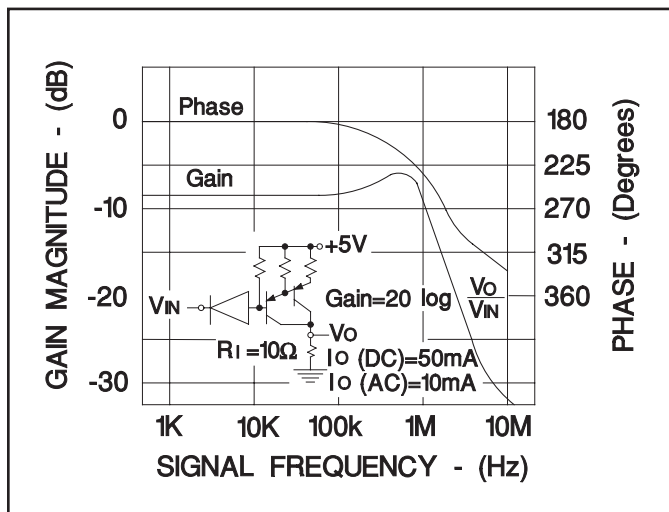


Figure 4. Reset driver response.

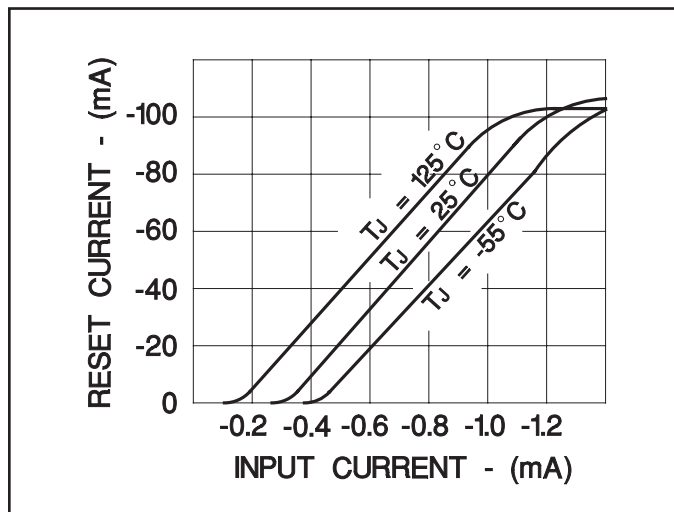


Figure 2. Reset driver-input current.

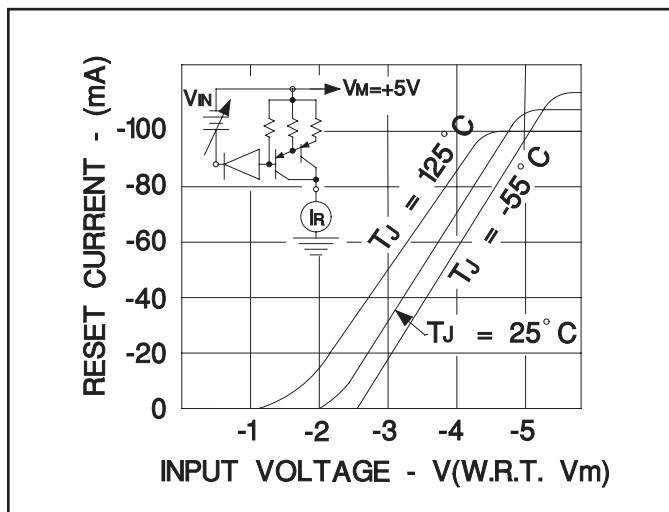


Figure 5. Reset driver-input voltage.

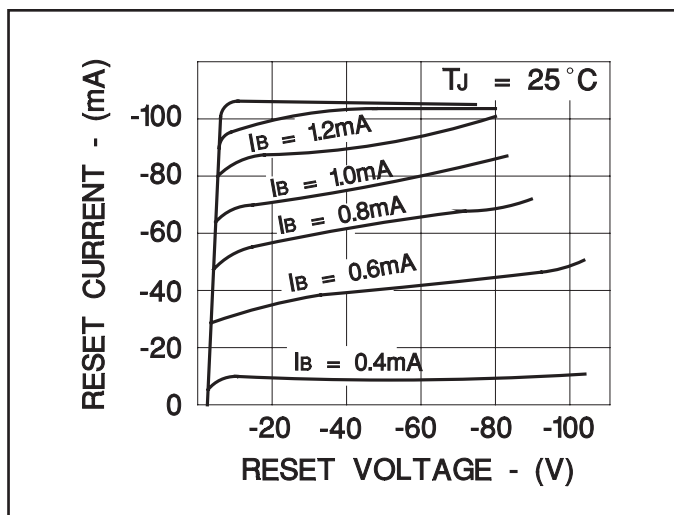


Figure 3. Reset driver-output impedance.

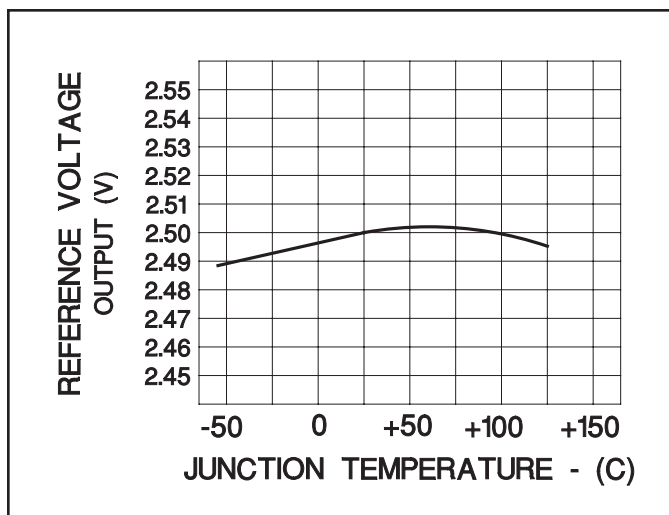


Figure 6. Reference temperature coefficient.

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