iChip™

iChip CO561AD-S
iChip CO561AD-C
iChip LAN CO561AD-L
Datasheet

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1.0	November 1999	Original Release for iChip CO561AD-S. Author Amit Resh
4.0	November 2000	Updated with iChip LAN CO561AD-L. Author Jakob Apelblat
5.0	February 2001	Parallel modem obsolete. Figure 4-1 iChip pin names changed for pin #14, 21, 40, 61 - 66. Figure 4-2 iChip pin names changed for pin #14, 21, 28 – 30, 40, 61 – 63, 65. Removed components for debugging from reference designs. Author Jakob Apelblat
5.1	March 2001	Chapter 2 “Ordering Information” is new. Figure 6-3, pin 61 of U2 connected to VCC, 56 no pin, 55, 54 changed, pin 40 of U1 connected via pull up to VCC, U3A changed to U4. Figure 6-4, pin 40 of U1 connected via pull up to VCC. Figure 7-1, pin 53, 56 changed. Figure 7-3, 55, 54 changed. Table 6-1, #27 P/N changed, #23, R10 added, #17, #28, #29, #32 updated. Table 6-2, #14, R19 added, #11, #22, #24, #25, #27 updated. “2.1 Overview” updated. “2.2.6 Local Bus Connection to Ethernet Controller” updated. “4.3.3 iChip Serial Modem Signals” MMSEL updated. Chapter “6.3 Mechanical Dimensions” has been updated. Chapter 7.6 “PLD Equations” reset removed. Author Jakob Apelblat

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1 Introduction

Description

The iChip™ Internet Controller™ is a family of low-cost intelligent peripheral device that provide Internet connectivity solutions to a myriad of embedded devices. Two firmware versions are available: iChip CO561AD-S for dial-up and wireless Internet connectivity, and iChip LAN™ CO561AD-L for 10BaseT Ethernet LAN Internet connectivity. For the sake of consistency, the name “iChip” is used herein when referring to both iChip CO561AD-S and iChip LAN. Otherwise, the specific product name is used.

The Socket iChip™ Internet Controller, CO561AD-C, is the iChip CO561AD-S on a carrier board that is pin-compatible with Conexant SocketModem™.

As an embedded, self-contained Internet engine, iChip acts as mediator device between a host processor and an Internet communications platform. By completely offloading Internet connectivity and standard protocols, it relieves the host from the burden of handling Internet communications. From the perspective of a host device, the complexity of establishing and maintaining Internet-related sessions are reduced to simple, straightforward commands that are entirely dealt with within iChip’s domain.

A serial bus interfaces iChip CO561AD-S to a device’s host processor via an on-chip UART. An optional 8/16-bit parallel interface to a host processor is supported as well by adding an external UART for low-bandwidth applications or a dual-port-RAM for high bandwidth applications. iChip CO561AD-S also directly interfaces a serial data modem, through which it supports independent communications on the Internet via a dial-up ISP connection.

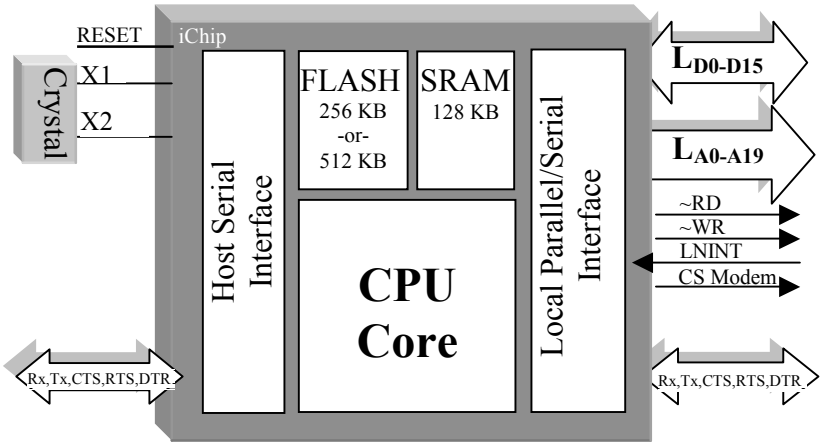
In addition to supporting dial-up modems, iChip CO561AD-S also supports GSM modems.

Through its host Application Programming Interface (API), iChip accepts commands formatted in Connect One's AT+i™ extension to the renowned Hayes AT command set. Commands are available to store and manipulate functional and Internet-related non-volatile parameter data; transmit and receive textual Email messages; transmit and receive binary (MIME encoded) Email messages; fetch HTML web pages; and download parameter and firmware updates for the host device or iChip itself. Send command variants exist for immediate communications or scheduled "store-and-forward”. iChip supports several levels of status reporting to the host. When the host CPU issues standard AT commands, iChip CO561AD-S gains direct access to the modem, and automatically operates in transparent mode, emulating a direct host-to-modem environment.

iChip LAN™ supports 10BaseT Ethernet LANs with the addition of an external 16-bit Cirrus Logic Crystal LAN CS8900A Ethernet controller. AT commands enable iChip LAN to send and receive Internet commands through the LAN.

Upon receiving an AT+i command, iChip operates in Internet mode, controls the modem or Ethernet controller, and independently manages standard Internet protocols to transmit and receive messages. iChip provides all the necessary procedures to log onto an ISP, authenticate the user and establish an Internet session.

Functional Block Diagram



Pin Diagram

PLCC68

Figure 1-1 iChip Functional Block Diagram

General Features

- Microprocessor-controllable through a standard serial connection or optional parallel bus.
- Supports remote firmware update by host, email, or direct modem-to-modem communications.
- Includes onboard 128KB SRAM and 256KB or 512KB flash memory.
- Supports up to 1MB of external memory.
- Driven by Connect One's "AT+i" extension to the AT command set.
- Stand-alone Internet communication capabilities.
- Binary Base64 encoding and MIME.
- Opens up to 5 TCP or UDP sockets.
- Power save mode reduces power consumption.
- 3.3 and 5V versions available, CMOS technology.
- Onboard non-volatile memory stores all functional and Internet-related parameters.
- Supports several layers of status reports.
- Internal self-test procedures.
- Internal "Watch-Dog" guard circuit.
- Auto baud rate detection.
- Includes hardware and software flow control.
- PLCC68 package.

Dial-up Features

- Supports following Internet Protocols and formats:
  PPP, LCP, IPCP, IP, TCP, UDP, DNS, SMTP, POP3, HTTP and PAP, CHAP, or Script authentication.
- Supports data modems up to 56 Kbps throughput.
- Supports GSM modems.
- Stay-on-line feature for multiple send/receive.

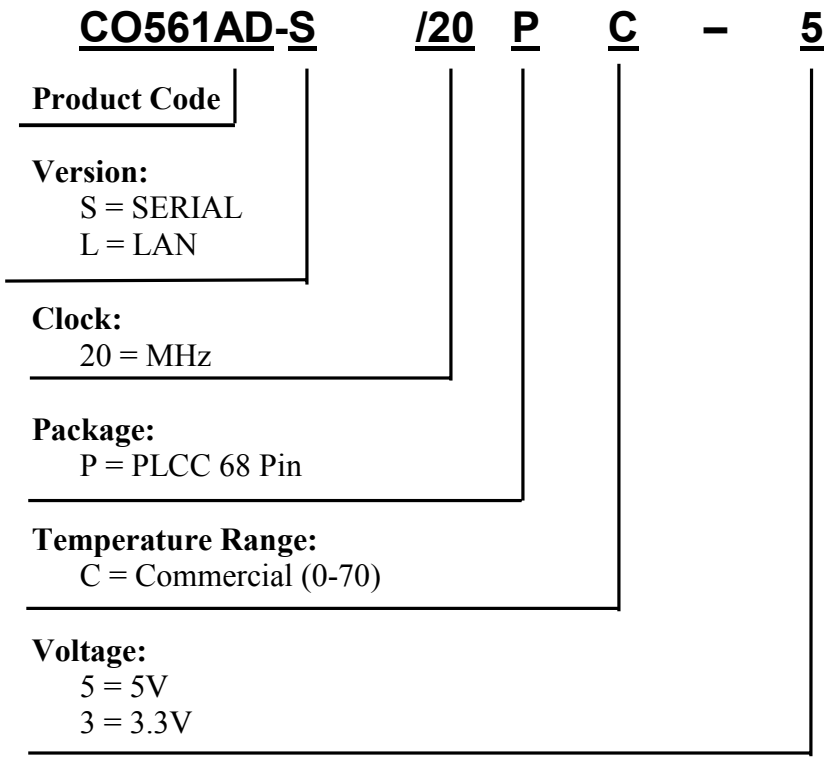
LAN Features

- Supports following Internet Protocols and formats:
  ARP, IP, ICMP, TCP, UDP, DNS, DHCP, SMTP, POP3, MIME, and HTTP.
- Provides 10BaseT Ethernet LAN connectivity via Crystal LAN CS8900A Ethernet controller
- Supports up to 230 Kbps throughput.

2 Ordering Information

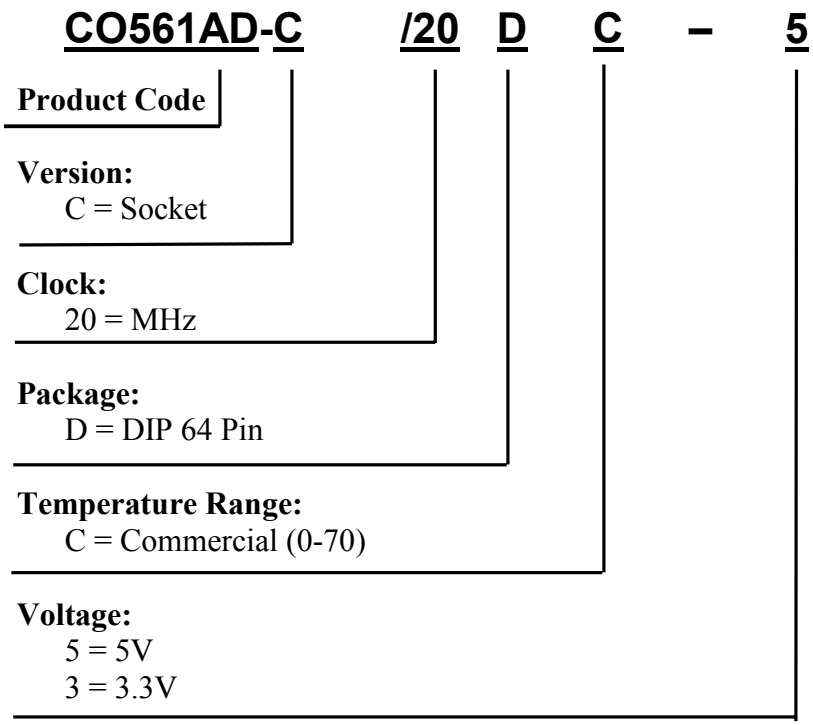
2.1 iChip / iChip LAN Order Number

Connect One's standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



2.2 Socket iChip Order Number

Connect One's standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



3 Functional Description

3.1 Overview

Connect One's iChip Internet Controller is an integrated, firmware-driven, self-contained Internet engine that is available in a 68-pin PLCC package. iChip accepts simple ASCII commands from a host CPU via a serial communication bus and manages an Internet communication session to send and receive Email and web pages, and to open and close sockets through a linked modem or Ethernet communications platform.

For dial-up and GSM cellular modem configurations, iChip CO561AD-S is available in two forms: CO561AD-S interfaces a serial modem. CO561AD-S is also available mounted on a carrier board, CO561AD-C that is pin-compatible with Conexant's SocketModem.

For 10BaseT Ethernet applications, iChip LAN CO561AD-L includes the firmware and pin-out necessary to drive an external Crystal LAN CS8900A 10BaseT Ethernet controller.

iChip CO561AD-S and iChip LAN contain non-volatile FLASH memory to store their firmware and Internet-related operational parameters. Remote firmware and parameter updates are supported through the host link, by Email or directly through the communications platform.

3.2 Technical Specifications

3.2.1 General

iChip constitutes a complete Internet messaging solution for non-PC embedded devices. It acts as a mediator device to completely offload the host processor of Internet-related software and activities. An industry-standard asynchronous serial link connects iChip to the host processor. Programming, monitoring and control are fully supported using Connect One's AT+i extension to the standard AT command set.

An additional industry-standard asynchronous serial link connects iChip CO561AD-S to a standard serial modem ,while iChip LAN CO561AD-L connects to an Ethernet MAC for Internet access. In serial modem configurations, iChip supports direct host-to-modem operations using the standard AT command set.

3.2.2 Data Rates

iChip supports standard baud rate configurations from 2,400 bps up to 57,600 bps, while iChip LAN supports bandwidth up to 230,000 bps on the host asynchronous serial communications bus. For safety reasons, iChip is shipped with a default zero connection rate. The default baud rate may be changed permanently by using the AT+iBDR command.

3.2.3 Operation

All iChip Internet and parameter operations are controlled by AT+i commands.

3.2.3.1 Transparent Mode

In modem configurations, iChip CO561AD-S defaults to transparent mode, allowing the host to control the modem device directly. Control is implemented by the host issuing standard AT commands to iChip. In this mode, iChip CO561AD-S transparently echoes the AT commands to the modem, as well as echoing the modem responses back to the host. In addition, hardware flow control signals are emulated on the host side to reflect the levels set by the modem and vice-versa. iChip CO561AD-S supports interlacing AT+i and AT commands, while the modem is in command mode.

When the modem is put into data mode, by issuing a dial command, transparent mode is sustained throughout the data-mode session.

3.2.3.2 Command Mode

iChip commands are implemented using the AT+i command set. Command flow exists only on the host serial bus between the host and iChip.

3.2.3.3 Internet Mode

iChip enters Internet mode after being issued an Internet messaging command to send or receive an Email message. iChip attempts to establish an Internet connection and carry out the required activity through the communication platform link. While in this mode, AT+i commands are supported to monitor and control the process when needed. All other AT+i commands return with an I/BUSY response.

3.2.3.4 Direct Modem Firmware Update Mode

In a modem configuration, issuing an AT+iFU command enters this mode. iChip CO561AD-S monitors the modem for an incoming call by detecting the ‘RING’ response. When called, iChip CO561AD-S instructs the modem to answer the call and assumes a YMODEM session to receive a file containing a firmware update. The incoming file contents are downloaded and authenticated. If the new firmware image checks out the existing firmware is replaced in the on-chip flash memory and iChip CO561AD-S is reinitialized.

3.2.4 Host Serial Connection

iChip supports a full-duplex, TTL-level serial communications link with the host processor. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, and DTR lines, is supported.

3.2.5 Serial Connection to Dial-up Modem

iChip CO561AD-S supports a full-duplex, TTL-level serial communications link with the modem device. Full EIA-232-D hardware flow control, including Tx, Rx, CTS, RTS, and DTR lines, is supported.

3.2.6 Local Bus Connection to Ethernet Controller

iChip LAN CO561AD-L directly supports a Crystal LAN CS8900A IEEE 802.3 Ethernet Controller in 16-bit memory mode. Interrupt and DMA request are directly connected to dedicated inputs. A small PLD or discrete logic is required to generate the MEMRD#/MEMWE# and IORD#/IOWR# signals that form iChip's RD# and WR# signals to simulate memory, IO and DMA accesses. See section "6.4 Reference Design for Embedded LAN Using iChip LAN CO561AD-L".

3.2.7 Hardware and Software Flow Control

Hardware flow control is supported between the host CPU and iChip. Hardware flow control is also provided between the iChip CO561AD-S and the modem. Flow control is programmed via the AT+iFLW command. The default flow control methods are set to Wait/Continue software flow control between iChip and host, and no flow control between iChip and modem.

The hardware flow control method frees the host CPU from monitoring and handling the software flow control. The host can program iChip to either use hardware flow control or to use Wait/Continue software flow control between the iChip and the host CPU. The flow control mechanism is based on the RTS/CTS signals.

Flow control between iChip and the Modem can be individually programmed to hardware flow control or no flow control.

The Crystal Ethernet Controller CS8900A provides sufficient buffers to support the packet flow control on TCP/IP level between iChip LAN and the Ethernet LAN.

4 Hardware Interface

iChip CO561AD-S interfaces between a host CPU and a modem.

4.1 Host Interface

The host interface is a serial DTE interface. iChip can change the rate and format of the data sent and received from the host CPU. Speeds of 2400, 4800, 7200, 9600, 19200, 38400, and 57600 bps (iChip LAN up to 230,000 bps) are supported in the following data formats:

Parity	Data Length (No. of Bits)	No. of Stop Bits	Character Length (No. of Bits)
None	8	1	10

Table 4-1 Host Data Format

4.2 Serial Modem Interface

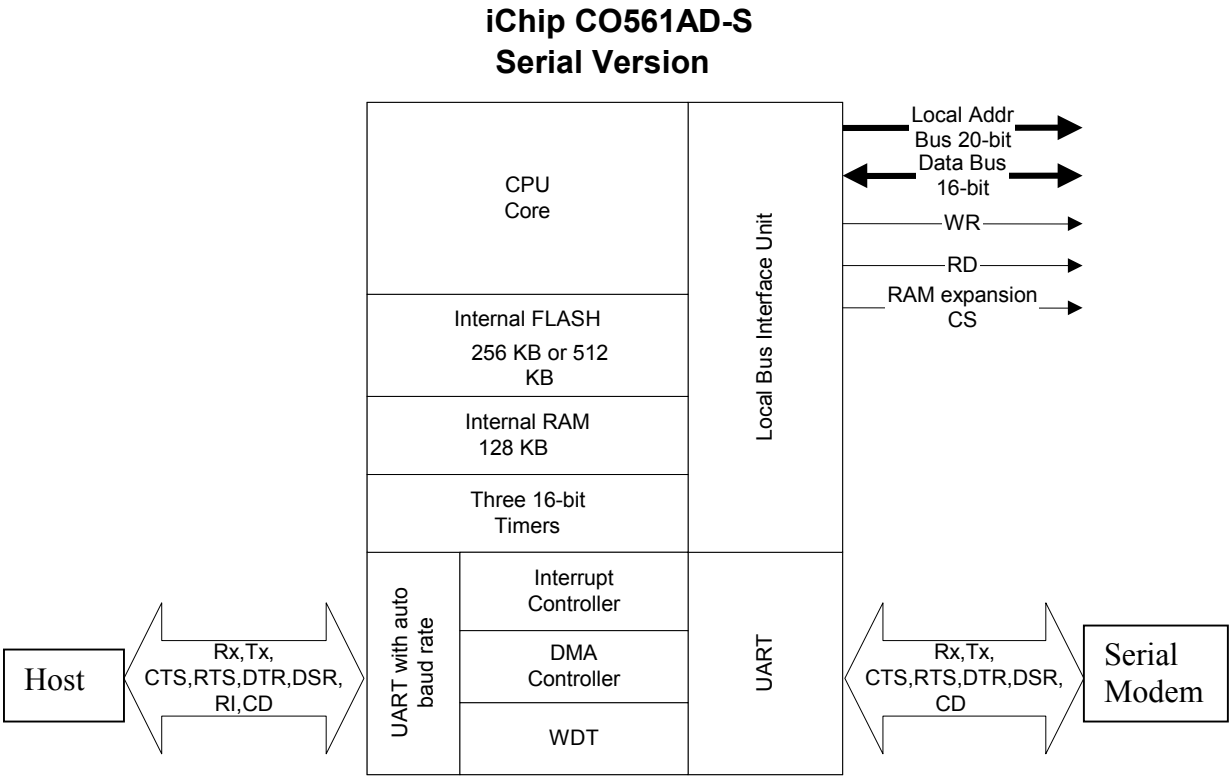


Figure 4-1 iChip CO561AD-S with a Serial Modem Interface

In addition to a serial modem interface, iChip supports a memory expansion option, which is used to increase the store-and-forward buffer.

3.3 Ethernet Controller Interface

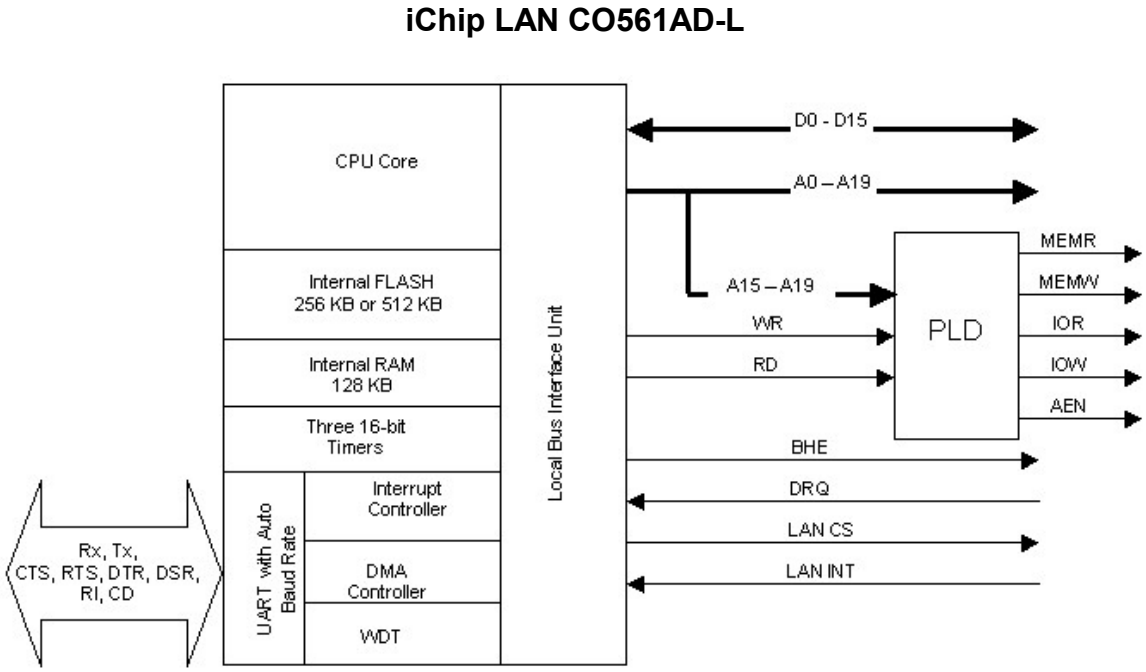


Figure 4-2 iChip LAN with an Ethernet Controller Interface

iChip and iChip LAN support a memory expansion option, which is used to increase the store-and-forward buffer.

5 Pin Descriptions

5.1 iChip CO561AD-S Pin Assignments

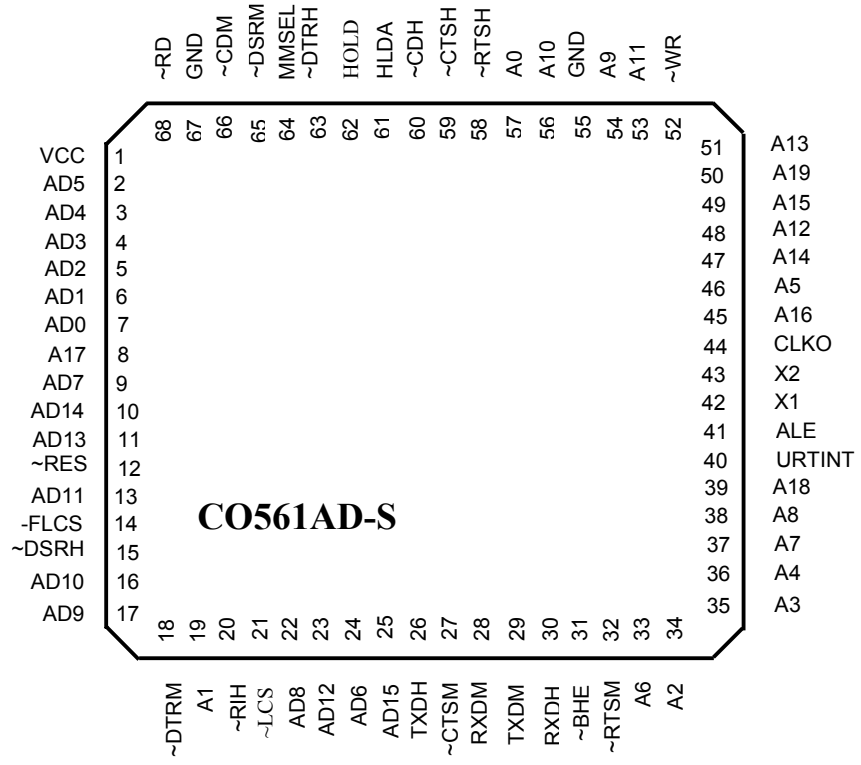


Figure 5-1 PLCC68 Package for iChip CO561AD-S Serial Version

5.2 iChip LAN Pin Assignments

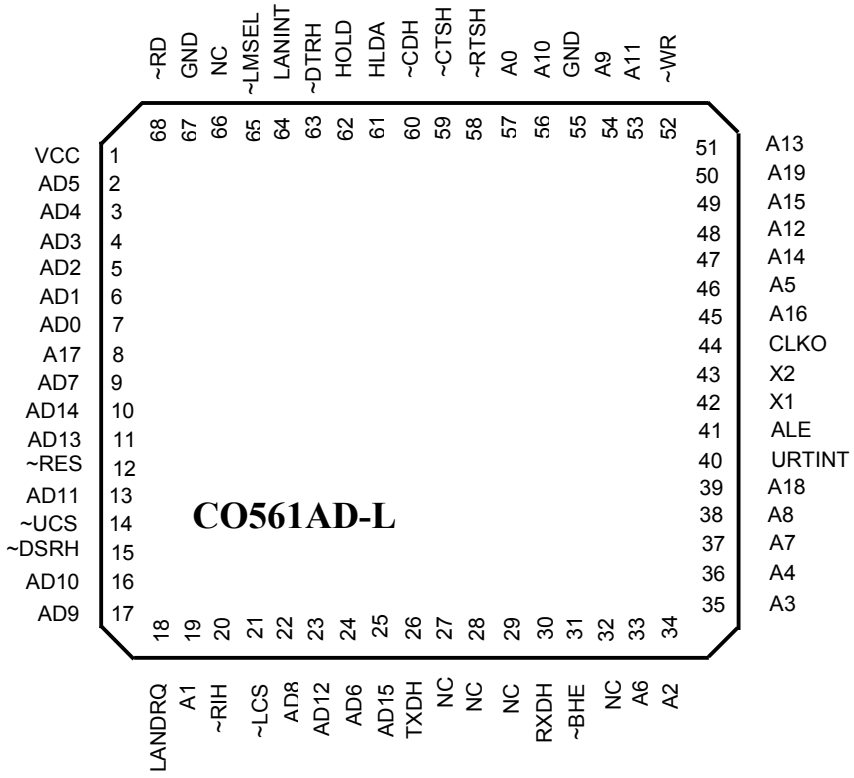


Figure 5-2 PLCC68 Package for iChip LAN CO561AD-L Serial Version

5.3 iChip Pin Functional Descriptions

5.3.1 Local Bus Signals

A19–A0
Address Bus (output, three-state, synchronous)
These pins supply non-multiplexed memory or I/O addresses to the system one half of a CLKO period earlier than the multiplexed address and data bus AD15–AD0. During a bus hold or reset condition, the address bus is in a high-impedance state.

AD15–AD0
Address and Data Bus (input/output, three-state, synchronous, level-sensitive)
AD15–AD0—These time-multiplexed pins supply memory or I/O addresses and data to the system. This bus can supply an address to the system during the first period of a bus cycle. It supplies data to the system during the remaining periods of that cycle. When ~WR is deasserted, these pins are three-stated.

ALE
Address Latch Enable (output, synchronous)
This pin indicates to the system that an address appears on the address and data bus (AD15–AD0). The address is guaranteed to be valid on the trailing edge of ALE. This pin is not three-stated during a bus hold or reset.

~BHE
Bus High Enable (three-state, output, synchronous)
During a memory access, this pin and the least-significant address bit (AD0 or A0) indicate to the system, which bytes of the data bus (upper, lower, or both) participate in a bus cycle. The ~BHE and AD0 pins are encoded as shown in the table below.

~BHE	AD0	Type of bus cycle
0	0	Word Transfer
1	0	Even Byte Transfer
0	1	Odd Byte Transfer
1	1	N/A

Table 5-1 Data Byte Encoding

BHE floats during bus hold and reset. During refresh cycles, the A bus and the AD bus are not guaranteed to provide the same address during the address phase of the AD bus cycle. For this reason, the A0 signal cannot be used in place of the AD0 signal to determine refresh cycles.

CLKO
Clock Output.
This pin Supplies the internal clock to the system. CLKO remains active during RESET.

~UCS
Upper Chip Select (output, synchronous)
This pin indicates to the system that that a memory access is in progress to the Flash memory.
Normally this pin should be Open.

HOLD
Bus Hold Request (input, synchronous, level sensitive)
This pin indicates to the iChip that an external bus master needs control of the local bus .
Normally this pin should connect to GND.

HLDA
Bus Hold Acknowledge (output , synchronous, level sensitive)
This pin asserted High to indicate to an external bus master that the iChip has release control of local bus. Normally this pin should be Open.

~LCS
Low memory Ram Chip Select (output, synchronous)
This pin indicates to the system that that a memory access is in progress to the Static Ram memory. Normally this pin should be Open.

~RD
Read Strobe (output, synchronous, three-state)
This pin indicates to the system that the iChip is performing a memory or I/O read cycle. ~RD is guaranteed to not be asserted before the address and data bus is floated during the address-to-data transition. ~RD floats during a bus hold condition.

~RES
Reset (input, asynchronous, level-sensitive)
This pin requires the iChip to perform a reset.
When ~RES is asserted, the iChip immediately terminates its present activity and clears its internal logic.
~RES must be held Low for at least 1 ms.
~RES can be asserted asynchronously to CLKO because ~RES is synchronized internally. For proper initialization, VCC must be within specifications, and CLKO must be stable for more than four CLKO periods during which RES is asserted. The iChip begins fetching instructions approximately 6.5 CLKO periods after ~RES is de-asserted. This input is provided with a Schmidt trigger to facilitate power-on RES generation via an RC network.

URTINT
Uart Interrupt (input , asynchronous)
This pin for debugging only . It must be pull up to Vcc with resistor of 4.7K.

~WR

Write Strobe (output, synchronous)

This pin indicates to the system that the data on the bus is to be written to a memory or I/O device. ~WR floats during reset condition.

X1

Crystal Input (input)

This pin and the X2 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit. To provide the iChip with an external clock source, connect the source to the X1 pin and leave the X2 pin unconnected.

X2

Crystal Output (output)

This pin and the X1 pin provide connections for a fundamental mode or third-overtone, parallel-resonant crystal used by the internal oscillator circuit. To provide the iChip with an external clock source, leave the X2 pin unconnected and connect the source to the X1 pin.

Selecting a Crystal

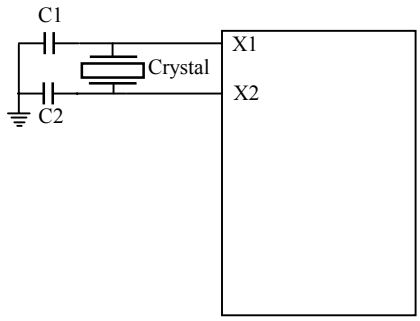


Figure 5-3 Selecting a Crystal

The characteristics of the built-in inverting amplifier set limits on the following parameters for crystals:

Crystal first overtone frequency ..... 18.432 MHz
ESR (Equivalent Series Resistance) ..... 40 Ω max
Drive Level .....…. 1 mW max

The recommended range of values for C 1 and C 2 are as follows:

C 1 ..... 15 pF ± 20%
C 2 ..... 22 pF ± 20%

The specific values for C1 and C2 must be determined by the designer and are dependent on the characteristics of the chosen crystal and board design.

GND

Ground

Ground pins connect the iChip to the system ground.

VCC
Power Supply (input)
These pins supply power (+5 V) to the iChip.

5.3.2 Host Interface Signals

TXDH
Transmit Data Host (output, asynchronous)
This pin supplies asynchronous serial transmit data to the system from serial port.

RXDH
Receive Data Host (input, asynchronous)
This pin supplies asynchronous serial receive data from the system to asynchronous serial port.

~CTSH
Clear-to-Send Host (input, asynchronous)
This pin provides the Clear to Send signal for asynchronous serial port when the hardware flow control is enabled for the port. The ~CTSH signal gates the transmission of data from the associated serial port transmit register. When ~CTSH is asserted, the transmitter begins transmission of a frame of data, if any is available. If ~CTSH is de-asserted, the transmitter holds the data in the serial port transmit register. The value of ~CTSH is checked only at the beginning of the transmission of the frame.

~RTSH
Ready-to-Send Host (output, asynchronous)
This pin provides the Ready to Send signal for asynchronous serial port when the hardware flow control is enabled for the port. The ~RTSH signal is asserted when the associated serial port transmit register contains data which has not been transmitted.

~DSRH
Data Set Ready Host (input, synchronous)
When flow control is enabled, this pin is Data Set Ready Input.

~DTRH
Data Terminal Ready Host (output, synchronous)
When flow control is enabled, this pin operates as Data Terminal Ready Output.

~CDH
Carrier Detect Host (output, synchronous)
This pin indicates to the system that a carrier was detected by the communication device (modem).

~RIH
Ring Indicator Host (output, synchronous)
This pin indicates to the system that a Ring signal was detected by communication device (modem).

5.3.3 iChip Serial Modem Signals

RXDM
Receive Data Modem (input, asynchronous)
This pin supplies asynchronous serial receive data from modem to asynchronous serial port.

TXDM
Transmit Data Modem (output, asynchronous)
This pin supplies asynchronous serial transmit data to modem from serial port.

~CDM
Carrier Detect Modem (input, asynchronous, internal pull-up)
When configured in Serial-to-Serial mode, this pin is Carrier Detect input.

~DSRM
Data Set Ready Modem (input, asynchronous).
When Flow control is enabled, this pin is Data Set Ready input.

~RTSM
Ready-to-Send Modem (output, asynchronous)
This pin provides the Ready to Send signal for asynchronous serial port when the hardware flow control is enabled for the port. The ~RTSM signal is asserted when the associated serial port transmit register contains data that has not been transmitted.

~CTSM
Clear-to-Send Modem (input, asynchronous)
Enable-Receiver-Request M (input, asynchronous)
This pin provides the Clear to Send signal for asynchronous serial port when flow control option is enabled. The ~CTSM signal gates the transmission of data from the associated serial port transmit register. When ~CTSM is asserted, the transmitter begins transmission of a frame of data, if any is available. If ~CTSM is de-asserted, the transmitter holds the data in the serial port transmit register. The value of ~CTSM is checked only at the beginning of the transmission of the frame.

~DTRM
Data Terminal Ready Modem(Output, asynchronous)
When flow control is enabled, this pin is Channel Data Terminal Ready Output.

MMSEL
Modem Mode Input (input, asynchronous) (For modem application only)
When this pin is held Low during power up, for at least 5 seconds, the iChip will automatically enter firmware update mode. During a firmware update procedure, when an external modem dials to the iChip, pulling this pin down to Low will cause the iChip to immediately answer the call and begin the update session. When this pin is held Low during power up for less than 5 seconds, it forces the iChip into auto baud rate detection.

5.4 iChip LAN Signals

LANINT
LAN Interrupt (active high input)
This pin inputs the interrupt from the Ethernet controller.

LANDRQ
LAN DMA Request (active high input)
This pin inputs the DMA request from the Ethernet controller.

LMSEL
LAN Mode Input (input, asynchronous) (For LAN application only)
When this pin is held Low during power up, for at least 5 seconds, the iChip will automatically enter firmware update mode.

6 Electrical/Mechanical Specifications

6.1 Environmental Specifications

6.1.1 Absolute Maximum Ratings

6.1.1.1 3.3 Volt Version

Parameter	Rating
Voltage at any pin with respect to ground	-1.0 to VCC + 0.5 Volts
Operating temperature	0°C to 70°C (32 to 158°F)
Storage temperature	-60°C to 120°C (–76 to 248°F)
Soldering temperature (max. 10 sec.)	220°C (428°F)
Package dissipation	1.5 Watts

Table 6-1 Environmental Specifications 3.3V Version

6.1.1.2 5 Volt Version

Parameter	Rating
Voltage at any pin with respect to ground	-1.0 to +7.0 Volts
Operating temperature	0°C to 70°C (32 to 158°F)
Storage temperature	-60°C to 120°C (–76 to 248°F)
Soldering temperature (max. 10 sec.)	220°C (428°F)
Package dissipation	1.5 Watts

Table 6-2 Environmental Specifications 5V Version

6.1.2 DC Operating Characteristics

6.1.2.1 3.3 Volt Version

Parameter	Min	Typical	Max	Units
DC Supply	3.0	3.3	3.6	Volts
High-level Input	2.0		VCC+0.5	Volts
Low-level Input	-0.5		0.8	Volts
High-level Output[1]	2.4		VCC	Volts
Low-level Output			0.45	Volts
Input leakage current			+/- 10	µA
Power supply current (Operating Mode)[2]		30	60	MA
Power supply current (Power Save Mode)		0.25	0.5	MA
Input capacitance			20	PF

Notes: [1] I_{OL} = 2mA
[2] 20 MHz clock

Table 6-3 DC Operating Characteristics 3.3V Version

6.1.2.2 5 Volt Version

Parameter	Min	Typical	Max	Units
DC Supply	4.75	5.0	5.25	Volts
High-level Input	2.0		VCC+0.5	Volts
Low-level Input	-0.5		0.8	Volts
High-level Output[1]	2.4		VCC	Volts
Low-level Output			0.45	Volts
Input leakage current			+/- 10	µA
Power supply current (Operating Mode)[2]		160	250	mA
Power supply current (Power Save Mode)		10		mA
Input capacitance			20	pF

Notes: [1] I_{OL} = 2mA
[2] 20 MHz clock

Table 6-4 DC Operating Characteristics 5V Version

6.2 Interface Timing and Waveforms

6.2.1 Local Bus Read Cycle

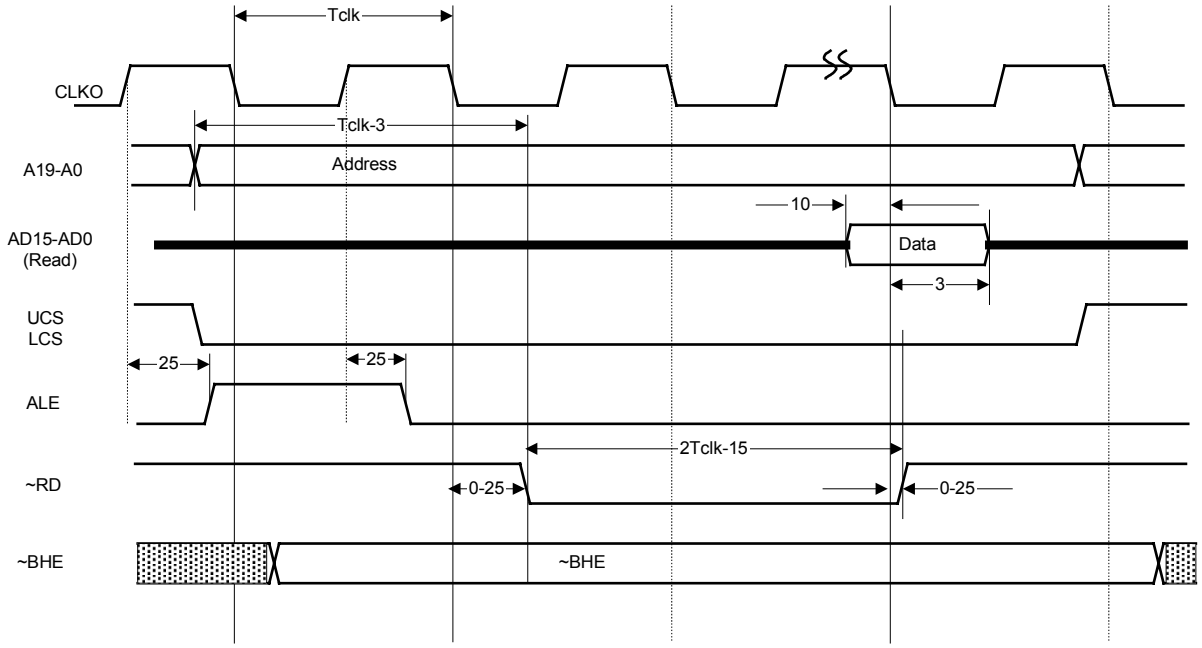


Figure 6-1 Local Bus Read Cycle

6.2.2 Local Bus Write Cycle

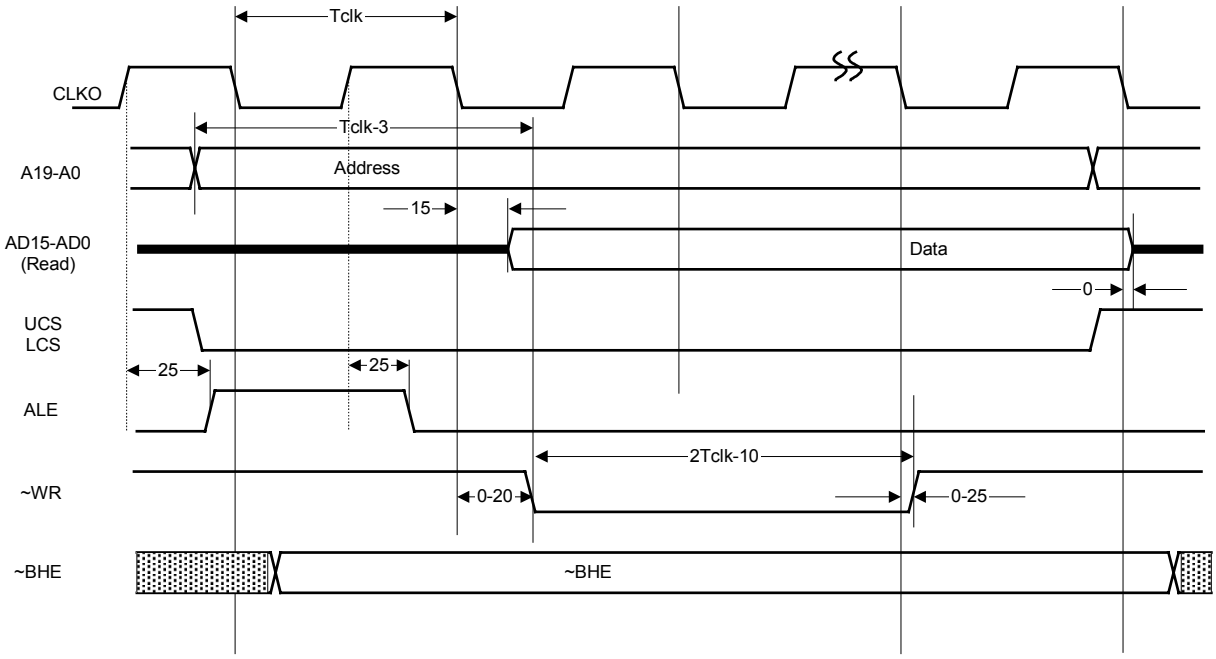
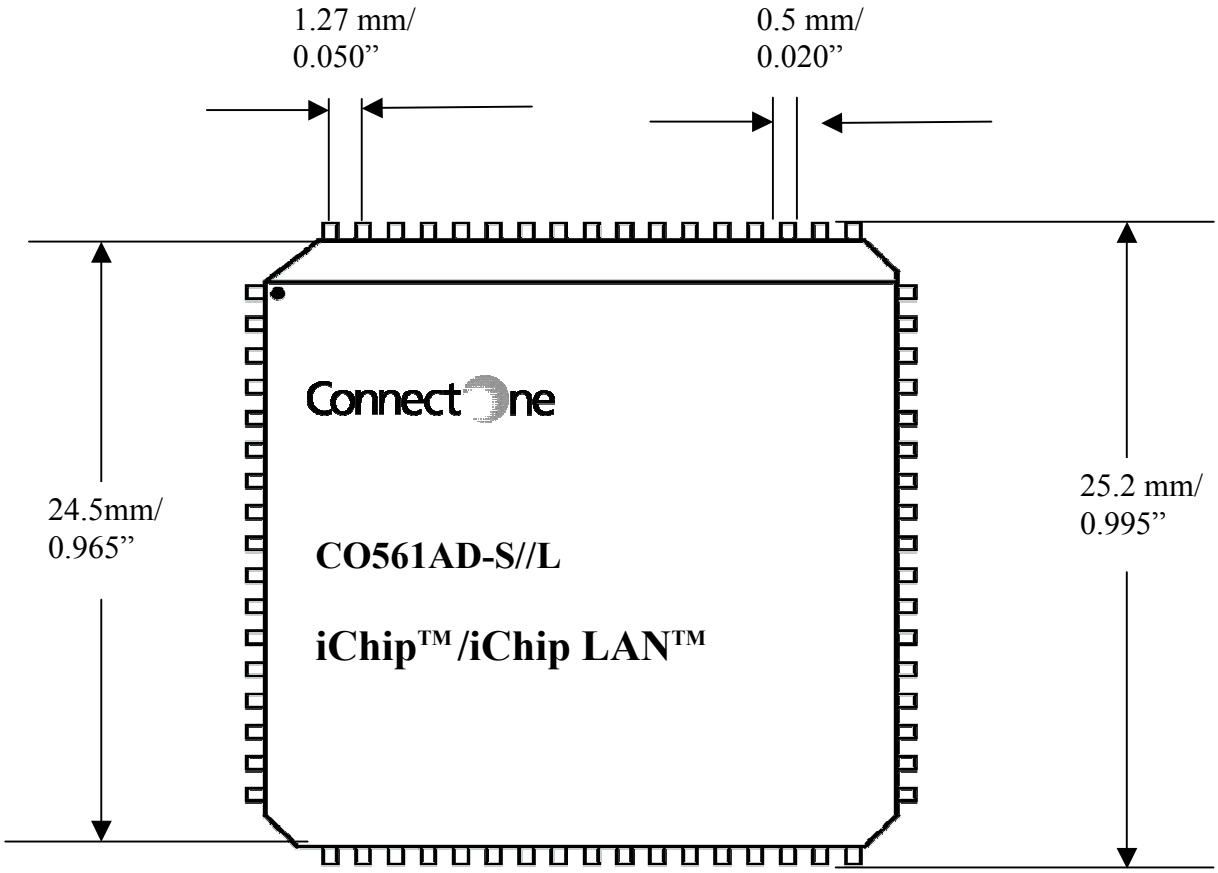


Figure 6-2 Local Bus Write Cycle

6.3 Mechanical Dimensions



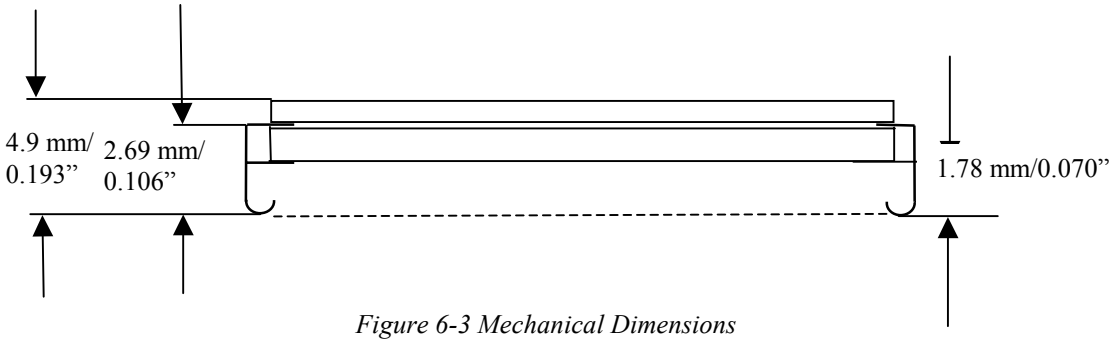


Figure 6-3 Mechanical Dimensions

7 iChip Designs

7.1 General Hardware Architecture

7.1.1 Serial Modem Environment

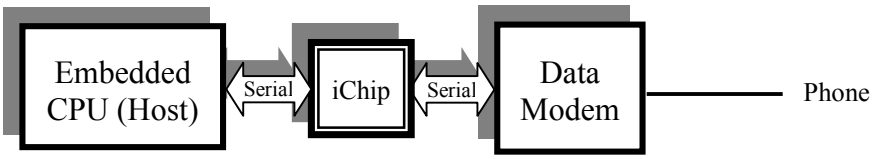


Figure 7-1 Serial Modem Environment

7.1.2 Ethernet Controller Environment

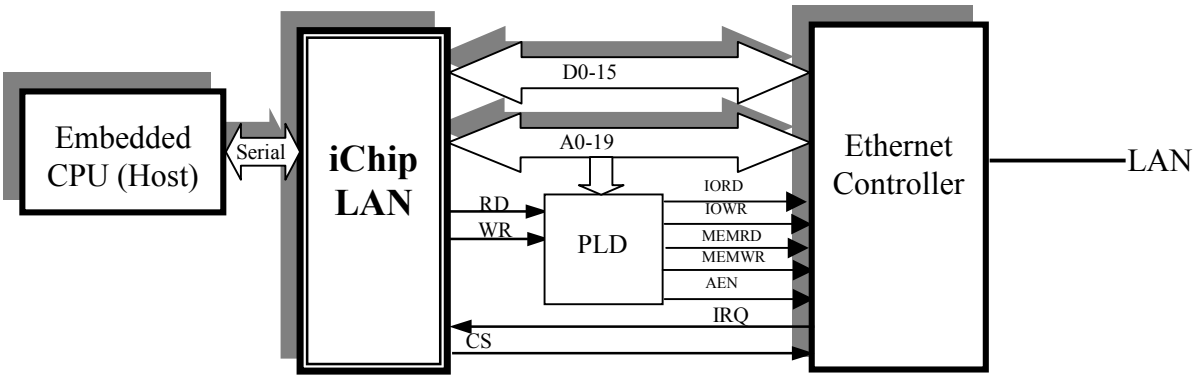


Figure 7-2 Ethernet Controller Environment

7.2 Reference Design for Embedded iModem Using CO561AD-S

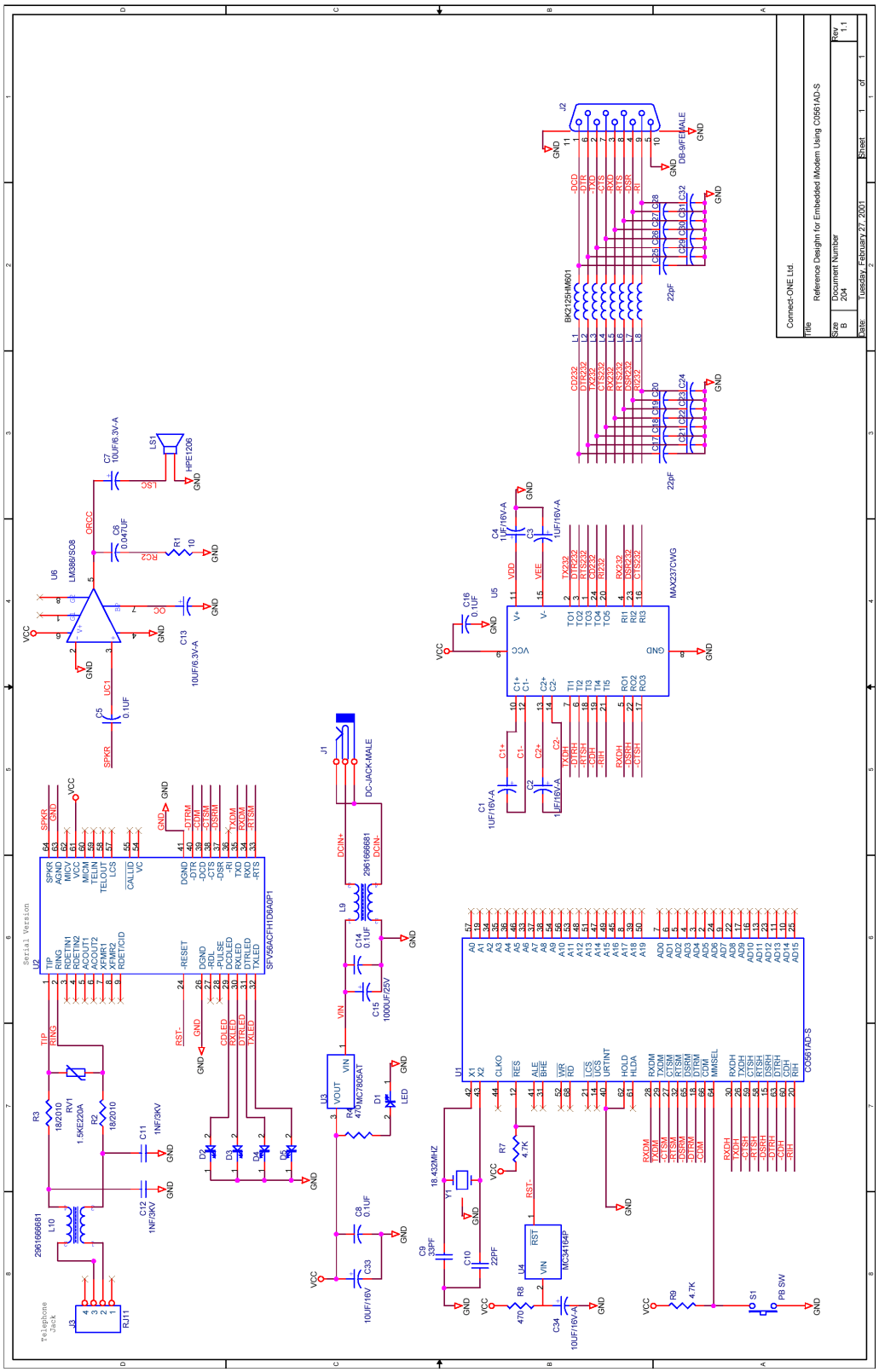


Figure 7-3 Reference Design for Embedded iModem Using CO561AD-S

7.3 Bill of Materials for CO561AD-S Reference Design

#	Qty	Reference Designator	P/N, Description	Manufacturer
1.	4	C1,C2,C3,C4	1UF/16V, Tantalum	
2.	4	C5,C8,C14,C16	0.1UF, Ceramic	
3.	1	C6	0.047UF Ceramic	
4.	2	C7,C13	10UF/6.3V	
5.	1	C9	33PF, Ceramic	
6.	1	C10	22PF, Ceramic	
7.	2	C11,C12	1NF/3KV	
8.	1	C15	1000UF/25V	
9.	16	C17,C18,C19,C20,C21,C22,	56pF, Ceramic	
10.		C23,C24,C25,C26,C27,C28,		
11.		C29,C30,C31,C32		
12.	2	C33,C34	10UF/16V	
13.	5	D1,D2,D3,D4,D5	LED, 10mA	
14.	1	J1	DC-JACK-MALE	
15.	1	J2	DB-9/FEMALE	
16.	1	J3	RJ11	
17.	1	LS1	HPE-1206, Speaker 50 Ω	
18.	8	L1,L2,L3,L4,L5,L6,L7,L8	BK2125HS601	Taiyoyuden Co. Ltd.
19.	2	L9,L10	2961666681	Fair Rite Inc.
20.	1	RV1	1.5KE220A	
21.	1	R1	10, 0.125W	
22.	2	R2,R3	18R, 0.75W	
23.	3	R7,R9,R10	4.7K, 0.125W	
24.	2	R4,R8	470, 0.125W	
25.	1	S1	PB Switch	
26.	1	U1	CO561AD-S	Connect One Ltd.
27.	1	U2	SF336D/SP-H1-D5	Conexant
28.	1	U3	7805	
29.	1	U4	MC34164P	On Semiconductor
30.	1	U5	MAX237CWG	Maxim Integrated Products
31.	1	U6	LM386D	National Semiconductor
32.	1	Y1	18.432MHz, parallel resonance, 100ppm	

Table 7-1 Bill of Materials for CO561AD-S Reference Design

Item #27 SF**XX**D/SP-H1-**YY**, Conexant Socket Modem, can be ordered in the following configurations:
XX = 56 (56,000 bps), 336 (33,600 bps), 144 (14,400 bps)
YY = D5: (U.S), DF (France), DG (Germany), DT (Italy), DE (Spain), DJ (Japan), DC (CTR21: CTR21 countries include Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Norway, Portugal, Spain, Sweden, Switzerland, The Netherlands, and UK. The country is selected by issuing the AT*NC70 command.)

7.4 Reference Design for Embedded iLAN Using CO561AD-L

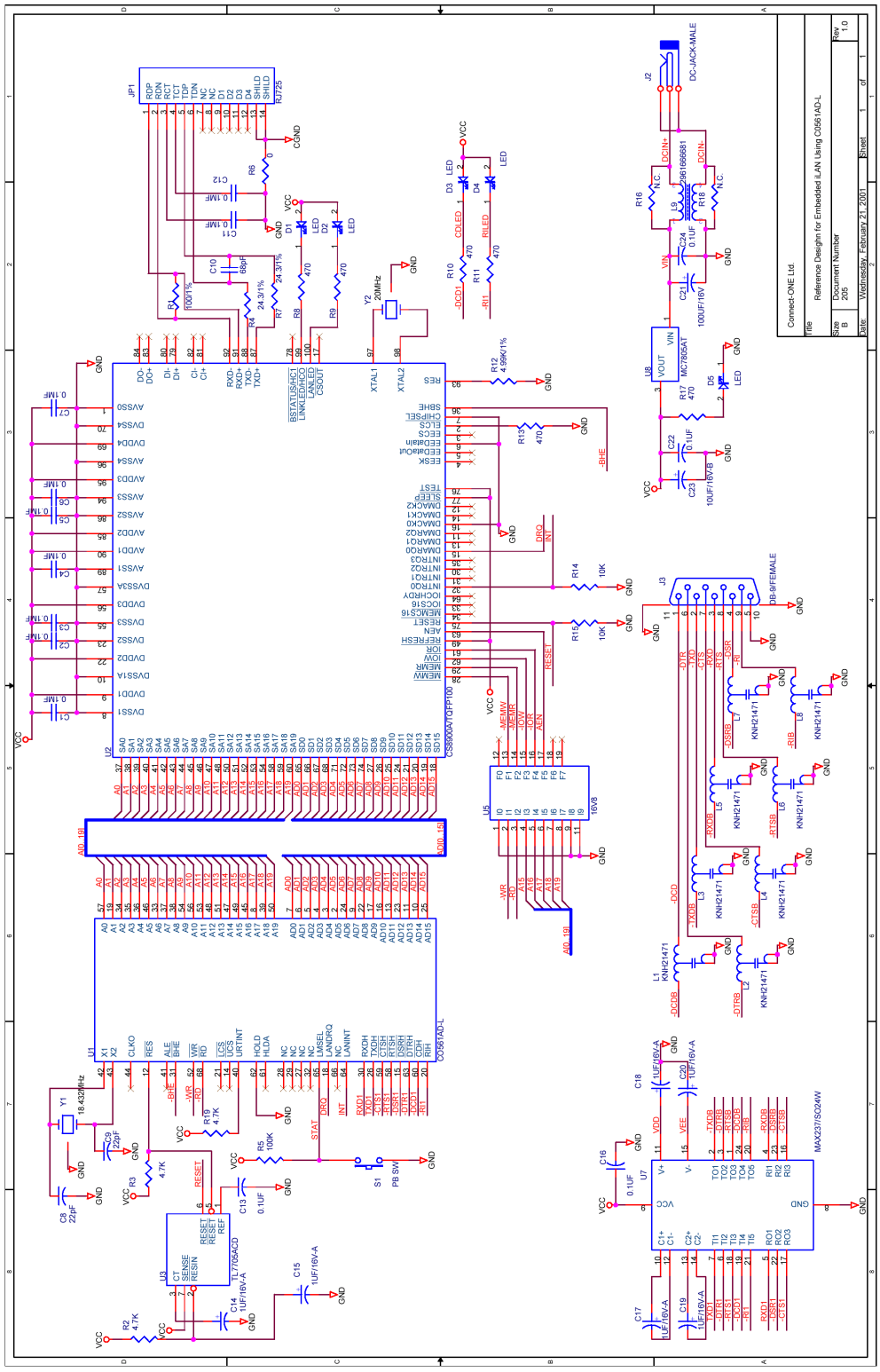


Figure 7-4 Reference Design for Embedded iLAN Using CO561AD-L

7.5 Bill of Materials for CO561AD-L Reference Design

#	Qty	Reference Designator	P/N, Description	Manufacturer
1	1	C10	68pF	
2	13	C1,C2,C3,C4,C5,C6,C7,C11,	0.1UF	
		C12,C13,C16,C22,C24		
3	6	C14,C15,C17,C18,C19,C20	1UF/16V-A	
4	1	C21	100UF/16V	
5	1	C23	10UF/16V-B	
6	2	C8,C9	22pF	
7	5	D1,D2,D3,D4,D5	LED	
8	1	JP1	RJ-725	Transpower
9	1	J2	DC-JACK-MALE	
10	1	J3	DB-9/FEMALE	
11	8	L1,L2,L3,L4,L5,L6,L7,L8	KNH21471	AVX Corporation
12	1	L9	2961666681	Fair Rite
13	1	R1	100/1%	
14	3	R2,R3,R19	4.7K	
15	2	R4,R7	24.3/1%	
16	1	R5	100K	
17	1	R6	0	
18	6	R8,R9,R10,R11,R13,R17	470	
19	1	R12	4.99K/1%	
20	2	R15,R14	10K	
21	1	S1	PB SW	
22	1	U1	CO561AD-L	Connect One Ltd.
23	1	U2	CS8900A	Crystal
24	1	U3	TL7705ACD	Texas Instruments
25	1	U5	PAL16V8	
26	1	U7	MAX237CWG	Maxim Integrated Products
27	1	U8	7805	
28	1	Y1	18.432MHz, parallel resonance, 100ppm	
29	1	Y2	20MHz, parallel resonance, 50ppm	

Table 7-2 Bill of Materials for CO561AD-L Reference Design

7.6 PLD Equations

```
--------------------------------------------------------------------
-- File name:           imdlnref.vhd
-- Designed by:         Leonid Epstein
-- Purpose:             iLAN board Control Logic.
-- The board memory map:
-- 0x00000 - 0x1ffff      - system SRAM
-- 0x20000 - 0x27fff      - LAN IO space (32KB)
--                                (default IO 0x300 so the first access s.b. to 0x20300)
-- 0x28000 - 0x2ffff      - LAN DMA access (32KB)
-- 0x38000 - 0x3ffff      - LAN memory space (32KB)
-- 0x80000 - 0xfffff      - System FLASH
--------------------------------------------------------------------

library IEEE;
use IEEE.std_logic_1164.all;

entity imdlnref is
   port (
    a          : in    std_logic_vector(19 downto 15);
    wr_n       : in    std_logic;
    rd_n       : in    std_logic;

    memwr_n    : out   std_logic;
    memrd_n    : out   std_logic;
    iowr_n     : out   std_logic;
    iord_n     : out   std_logic;
    aen        : out   std_logic
);

attribute   loc : string ;
attribute   loc  of wr_n      : signal is "P2" ;
attribute   loc  of rd_n      : signal is "P3" ;
attribute   loc  of a15       : signal is "P4" ;
attribute   loc  of a16       : signal is "P5" ;
attribute   loc  of a17       : signal is "P6" ;
attribute   loc  of a18       : signal is "P7" ;
attribute   loc  of a19       : signal is "P8" ;
attribute   loc  of memwr_n   : signal is "P13" ;
attribute   loc  of memrd_n   : signal is "P14" ;
attribute   loc  of iowr_n    : signal is "P15" ;
attribute   loc  of iord_n    : signal is "P16" ;
attribute   loc  of aen       : signal is "P17" ;

end imdlnref;

architecture behavioral of imdlnref is

signal  mem_access: std_logic;
signal  io_access:  std_logic;
signal  dma_access: std_logic;

begin

mem_access  <= '1' when a(19 downto 16) = "0011" and a(15) = '1'
               else '0';  -- 0x38000 - 0x3FFFF ;
io_access   <= '1' when a(19 downto 16) = "0010" and a(15) = '0'
               else '0';  -- 0x20000 - 0x27FFF ;
dma_access  <= '1' when a(19 downto 16) = "0010" and a(15) = '1'
               else '0';  -- 0x28000 - 0x2FFFF ;

memwr_n     <= wr_n when mem_access = '1' else '1';
memrd_n     <= rd_n when mem_access = '1' else '1';
iowr_n      <= wr_n when io_access = '1' or dma_access = '1' else '1';
iord_n      <= rd_n when io_access = '1' or dma_access = '1' else '1';
aen         <= '1' when dma_access = '1' else '0' ;

end behavioral;
```

8 Socket iChip™ Carrier Board

The Socket iChip™ Internet Controller, CO561AD-C, is the iChip CO561AD-S on a carrier board that is pin-compatible with Conexant SocketModem™.

8.1 Pin Assignments

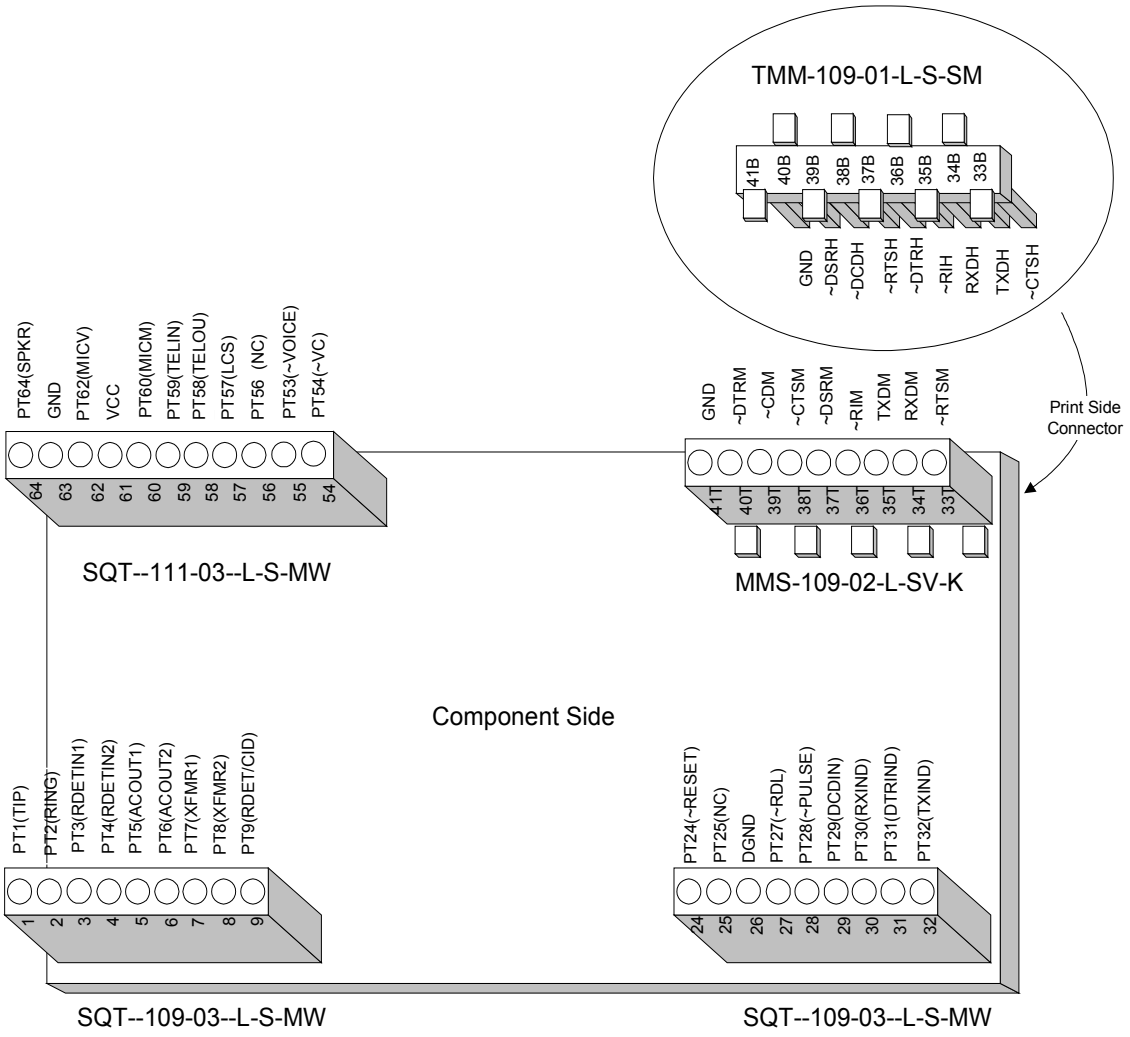


Figure 8-1 Carrier Board CO561AD-C Pinout

8.2 Pin Functional Descriptions

8.2.1 Socket Modem Interface Signals

PTx

Pass-Through connections.
The board provides pass-through connection between a motherboard and a socket modem mounted on top of the CO561AD-CT/R. Pins PT1 .. PT9 are dedicated for TNV signals. The CO561AD-CT/R board layout meets EN 60950:1992 +A1/A2:1993 +A3:1995 requirements for creepage distance and clearance. Signal names in brackets correspond to Conexant's' Socket modem data sheet.

VCC
+5VDC

DGND
Digital Ground.
Connect to Digital Ground on the interface circuit.

~RESET
Modem and iChip Reset.
The Active Low ~RESET input resets both the iChip and a SocketModem logic and returns the AT command set to the original factory default values and to "stored values" in NVRAM.

AGND

Analog Ground.
Connect to Analog Ground on the interface circuit. Note that AGND is connected to DGND on the SocketModem.

RXDM,
Received Data (TTL Active Low, EIA-232 Active High), Input.
This pin supplies asynchronous serial receive data from Socket modem to asynchronous serial port .

TXDM,
Transmitted Data Modem (TTL Active Low, EIA-232 Active High), Output.
This pin supplies asynchronous serial transmit data to Socket modem from serial port .

~CTSM,
Clear To Send Modem (TTL Active Low, EIA-232 Active High), Input
This pin provides the Clear to Send signal for asynchronous serial port when flow control option is enabled. The ~CTSM signal gates the transmission of data from the associated serial port transmit register. When ~CTSM is asserted, the transmitter begins transmission of a frame of data, if any is available. If ~CTSM is de-asserted, the

transmitter holds the data in the serial port transmit register. The value of ~CTSM is checked only at the beginning of the transmission of the frame.

~RTSM,
Ready To Send Modem (TTL Active Low, EIA-232 Active High),Output
This pin provides the Ready to Send signal for asynchronous serial port when the hardware flow control is enabled for the port. The ~RTSM signal is asserted when the associated serial port transmit register contains data that has not been transmitted.

~DTRM,
Data Terminal Ready Modem (TTL Active Low, EIA-232 Active High), Output.
When flow control is enabled, this pin is Channel Data Terminal Ready Output.

~DSRM,
Data Set Ready Modem (TTL Active Low, EIA-232 Active High), Input.
When Flow control is enabled, this pin is Data Set Ready input.

~RIM,
Ring Indicate Modem (TTL Active Low, EIA-232 Active High), Input.
~RIM input ON (low) indicates the presence of an ON segment of a ring signal on the telephone line (This signal is ignored by the socket iChip).

~CDM,
Carrier Detect Modem (TTL Active Low, EIA-232 Active High), Input.
This pin is the Carrier Detect Input from the modem.

8.2.2 Host Interface Signals

CO561AD-CT/R Interfaces to a Host CPU via asynchronous serial interface with TTL (T) or EIA-232 (R) signal levels.

~ TXDH/TXD232
Transmit Data Host (output, asynchronous)
This pin supplies asynchronous serial transmit data to the system from serial port.

~RXDH/RXD232
Receive Data Host (input, asynchronous)
This pin supplies asynchronous serial receive data from the system to asynchronous serial port.

~CTSH/CTS232
Clear-to-Send Host (input, asynchronous)
This pin provides the Clear to Send signal for asynchronous serial port 1 when the hardware flow control is enabled for the port. The ~CTSH signal gates the transmission of data from the associated serial port transmit register. When ~CTSH is asserted, the transmitter begins transmission of a frame of data, if any is available. If ~CTSH is de-asserted, the transmitter holds the data in the serial port transmit register. The value of ~CTSH is checked only at the beginning of the transmission of the frame.

~RTSH/RTS232
Ready-to-Send Host (output, asynchronous)
This pin provides the Ready to Send signal for asynchronous serial port when the hardware flow control is enabled for the port. The ~RTSH signal is asserted when the associated serial port transmit register contains data which has not been transmitted.

~DSRH/DSR232
Data Set Ready Host (input, synchronous)
When flow control is enabled, this pin is Data Set Ready Input

~DTRH/DTR232
Data Terminal Ready Host (input, synchronous)
When flow control is enabled, this pin operates as Data Terminal Ready Output

~CDH/CD232
Carrier Detect Host (output, synchronous)
This pin indicates to the system that carrier was detected by communication device (modem).

~RIH/RI232
Ring Indicator Host (output, synchronous)
This pin indicates to the system that Ring signal was detected by communication device (modem).

8.3 Socket iChip™ Package Dimensions

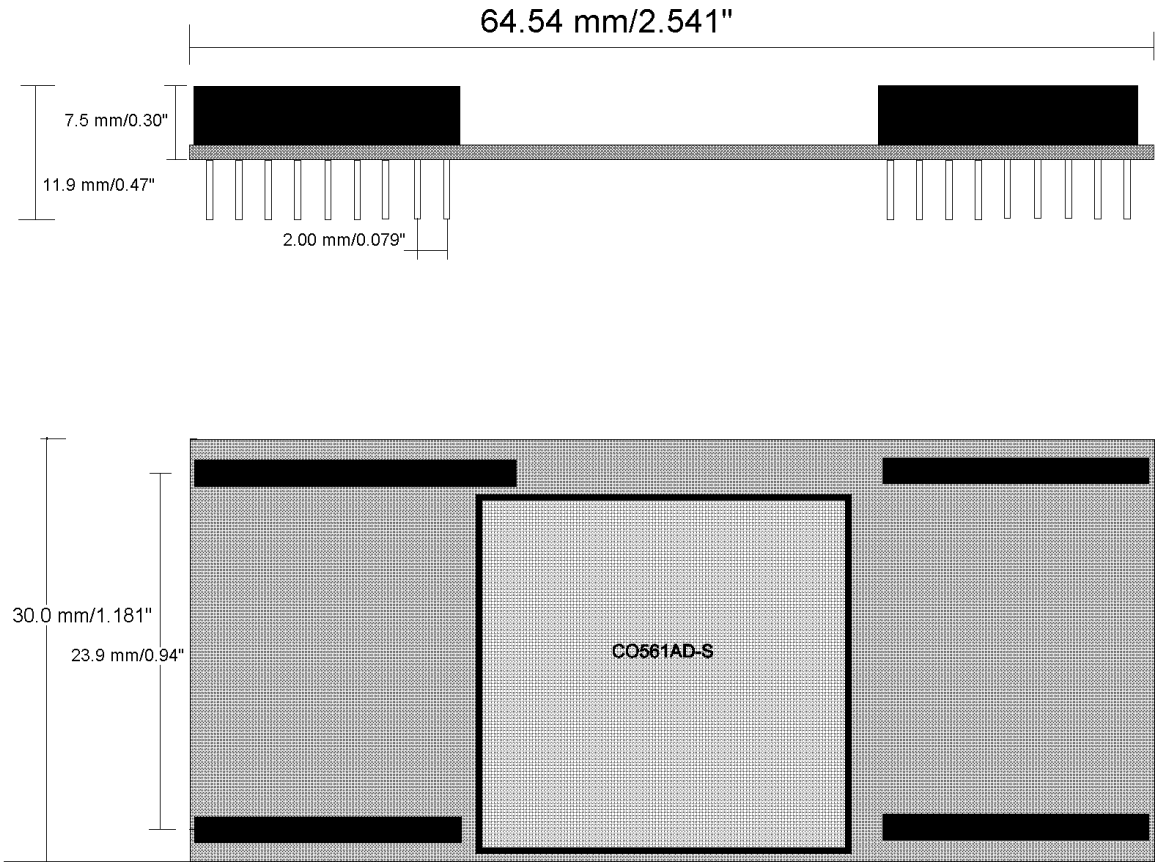


Figure 8-2 Socket iChip Package Dimensions

8.4 Reference Design for CO561AD-C Based Modem

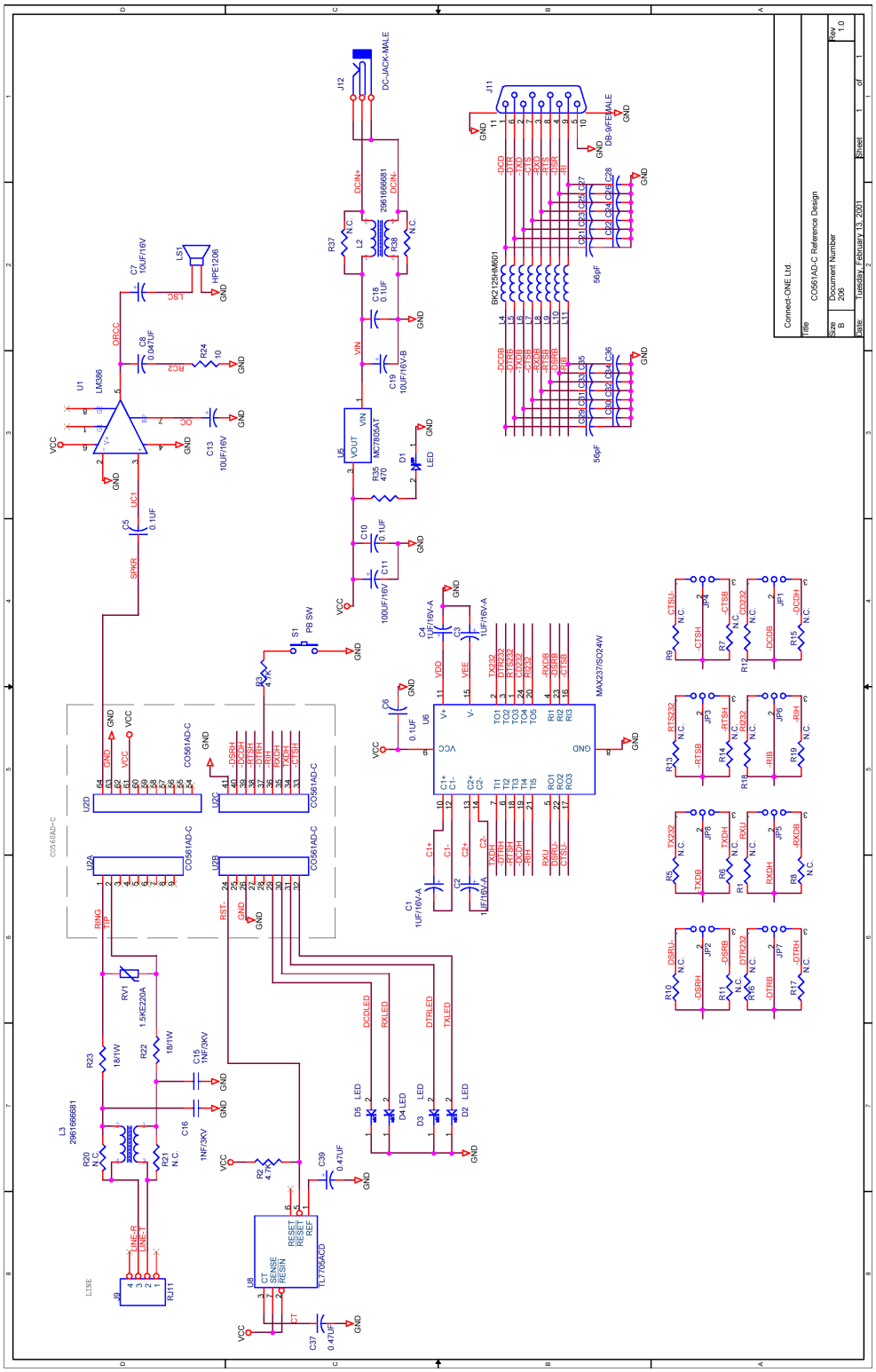


Figure 8-3 Reference Design for CO561AD-C Based Modem

8.5 Bill of Materials for CO561AD-C Reference Design

#	Qty	Reference Designator	P/N, Description	Manufacturer
1.	4	C1,C2,C3,C4	1UF/16V, Tantalum	
2.	1	C8	0.047UF	
3.	4	C6,C10,C18,C5	0.1UF, Ceramic	
4.	2	C19,C13,C7	10UF/16V	
5.	2	C15,C16	1NF/3KV	
6.	1	C11	100UF/16V	
7.	16	C21,C22,C23,C24,C25	56Pf, Ceramic	
8.		,C26,C27,C28,C29,C30		
9.		,C31,C32,C33,C34,C35,C36		
10.	2	C37,C39	0.47UF CERAMIC	
11.	5	D1,D2,D3,D4,D5	LED	
12.	1	J12	DC-JACK-MALE	
13.	1	J11	DB-9/FEMALE	
14.	1	J9	RJ11	
15.	2	L2,L3	2961666681	Fair Rite Inc.
16.	8	L4,L5,L6,L7,L8,L9,L10,L11	BK2125HS601	Taiyoyuden Co. Ltd.
17.	1	RV1	1.5KE220A	
18.	2	R22,R23	18R,1W	
19.	1	R24	10R	
20.	2	R2,R3	4.7K	
21.	2	R35	470	
22.	1	S1	PB Switch	
23.	1	U1	LM386	National Semiconductor
24.	1	U2	CO561AD-C	Connect One Ltd.
25.	1	U5	7805	
26.	1	U8	TL7705ACD	Texas Instruments
27.	1	U6	MAX237CWG	Maxim Integrated Products
28.	1	LS1	HPE-1206, Speaker 50 Ω	

Table 7-1 Bill of Materials for CO561AD-C Reference Design

9 PCB Design and Layout Considerations

9.1 Design Consideration

Good engineering practices must be adhered to when designing a printed circuit board (PCB) containing the SocketModem module. Suppression of noise is essential to the proper operation and performance of the modem itself and for surrounding equipment.

Two aspects of noise in an OEM board design containing the Conexant SocketModem module must be considered: on-board/off-board generated noise that can affect analog signal levels and analog-to-digital conversion (ADC)/digital-to-analog conversion (DAC), and on-board generated noise that can radiate off-board.

Both on-board and off-board generated noise that is coupled on-board can affect interfacing signal levels and quality, especially in low level analog signals. Of particular concern is noise in frequency ranges affecting modem performance.
On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met for use in specific environments.

Proper PC board layout (component placement, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to attain EMI certification.

9.2 PC Board Layout Guidelines

1. In a 2-layer design, all unused space around and under components should be filled with copper connected to the board ground on both sides of the board, and connected in such a manner as to avoid small islands. Isolated islands should be avoided by connecting all grounds on the same side at several points and to the ground plane on the opposite side through the board at several points. In a modem design, connect the SocketModem DGND and AGND pins to the ground plane.

2. In a 4-layer design, provide an adequate ground plane covering the entire board. In a modem design, SocketModem DGND and AGND pins are tied together on the SocketModem. Do not split analog and digital ground planes.

3. As a general rule, route digital signals on the component side of the PCB and the analog signals on the solder side. The sides may be reversed to match particular OEM requirements. Route the digital traces perpendicular to the analog traces to minimize signals cross coupling.

4. Route the modem signals to provide maximum isolation between noise sources and noise sensitive inputs. When layout requirements necessitate routing these

signals together, they should be separated by neutral signals. For the iChip LAN version, void power/ground plane as well as other digital signals between the CS8900A and the RJ45 module.

5. All power and ground traces should be at least 0.05 in. wide.

6. 0.1 UF ceramic capacitors should be placed as close as possible to the power pins. When internal power plane is used, the traces connecting between the power pins of the components and the vias should be kept short and to have bypass capacitor between the via and the pin.

7. In a modem design, TIP and RING signal traces are to be no closer than 0.062" from any other traces for U.S. applications. TIP and RING signal traces are to be no closer than 2.5mm (0.1”) from any other traces for European applications. 2.5mm spacing must be used if the host board is to support both U.S. and European Socket Modems. In multi layer design, power and ground planes should be cleared underneath the traces, which belong to the primary (TIP and RING) circuit. For an Ethernet design, route differential signals (RXD, TXD) close together as pairs. Try to avoid vias.

8. In a modem design, if the SocketModem is mounted flush with the host PCB, the host PCB should be clear of all traces directly underneath the SocketModem oscillator section. It is strongly suggested that the SocketModem be mounted at least 0.130 inch above the host board.

9.2.1 Electromagnetic Interference (EMI) Considerations

In a modem design, the following guidelines are offered to specifically help minimize EMI generation. Some of these guidelines are the same as, or similar to, the general guidelines but are mentioned again to reinforce their importance. In order to minimize the contribution of the SocketModem-based design to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

1. Keep traces carrying high frequency signals as short as possible.

2. Decouple power from ground with decoupling capacitors as close to the active components’ power pins as possible.

3. Eliminate ground loops, which are unexpected current return paths to the power source and ground.

4. Decouple the telephone line cables at the telephone line jacks. Typically, use common mode chokes and shunt capacitors. Methods to decouple telephone lines are similar to decoupling power lines, however, telephone line decoupling may be more difficult and deserves additional attention. A commonly used design aid is to place footprints for these components and populate as necessary during performance/EMI testing and certification.

5. Decouple the power cord at the power cord interface with decoupling capacitors. Methods to decouple power lines are similar to decoupling telephone lines.

6. Locate cables and connectors so as to avoid coupling from high frequency circuits.

7. Avoid right angle turns on high frequency traces. Forty-five degree corners are good, however, radius turns are better.

9.2.2 Other Considerations in a Modem Design

The pins of all SocketModems are grouped according to function. The DAA interface, host interface, and LED interface pins are all conveniently arranged, easing the host board layout design. Conexant has tested each of the W.Class SocketModems for compliance with their respective country's PTT requirements and has received PTT certificates that cover, without additional expense to the user, all applications that use these SocketModems in their respective countries. The certificates apply only to designs that route TIP and RING (pins 1 and 2) directly to the telco jack. Only specified EMI filtering components are allowed on these two signals.

10 Protocol Compliance

iChip complies with the following Internet standards:

RFC 768	User Datagram Protocol (UDP)
RFC 791	Internet Protocol (IP)
RFC 792	Internet Control Message Protocol
RFC 793	Transmission Control Protocol (TCP)
RFC 821	Simple Mail Transfer Protocol (SMTP)
RFC 826	Ethernet Address Resolution Protocol (iChip LAN)
RFC 951	Bootstrap Protocol (iChip LAN)
RFC 822	Standard for the Format of ARPA Internet Text Messages
RFC 1331	Point-to-Point Protocol (PPP) (iChip CO561AD-S/P)
RFC 1332	PPP Internet Protocol Control Protocol (IPCP) (iChip CO561AD-S/P)
RFC 1334	PPP Authentication Protocols (PAP) (iChip CO561AD-S/P)
RFC 1661	Point-to-Point Protocol (PPP) (iChip CO561AD-S/P)
RFC 1939	Post Office Protocol - Version 3 (POP3)
RFC 1957	Some Observations on the Implementations of the Post Office Protocol (POP3)
RFC 2045	Multipurpose Internet Mail Extensions (MIME) Part One: Format of Internet Message Bodies
RFC 2046	Multipurpose Internet Mail Extensions (MIME) Part Two: Media Types
RFC 2047	MIME (Multipurpose Internet Mail Extensions) Part Three: Message Header Extensions for Non-ASCII Text
RFC 2048	Multipurpose Internet Mail Extensions (MIME) Part Four: Registration Procedures
RFC 2049	Multipurpose Internet Mail Extensions (MIME) Part Five: Conformance Criteria and Examples
RFC 2068	HyperText Transfer Protocol HTTP/1.1
RFC 2131	Dynamic Host Configuration Protocol (iChip LAN)
RFC 2132	DHCP Options and BOOTP Vendor Extensions (iChip LAN)

Table 10-1 Internet Protocol Compliance

11 List of Terms and Acronyms

10BaseT	10-Mbps baseband Ethernet specification using two pairs of twisted-pair cabling (Category 3, 4, or 5): one pair for transmitting data and the other for receiving data.
ARP	**Address Resolution Protocol**. Internet protocol used to map an IP address to a MAC address.
AT+i™	**Connect One's** Internet extension to the industry-standard Hayes AT command set. Supports simplified Internet connectivity commands in the spirit of the AT syntax.
Base64	**Encoding scheme**, which converts arbitrary binary data into a 64-character subset of US ASCII. The encoded data is 33% larger than the original data.
CHAP	**Challenge Authentication Protocol.** Extends the PAP procedure by introducing advanced elements of security.
DHCP	**Dynamic Host Configuration Protocol.** Provides a mechanism for allocating IP addresses dynamically so that addresses can be reused when hosts no longer need them.
DNS	**Domain Name System**. Defines the structure of Internet names and their association with IP addresses.
iChip™	**Connect One's Internet Controller for embedded Internet connectivity.**
ICMP	**Internet Control Message Protocol**. Network layer Internet protocol that reports errors and provides other information relevant to IP packet processing.
IP	**Internet Protocol**. Provides for transmitting blocks of data, called datagrams, from sources to destinations, which are hosts identified by fixed length addresses. Also provides for fragmentation and reassemble of long datagrams, if necessary.
IPCP	**Internet Protocol Control Protocol**. Establishes and configures the Internet Protocol over PPP. Also negotiates Van Jacobson TCP/IP header compression with PPP.
ISP	**Internet Service Provider**. Commercial company that provides Internet access to end (mostly PC) users through a dial-up connection.
LAN	**Local Area Network**. High-speed, low-error data network covering a relatively small geographic area (up to a few thousand meters).
LCP	**Link Control Protocol**. Negotiates data link characteristics and tests the integrity of the link.
MAC	**Media Access Control.** Lower of the two sublayers of the data link layer defined by the IEEE. The MAC sublayer handles access to shared media, such as whether token passing or contention will be used.
MAC Address	Standardized data link layer address that is required for every port or device that connects to a LAN. Other devices in the network use these addresses to locate specific ports in the network and to create and update routing tables and data structures. MAC addresses are 6 bytes long and are controlled by the IEEE. It is represented as a 12-digit hexadecimal integer, where the first (left-most) six digits are the Connect One company identification "000394".

MIME	**Multipurpose Internet Mail Extensions**. Extends the format of mail message bodies to allow multi-part textual and non-textual data to be represented and exchanged between Internet mail servers.
PAP	**Password Authentication Protocol**. Used optionally by the PPP protocol to identify the user to the ISP.
ping	**packet internet groper**. ICMP echo message and its reply. Often used in IP networks to test the reachability of a network device.
POP3	**Post Office Protocol Version 3**. Allows a workstation/PC to dynamically retrieve mail from a mailbox kept on a remote server.
PPP	**Point-to-Point Protocol**. Communications protocol used to send data across serial communication links, such as modems.
RFC	**Request For Comments**. Collections of standards that define the way remote computers communicate over the Internet.
SMTP	**Simple Mail Transfer Protocol**. Provides for transferring mail reliably and efficiently over the Internet.
TCP	**Transmission Control Protocol**. Provides reliable stream-oriented connections over the Internet. Works in conjunction with its underlying IP protocol.
"Leave on Server"	**An option** designating whether retrieved Email messages are to be left intact on the server for subsequent downloads or are to be deleted from the server after a successful download.

Table 11-1 Terms and Acronyms

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