Network Processing Unit (NPU)

The HD64180S network processing unit (NPU) contains a 2-channel high-speed, multifunction serial interface, 8-bit CPU, 2-channel direct memory access controller (DMAC) with a chained block transfer function, timers, etc., all integrated on a single chip. The HD64180S is thus well suited to multiprotocol communications processing.

The multiprotocol serial communications interface (MSCI) and the asynchronous serial communications interface/clocked serial I/O port (ASCI/CSIO) allow high-speed data transfer using various communications protocols.

In particular, the MSCI is capable of handing asynchronous, byte synchronous, and bit synchronous communications protocols. Since the MSCI is connected to the on-chip DMAC, it is possible to realize high-speed single-address DMA transfer (chained-block transfer) in frame units during bit synchronous communications. Furthermore, the flexible processing capability of the HD64180S's CPU ensures compatibility with a wide range of communications protocols.

Features

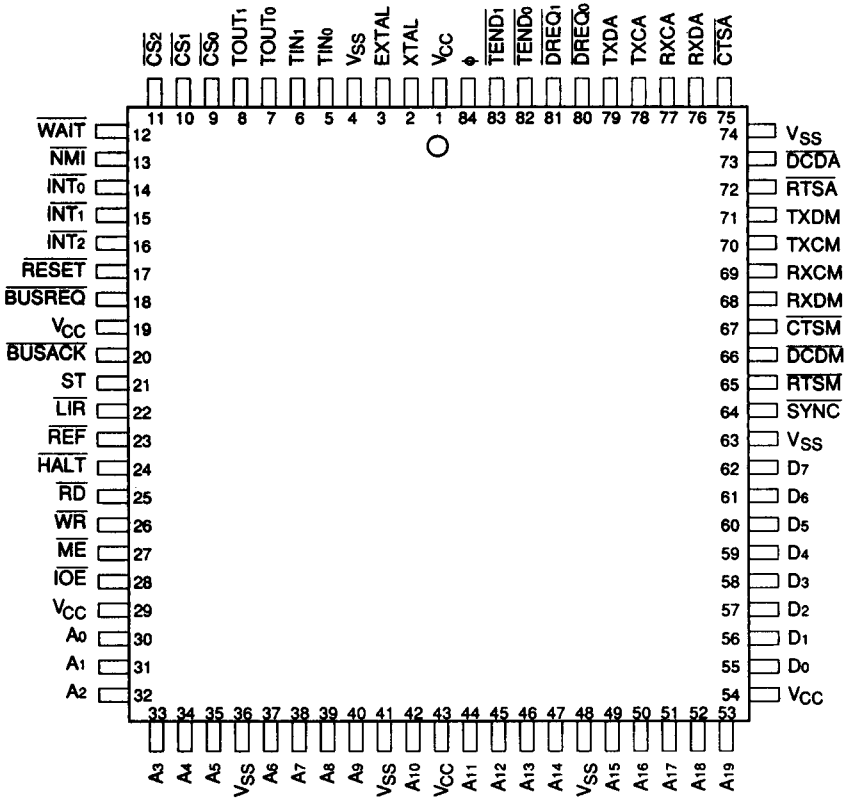
- CPU
  - Software-compatible with HD64180Z
  - 80-type bus interface
  - On-chip MMU (1 Mbyte physical address space)
- DMAC
  - 2 channels
  - DMA transfer between memory and memory, memory and I/O (memory-mapped I/O), and memory and MSCI
  - Chained-block transfer between memory and MSCI
  - Internal interrupts can be requested
- Multiprotocol serial communications interface (MSCI)
  - Full duplex channel
  - Asynchronous, byte synchronous (mono-, bi-, or external synchronous), or bit synchronous (HDLC or loop), selectable
  - Transmit/receive control using modem control signals ($\overline{\text{RTSM}}$, $\overline{\text{CTSM}}$, and $\overline{\text{DCDM}}$)
  - Internal Advanced Digital PLL (ADPLL) clock extraction receive data and/or receive clock noise suppression
  - On-chip baud rate generator
  - Internal interrupts can be requested
  - Maximum transfer rate 7.1 Mbps (with 10 MHz clock)
- Asynchronous serial communications interface /clocked serial I/O port (ASCI/CSIO)
  - Full duplex channel
  - Asynchronous or clocked serial mode (selectable)
  - Transmit/receive control using modem control signals ($\overline{\text{RTSA}}$, $\overline{\text{CTSA}}$, and $\overline{\text{DCDA}}$)
  - On-chip baud rate generator
  - Internal interrupts can be requested
- Timers
  - 2 channels
  - 8-bit reloadable up-counter
  - Output waveform generator and external event count functions
  - Internal interrupts can be requested
- Interrupt controller
  - Four external interrupt lines ($\overline{\text{NMI}}$, $\overline{\text{INT}_0}$, $\overline{\text{INT}_1}$, and $\overline{\text{INT}_2}$)
  - Fifteen internal interrupt sources
- Memory access support function
  - Internal refresh controller
  - Internal wait state controller
  - Internal chip-select controller
- Other functions
  - On-chip clock oscillator circuit
  - Low power dissipation modes (sleep and system stop)

Ordering Information

Product name	Max operating frequency	Package
HD64180SCP6	6	CP–84 (84-pin PLCC)
HD64180SCP8	8	
HD64180SCP10	10	
HD64180SH6	6.17	FP–80A (80-pin QFP)
HD64180SH8	8	
HD64180SH10	10	

Pin Arrangement

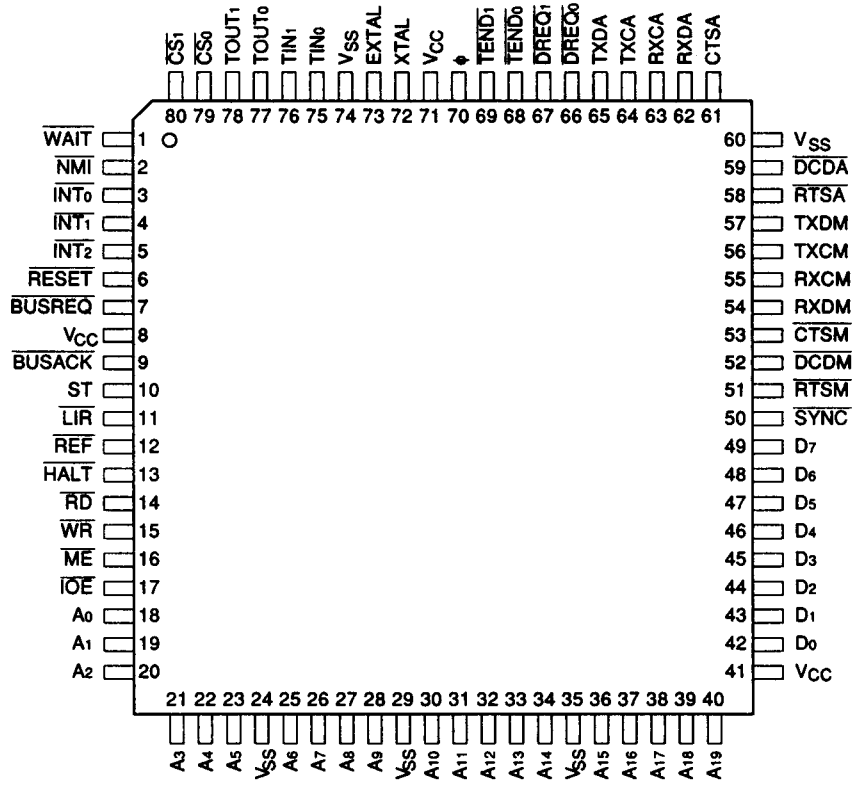
• CP–84



(Top View)

Pin Arrangement (cont)

• FP–80A



(Top View)

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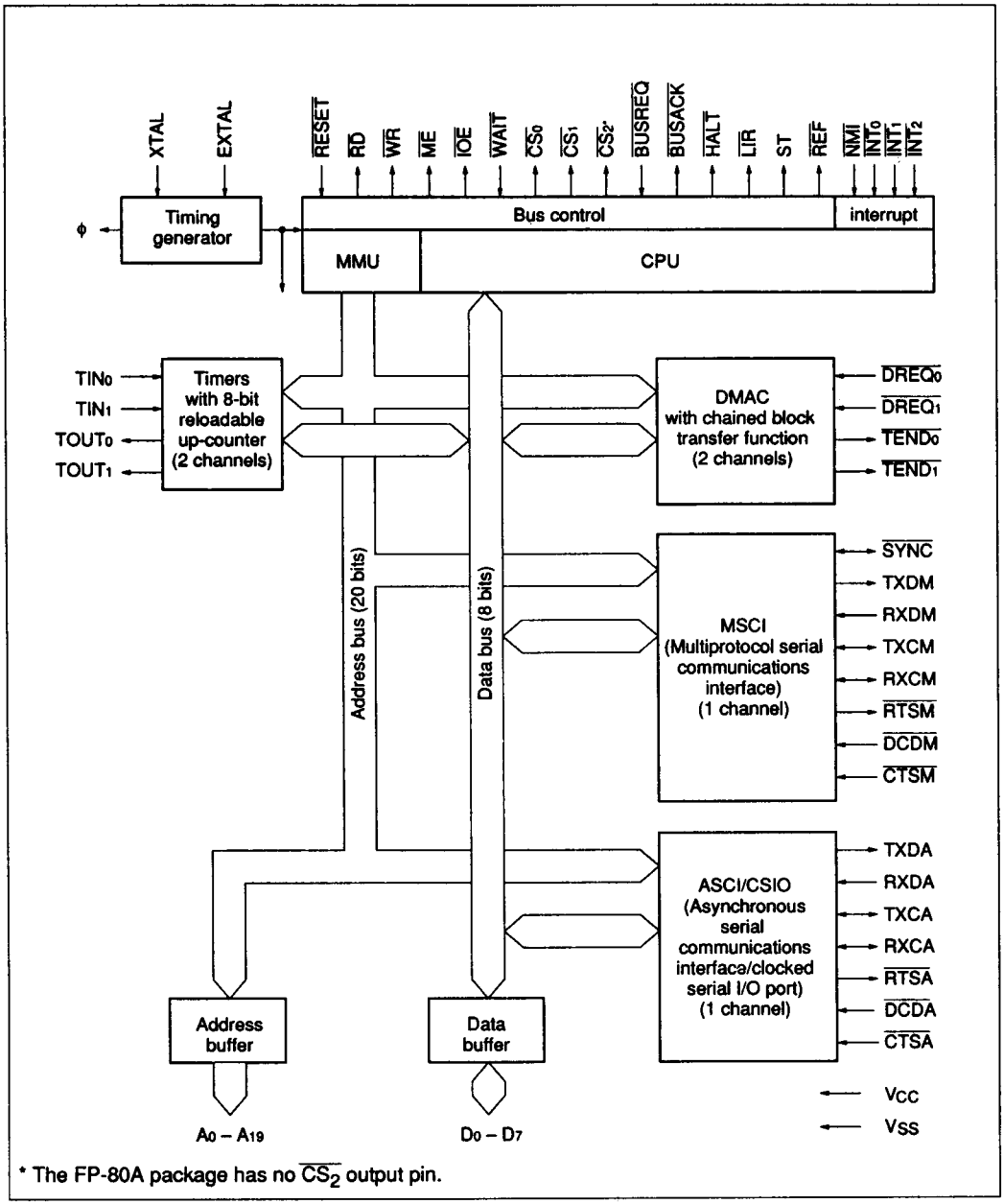
Block Diagram



* The FP-80A package has no $\overline{CS_2}$ output pin.

Pin Functions

Power Supply

Signal	Pin number CP-84	Pin number FP-80A	Input/ Output	Remarks
V_{CC}	1, 19, 29, 43, 54	8, 41, 71	Input	+5 V power supply: All V_{CC} pins must be connected to the +5 V system power supply.
V_{SS}	4, 36, 41, 48, 63, 74	24, 29, 35, 60, 74	Input	Ground: All V_{SS} pins must be connected to the system ground (0 V).

Note: 1. To minimize potential variations, use the shortest possible lead length to the V_{CC} and V_{SS} pins.

Clock

Signal	Pin number CP-84	Pin number FP-80A	Input/ Output	Remarks
XTAL	2	72	Input	Crystal resonator input: The input frequency must be twice that of the ϕ clock. When the EXTAL pin is connected to an external clock, the XTAL pin should be left floating.
EXTAL	3	73	Input	Crystal resonator or external clock input: The input frequency must be double that of the ϕ clock. Figures 1 and 2 show crytal resonator and external clock connection diagrams, respectively.
ϕ	84	70	Output	System clock: Supplies the ϕ clock to peripheral devices.

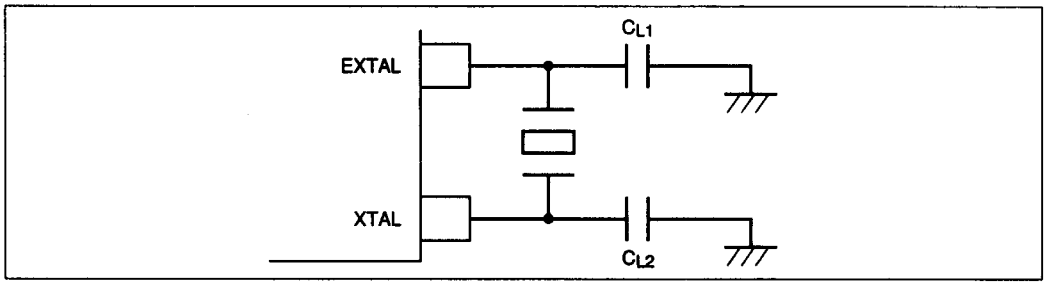


Figure 1 Example of Crystal Resonator Connection

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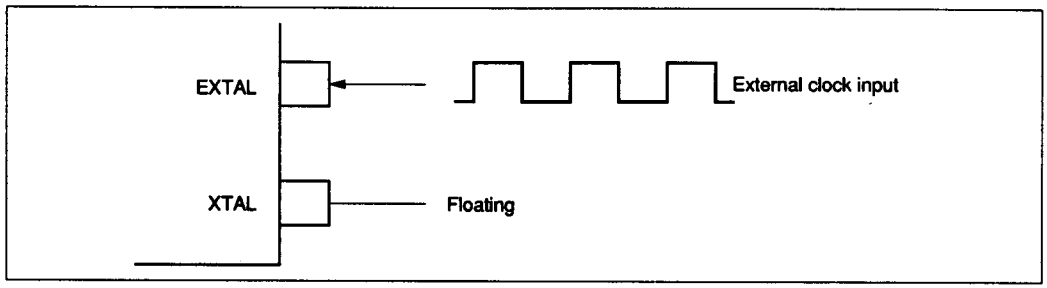

Figure 2 Example of External Clock Connection

Reset

Signal	Pin number CP-84	Pin number FP-80A	Input/ Output	Remarks
$\overline{\text{RESET}}$	17	6	Input	Reset: When this line is driven active low for 6 or more clock cycles, the HD64180S enters the reset mode and all NPU functions are reset.

Address Lines

Signal	Pin number CP-84	Pin number FP-80A	Input/ Output	Remarks
A_0 to A_{19}	30 to 35, 37 to 40, 42, 44 to 47, 49 to 53	18 to 23, 25 to 28, 30 to 34, 36 to 40	Output (High impedance)	Address bus: This 20-bit address bus supports 1 Mbyte of memory and a 64 kbyte (16-bit address width) I/O space. The address bus goes to high impedance during: • Reset mode • Bus release mode (when the $\overline{\text{BUSREQ}}$ input line is asserted and control of the bus is passed to another device).

Data Lines

Signal	Pin number CP-84	Pin number FP-80A	Input/ Output	Remarks
D_0 to D_7	55 to 62	42 to 49	Input/Output (High impedance)	Data bus: The 8-bit bi-directional data bus handles data input and output.

Memory and I/O Interface Lines

Signal	Pin number CP–84	Pin number FP–80A	Input/ Output	Remarks
$\overline{RD}$	25	14	Output (High impedance	Read: This line is asserted during read cycles. When this line is driven low, the data lines are used as inputs.
$\overline{WR}$	26	15	Output (High impedance)	Write: This line is asserted during write cycles. When this line is driven low, the data lines are used as outputs.
$\overline{ME}$	27	16	Output (High impedance)	Memory enable: This line is used to indicate a memory read or write operation. It is asserted in the following cases: • Instruction fetch, operand read, and memory read/ write instructions • Memory access during DMA cycles • Refresh cycles
$\overline{IOE}$	28	17	Output (High impedance)	I/O enable: This line is used to indicate an I/O read/ write operation. It is asserted in the following cases: • I/O read/write instructions • I/O access during DMA cycles • $\overline{INT_0}$ acknowledge cycles
$\overline{WAIT}$	12	1	Input	Wait: This line is used to delay either memory or I/O read/write cycles. If this line is low at the falling edge of a T_2 state, a T_W state is inserted. If the line is still low at the falling edge of the inserted T_W state, an additional T_W state is inserted. This process is repeated until the signal level on this line is high at the falling edge.
$\overline{CS_0}$	9	79	Output	Chip select: The wait controller partitions the physical address space into three areas. These lines output chip select signals during access to each area.
$\overline{CS_1}$	10	80	Output	
$\overline{CS_2}$	11	—*1	Output	

Physical address area accessed	Signal asserted
PAL area (lower physical address area)	$\overline{CS_0}$
PAM area (middle physical address area)	$\overline{CS_1}$
PAH area (upper physical address area)	$\overline{CS_2}$*1

Note: 1. The FP–80A package has no $\overline{CS_2}$ output line.

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System Control Signal

Signal	Pin number CP-84	Pin number FP-80A	Input/ Output	Remarks
$\overline{\text{BUSREQ}}$	18	7	Input	Bus request: This line is asserted by an external device to request control of the bus. When this line is driven low, the internal bus master waits until the end of the current machine cycle, then places the address lines, the data lines, and some of the memory I/O lines ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{ME}}$, and $\overline{\text{IOE}}$) in the high impedance state.
$\overline{\text{BUSACK}}$	20	9	Output	Bus acknowledge: This line is used by the internal bus master to notify an external device that a $\overline{\text{BUSREQ}}$ signal has been received and the bus has been released.
$\overline{\text{HALT}}$	24	13	Output	$\overline{\text{HALT}}$: This line is asserted whenever a $\overline{\text{HALT}}$ or SLP instruction is executed. It indicates that the CPU is in the halt, sleep, or system stop mode. This line is also used in conjunction with the $\overline{\text{LIR}}$ and ST lines to indicate the status of the CPU and DMAC.
$\overline{\text{LIR}}$	22	11	Output	Load instruction register: This line is asserted during opcode fetch cycles. This line can also be used to output interface signals to Z80 peripheral chips.
ST	21	10	Output	Status: This line is used, together with $\overline{\text{LIR}}$ and $\overline{\text{HALT}}$, to indicate the internal status of the HD64180S (see table).

$\overline{\text{HALT}}$	$\overline{\text{LIR}}$	ST	Status
(1) 1	0*2	0	CPU active (first byte of an opcode fetch)
	1		
(2) 1	0*2	1	CPU active (second or third byte of an opcode fetch)
	1		
(3) X*1	1	0	DMAC operation
(4) 1	1	1	Normal operating mode (other than (1), (2), and (3)) Reset mode
(5) 0	0*2	0	Opcode fetch during halt mode (no instructions are executed)
	1		
(6) 0	1	1	Halt mode (other than (3) and (5)) Sleep mode (other than (3)) System stop mode

$\overline{\text{REF}}$	23	12	Output	Refresh: This line is asserted during DRAM refresh cycles. When $\overline{\text{REF}}$ is low (active), a refresh address is output on the 12 low-order lines (A_0–A_{11}) of the address bus.

Notes: 1. X: Don't care
2. The upper value shows the $\overline{\text{LIR}}$ pin status when the LIRE bit of the operation mode control register is 1 and the lower value shows the $\overline{\text{LIR}}$ pin status when the LIRE bit is 0.

Interrupt Signals

Signal	Pin number CP–84	Pin number FP–80A	Input/ Output	Remarks
$\overline{NMI}$	13	2	Input	Non-maskable interrupt: This line requests a non-maskable interrupt.
$\overline{INT_0}$	14	3	Input	Interrupt 0: This line requests a level-0 maskable interrupt. There are three different modes for level-0 interrupts (see table).
$\overline{INT_1}$	15	4	Input	Interrupt 1 and 2: These lines respectively request a level-1 and level-2 maskable, vectored interrupt.
$\overline{INT_2}$	16	5	Input	

Mode	Description
0	Execute the instruction on the data bus
1	Execute the instruction at address 0038H
2	Vector mode

DMA Signals

Signal	Pin number CP–84	Pin number FP–80A	Input/ Output	Remarks
$\overline{DREQ_0}$	80	66	Input	DMA request for channel 0: This line requests a DMA transfer using internal DMAC channel 0.
$\overline{DREQ_1}$	81	67	Input	DMA request for channel 1: This line requests a DMA transfer using internal DMAC channel 1.
$\overline{TEND_0}$	82	68	Output	Transfer end for channel 0: This line indicates the end of a DMA transfer using internal DMAC channel 0. It is asserted synchronously with the read cycle of the last data transfer.
$\overline{TEND_1}$	83	69	Output	Transfer end for channel 1: This line indicates the end of a DMA transfer using internal DMAC channel 1. It is asserted synchronously with the read cycle of the last data transfer.

Serial I/O (MSCI) Signals

Signal	Pin number CP–84	Pin number FP–80A	Input/ Output	Remarks
TXDM	71	57	Output	Transmit data from the MSCI: This line is used to output transmit data from the MSCI.
RXDM	68	54	Input	Receive data to the MSCI: This line is used to input receive data to the MSCI.
TXCM	70	56	Input/Ouput	Transmit clock for the MSCI: This line is used to input/output the MSCI transmit clock. There are three programmable modes: Input: • External transmit clock Output: • Transmit clock from the on-chip baud rate generator • Receive clock (used as the transmit clock)
RXCM	69	55	Input/Output	Receive clock for the MSCI: This line is used to input/output the MSCI receive clock. This line can also be used to input the ADPLL operating clock. There are four programmable modes: Input: • External receive clock • ADPLL operating clock Output: • Receive clock extracted by the ADPLL (the baud rate generator provides the ADPLL operating clock) • Receive clock from the baud rate generator
$\overline{\text{RTSM}}$	65	51	Output	Request to send for MSCI: Indicates that the HD64180S has data to be output to a communications device such as modem. This line can be automatically controlled by MSCI operation (auto-enable function). This line can also be used as a general-purpose output port.
$\overline{\text{DCDM}}$	66	52	Input	Data carrier detect for MSCI: Indicates that a communications device such as modem is receiving valid data from the communications line. MSCI receive operations can be automatically controlled by this input (auto-enable function). This line can also be used as a general-purpose input port.
$\overline{\text{CTSM}}$	67	53	Input	Clear to send for MSCI: Indicates that a communications device such as modem is ready to send data to the communications line. MSCI transmit operations can be automatically controlled by this input (auto-enable function). This line can also be used as a general purpose input port.

Serial I/O (MSCI) Signals (cont)

Signal	Pin number CP–84	Pin number FP–80A	Input/ Output	Remarks
$\overline{SYNC}$	64	50	Input/Output	Synchronization for MSCI: This line is used as an input in external byte synchronous mode. Synchronization is established by detecting the falling edge of $\overline{SYNC}$. This line is used as an output in byte synchronous mono-sync or bi-sync mode or bit-synchronous mode. In byte-synchronous mono-sync or bi-sync mode, a low pulse is output immediately after a SYN pattern is detected. In bit-synchronous mode, a low pulse is output immediately after a flag pattern is detected. In the asynchronous mode, this line is used as an input, but the input value does not affect operation.

Serial I/O (ASCI/CSIO) Signals

Signal	Pin number CP–84	Pin number FP–80A	Input/ Output	Remarks
TXDA	79	65	Output	Transmit data for ASCI/CSIO: This line is used to output transmit data from the ASCI/CSIO.
RXDA	76	62	Input	Receive data for ASCI/CSIO: This line is used to input receive data to the ASCI/CSIO.
TXCA	78	64	Input/Output	Transmit clock for ASCI/CSIO: This line is used to input/output the ASCI/CSIO transimt clock. There are two programmable modes: Input: • External transmit clock Output: • Transmit clock from the on-chip baud rate generator
RXCA	77	63	Input/Output	Receive clock for ASCI/CSIO: This line is used to input/output the ASCI/CSIO receive clock. There are two programmable modes: Input: • External receive clock Output: • Receive clock from the on-chip baud rate generator
$\overline{RTSA}$	72	58	Output	Request to send for ASCI/CSIO: Indicates that the HD64180S has data to be output to a communications device such as a modem. This line can be automatically controlled by ASCI/CSIO operation (auto-enable function). This line can also be used as a general-purpose output port.

Serial I/O (ASCI/CSIO) Signals (cont)

Signal	Pin number CP–84	Pin number FP–80A	Input/ Output	Remarks
$\overline{DCDA}$	73	59	Input	Data carrier detect for ASCI/CSIO: Indicates that a communications device such as a modem is receiving valid signals from the communications line. ASCI/CSIO receive operations can be automatically controlled by this input (auto-enable function). This line can also be used as a general-purpose input port.
$\overline{CTSA}$	75	61	Input	Clear to send for ASCI/CSIO: Indicates that a communications device such as modem is ready to send data to the communications line. ASCI/CSIO transmit operations can be controlled automatically by this input (auto-enable function). This line can also be used as a general-purpose input port.

Timer Lines

Signal	Pin number CP–84	Pin number FP–80A	Input/ Output	Remarks
TIN_0	5	75	Input	Timer inputs for channels 0 and 1: Event counter signals are input via these lines.
TIN_1	6	76	Input	
$TOUT_0$	7	77	Output	Timer outputs for channels 0 and 1: Timer signals are output via these lines.
$TOUT_1$	8	78	Output	