1. SYSTEM OVERVIEW

The OakNote™ Notebook PC subsystem is a set of highly integrated, semi-custom ICs designed from 80286 and 80386SX notebook PCs with clock speeds ranging from 8 Mhz to 20 Mhz. The subsystem consists of:

- OTI041 : System Support and Address Generation Logic
- OTI042 : I/O Control and Data Path Control Logic
- OTI043 : Flat Panel VGA Controller

The OakNote™ subsystem brings to systems designers an optimal solution for implementing a low cost and high performance PC/AT Laptop/Notebook system. To implement a full function PC/AT system, all that is required are: OTI041, OTI042, OTI043, CPU, ROM, RAM, I/O Controller, 8042 & one 7406. This system provides an amazing savings in PC board area. The OakNote™ also features a tightly-coupled video subsystem. The Flat Panel VGA Controller (OTI043) achieves the highest possible video performance by utilizing local bus architecture.

With the OakNote™ subsystem, there is no need for extensive BIOS development to implement your power management scheme. The O/S Independent Power Management Scheme and Activities Monitors, inside the subsystem, can bring the Laptop/Notebook system into power savings mode automatically without BIOS intervention.

The OTI041 integrates all the system support logic functions and address generation logic. It is implemented with 1.2 micron HCMOS technology and packaged in a 160 -pin PJQFP. The OTI041 features the following functions:

- Supports 80286 and 80386SX processors.
- Supports local bus video
- Supports local bus programmable memory range
- CPU clock control for power savings in Laptop/Notebook design
- Supports cartridge ROM
- Command state machine generates memory, I/O & Interrupt Acknowledge commands.
- Address and data path control that includes byte swapping for 16 bit to 8 bit memory or I/O devices.
- Memory controller, refresh cycle generator, EMS logic that supports EMS 4.0 specifications.
- Bus arbiter arbitrates the system bus between CPU, DMA, and DRAM refresh requests.
- Two 82C37 DMA controller running up to 8 Mhz.
- DMA support logic provides 7 channels of DMA page map address and burst mode DMA.
- Integrates all address buffers for the AT-bus.
- Supports fast reset to switch from protected mode to real mode for optimized OS/2 operations.

The OTI042 integrates peripheral devices, data and command buffers. It is implemented with a 1.2 micron HCMOS technology and packaged in a 144-pin PJQFP. The OTI042 features the following functions :

- 3 Activities Monitors for power management
- Automatic power-up functions
- Programmable bidirectional control pins
- Programmable I/O chip select pins
- 8254 compatible timer/counter
- Two 8259 compatible interrupt controllers
- Chip select logic for serial/parallel ports, disk controllers, video controller,and keyboard controller.
- Supports both 80287 & 80387SX with 80386 CPU
- Supports 80287 with 80286 CPU
- Memory parity checker & generator
- NMI generation logic
- 146818 compatible real-time clock with 128 bytes of CMOS RAM.
- Integrates all data buffers on the AT-bus.
- 82385SX support
- Optional external data buffer support

The OTI043 integrates all the key system elements for supporting a variety of flat panels on a single chip. It is implemented with a 1.0 micron HCMOS technology and packaged in a 160-pin PJQFP. The OTI043 features the following functions :

- Fully compatible to IBM VGA Hardware
- Supports CRT monitors and flat panel displays
- 800x600 resolution with 64 gray levels for flat panels and 256 colors for CRTs
- Supports 256Kx4 and 64Kx16 DRAMs
- O/S independent power management scheme
- Internal data cache
- Maximum pixel clock frequency up to 50Mhz
- Intelligent color summing and contrast adjusting logic
- Automatic video compensation logic adapts to different panel resolutions
- Integrated palette and separate LCD video timing circuit
- Local bus option with OTI40 Core Logic Subsystem

2.0 Introduction

The OTI042 is an integrated I/O peripheral controller implemented in double metal HCMOS process. It is housed in an industrial standard 144 pin plastic quad flat package and is intended to be used with OTI041 as a chip set for IBM AT compatible system.

The OTI042 consists of the following functional blocks:

- Dual **8259** compatible interrupt controllers
- **8254** compatible timer/counter
- **Chip select logic** for floppy disk controller , hard disk subsystem ,keyboard controller parallel/serial ports, and co-processor .
- Co-processor **interface logic**
- Real Time Clock which is compatible to MC146818 with the following exceptions:
    - 128 Bytes of CMOS RAM
    - no CKFS (clock select input)
    - no SQW (square wave output)
- Activity Monitors
- Wakeup Timer
- 82385SX Support
- External Data Buffer Support

3.0 Pin Description

Pin Name	Pin Type	Description
	**** CPU Interface ****	
CPUHLDA	I	CPU HOLD ACKNOWLEDGE: this signal is active when the CPU releases the control of the bus.
SD(0-15)	I/O	CPU DATA BUS (0-15) : is the CPU data bus.
	**** System Interface ****	
DENn	I	DATA BUFFER ENABLE : is an active low control signal to enable/disable the internal data transceiver between SD(0-15) and PCD(0-15).
PDLDIRn	O	EXTERNAL DATA BUFFER OUTPUT ENABLE : is an active low control signal to enable output for the external data transceiver between PCD(0-7) and slot data bus(0-7).
PDHDIRn	O	EXTERNAL DATA BUFFER OUTPUT ENABLE : is an active low control signal to enable output for the external data transceiver between PCD(8-15) and slot data bus(8-15).
ENSWAPn	I	ENABLE DATA SWAP: is an input signal used for enabling the byte swapping data buffer.
XD7-XD0	I/O	XD BUS : bi-directional data lines to/from the XD bus for accessing onboard peripherals.
IORDn	I	I/O READ COMMAND : active low command to instruct the I/O device to drive its data onto the data bus.
IOWRn	I	I/O WRITE COMMAND : active low command to instruct the I/O device to read the data present on the data bus.
MEMRDn	I	MEMORY READ COMMAND : active low signal to instruct the memory subsystem to drive its data onto the data bus.

MEMWRn	I	MEMORY WRITE COMMAND : active low signal to instruct the memory subsystem to read the data present on the data bus.
REFRQT	O	REFRESH REQUEST: indicates to the arbiter in the OTI041 that DRAM needs refreshing.
CROMCSn	I	CARTRIDGE ROM CHIP SELECT: An active low input signal from OTI041 indicating cartridge ROM is being accessed.
SEL0	I/O	SELECT FUNCTION 0: is one of the two address encoding signals. It is output during refresh period as TURBO signal for the OTI041.
SEL1	I	SELECT FUNCTION 0: together with SEL0 encodes the following address ranges:

SEL1	SEL0	FUNCTION
0	0	Nothing selected
0	1	A15-A10 = 0 (I/O) onboard video RAM
1	0	onboard video ROM
1	1	I/O channel memory but within 1M and not including onboard video RAM & ROM

ROMCS-	I	ROM CHIP SELECT : is an active low signal used to enable the ROM BIOS to output data on to the data bus.
VDPMSELn	O	VIDEO ROM CHIP SELECT : is the chip select signal for on board video ROM.
VDSEL/VGAEN	O	VIDEO CHIP SELECT/VGA ENABLE : is the chip select signal for on board video I/O and RAM address space, special for OAK VGA OTI037. If IBM compatible VGA is used, this pin becomes VGA enable signal.

**** 82385SX Support ****

FGA20	O	FAST GATE A20

FLUSH	O	FLUSH CACHE : this pin acts as cache flush when EMS mapper is updated.
	**** Bus Interface ****	
PCMEMRDn	O	MEMORY READ COMMAND : active low signal to instruct the memory subsystem within 1M on the I/O channel to drive its data onto the data bus.
PCMEMWRn	O	MEMORY WRITE COMMAND : active low signal to instruct the memory subsystem within 1M on the I/O channel to store the data present on the data bus.
PCAEN	O	ADDRESS ENABLE : signal to de-gate the I/O devices from the I/O channel and allow DMA transfers to take place.
MASTERn	I	MASTER: this signal is used together with a DRQ line to gain control of the system.
PCD(0-15)	I/O	IO CHANNEL DATA BUS (0-15) : is the IO channel data bus. There are 2 sets of data transceivers that are connected internally, i.e. between SD(0-7) and PCD(0-7) and between SD(8-15) and PCD(8-15) .
SADR9 - SADR0	I	ADDRESS BUS: I/O channel address bus.
PBHEn	I	BYTE HIGH ENABLE
MREFn	I	MEMORY REFRESH CYCLE : active low. It indicates that the system is in the memory refresh cycle.
	**** Real Time Clock ****	
XTAL1	I	XTAL INPUT FOR RTC: is the crystal input for the built-in real time clock.
XTAL2	O	XTAL OUTPUT FOR RTC: is the crystal output for the built-in real time clock.
VDDRTC	I	POWER: battery power for the built-in Real Time Clock.
	**** Reset Generation ****	

PWRGOOD	I	POWER GOOD: PWRGOOD is coming from the power supply to indicate that power is stable.
RESET	I	RESET : is an active high signal synchronized to the CPU clock to reset the system.
	**** Timer Counter ****	
SPKOUT	O	SPEAKER DATA OUTPUT : speaker output data, to be connected to a speaker driver to drive the speaker or beeper.
	**** Interrupt Controller ****	
IRQ1,3-7,9-12,14-15	I	INTERRUPT REQUEST INPUTS : asynchronous interrupt request inputs to the internal 8259 controllers.
INTR	O	INTERRUPT REQUEST : interrupt request to the CPU and is generated whenever a valid IRQ is received.
INTAn	I/O	INTERRUPT ACKNOWLEDGE: is an active low signal from the OTI041 indicating an interrupt acknowledge cycle is in progress.It is output during shutdown/sleep mode to pass wakeup signal to the OTI041,either from WAKEUP pin or from wakeup timer or from INTR signal. This pin also carries MASTERn & single ROM BIOS information from OTI041.
	**** Keyboard and Mouse Interface ****	
SELKBDn	O	SELECT KEYBOARD: active low. Indicates the keyboard controller is selected .
	**** Floppy Disk Controller ****	
FLPCSn	O	FLOPPY SELECT: active low. This pin is to select the floppy disk controller. This pin is multiplexed with POFF4n.
DACK2n	I	DMA ACKNOWLEDGE : active low. It indicates that the floppy disk controller has been granted a DMA cycle.
	**** Hard Disk Controller ****	

SELHDK1n	O	HARD DISK SELECT2: When Conner's hard disk is installed, this pin is used as one of the chip select signal decoding addresses 3F6 & 3F7.This pin is multiplexed with POFF3n.
SELHDK0n	O	HARD DISK SELECT1 : active low to select on-board hard disk drive. This pin is multiplexed with POFF2n.
	**** Co-processor Interface ****	
NPERRn	I	NUMERICAL PROCESSOR ERROR : active low. It indicates that an unmasked exception has occurred during numeric instruction execution when coprocessor interrupt is enabled.
NPBSYn	I	NUMERICAL PROCESSOR BUSY : active low. It is connected directly to the BUSY signal of the co-processor.
NPCSn	O	NUMERICAL PROCESSOR CHIP SELECT : When low, the co-processor is selected.
BUSY286n	O	BUSY TO CPU : active low. It is connected directly to the BUSY input of the CPU.
NPPREQ	I	NUMERICAL PROCESSOR REQUEST : active high. It indicates that the co-processor is requesting an operand transfer. This pin is coming from the PEREQ output of the co-processor.
CPEREQ	O	CPU REQUEST : active high. It indicates to the CPU that the co-processor is requesting an operand transfer. This pin goes to the CPU to request the transfer.
	**** NMI Generation ****	
IOCKn	I	I/O CHANNEL CHECK : when low ,it indicates an I/O channel error condition is detected.
PAR0 - PAR1	I/O	PARITY BIT (0 - 1) : are the memory parity bits for even and odd bytes of the memory bank. Each parity bit is generated and written during the memory write operation. Each is checked and reported on an error to the system at the end of memory read cycle. PAR0 is

		memory parity bit for even byte, PAR1 is the memory parity bit for odd byte.
ENPARn	I	ENABLE MEMORY PARITY : is an active low signal indicating that onboard RAM is being accessed.
RMRDn	I/O	ROM/RAM READ : is an active low signal indicating that onboard ROM or RAM is being read. It is an output equal to NPBSYn signal when I/O address F8 is selected.
NMI	O	NON-MASKABLE INTERRUPT: is an active high signal to CPU indicating that an error has occurred in one of the following area: - memory parity error - I/O channel check signal.
	**** Chip Select Signals ****	
PGIOCS0n	O	PROGRAMMABLE I/O CHIP SELECT 0 : is an active low I/O chip select signal with a programmable I/O address space.
COM1CSn	O	SERIAL PORT 1 CHIP SELECT : is an active low I/O chip select signal for the serial port 1.This pin is multiplexed with POFF7n.
COM2CSn	O	SERIAL PORT 2 CHIP SELECT : is an active low I/O chip select signal for the serial port 2.This pin is multiplexed with POFF8n.
PRTCSn	O	PRINTER PORT CHIP SELECT : is an active low I/O chip select signal for the printer port. This pin is multiplexed with POFF6n.
PRTOEn	O	PRINTER PORT OUTPUT ENABLE : is an active low bidirectional printer port output enable signal. This pin is multiplexed with POFF5n.
	****Power Control Signals****	
POFF0n	I/O	PROGRAMMABLE BIDIRECTIONAL CONTROL SIGNALS: I/O signal to control power to peripherals or as status input to system. This pin is multiplexed with LEDn.

POFF1n-POFF8n	I/O	PROGRAMMABLE BIDIRECTIONAL CONTROL SIGNALS: I/O signal to control power to peripherals or as status input to system. These pins are multiplexed with chip select signals.
HDDPWR	O	HARD DISK POWER: An active high output that controls power to the hard disk.
LCDPWR	O	LCD BACKLIGHT POWER: An active high output controls power to LCD backlight.
LCDMODE0,1	O	LCD POWER SAVINGS MODES CONTROL: signals to control the various LCD standby modes.
SYSPWR	O	SYSTEM POWER CONTROL : An active high output that controls power to the entire system.
	****Miscellaneous****	
WAKEUPn	I	WAKEUP PIN : when active high triggers internal wakeup counter. When the wakeup counter down-counts to zero, the system is resumed from sleep or shutdown mode.
BADBATTn	I	BAD BATTERY INPUT : when active indicates a bad battery status has been detected. This signal level can be readable and it can be optionally enabled to generate NMI.
PWRDOWN	I	POWER DOWN: an active high external input to trigger power-down modes.
CHGCLKn	O	CHANGE SYSTEM SPEED: An active low output to OTI041 for changing system clock frequency. This pin also carries power-savings mode information.
OSC	I	14.318 MHz OSCILLATOR OUTPUT: a 14.318 MHz TTL level clock signal to generate the clock for on-chip 8254.
LEDn	I/O	LED CONTROL OUTPUT OR GENERAL PURPOSE I/O PIN: when active low will turn on the LED which is controlled by TURBOn pin or an OAK proprietary register. Power up default is TURBOn. It can also be used as a general-purpose input/output pin controlled by bit 1 of index register FD.

TURBOn	I	TURBO SPEED SELECTION INPUT : when inactive high forces CPUCLK to be 8MHZ and when active low CPUCLK will be controlled by the speed control register. This pin is multiplexed with POFF1n.
GND	I	GROUND:@0V
VDD	I	POWER : @5V

NOTE:The OTI042 WOULD GO INTO THE TEST MODE UNDER THE FOLLOWING INPUT COMBINATION:

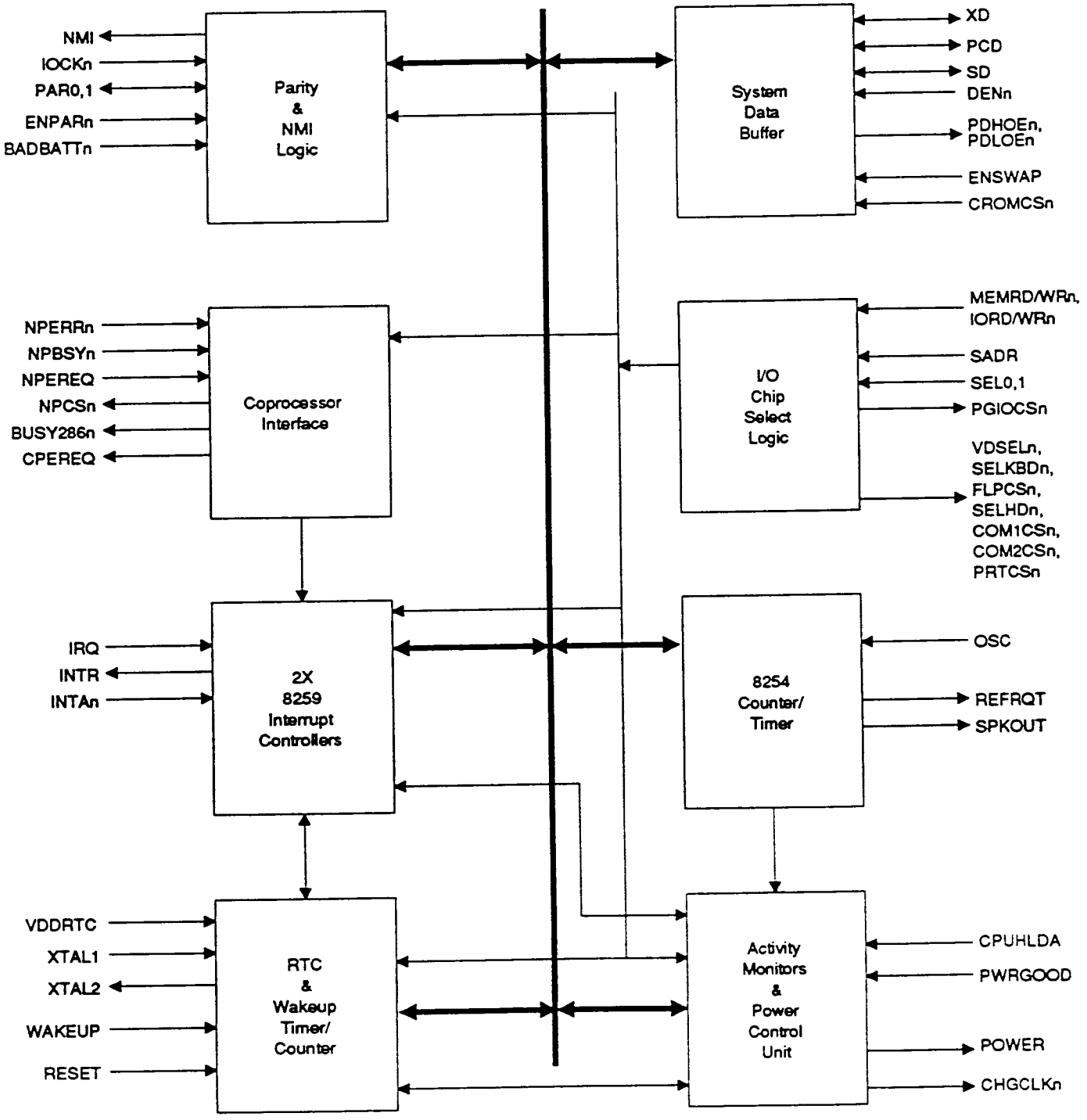
RESET = '0'

MASTERn = '0'

DACK2n = '0'

MREFn = '0'

4.0 System Block Diagram



5.0 OTI042 Special I/O Map

INDEX ADDR	ACCESS	FUNCTION NAME
0004	W	VIDEO0 - Video Interface Control Register
0005	W	VIDEO1 - Video Interface Control Register
0041	R/W	WAKCTR : WAKEUP count Register
0042	R/W	TIMERL : Timer Count Register- Low byte
0043	R/W	TIMERH : Timer Count Register-High byte
0044	R/W	WAKEUP : WakeUp Control Register
00FF	R	CHIPID : OTI042 ID
00FE	R/W	Floppy Interface Control
00FD	R/W	OTI042 Control/Status Register
00FC	R/W	Activity Enable Register
00FB	R	Activity Monitor Status Register
00F9	R/W	System Activity Monitor Interrupt Enable
00F8	R/W	System Activity Monitor Time-Out Value
00F7	R/W	Hard Disk Activity Monitor Interrupt Enable
00F6	R/W	Hard Disk Activity Monitor Time-Out Value
00F5	R/W	Display Activity Monitor Interrupt Enable
00F4	R/W	Display Activity Monitor Time-Out Value
00F3	R/W	Address Compare Enable High Byte Register
00F2	R/W	Address Compare Enable Low Byte Register
00F1	R/W	Address Compare Value High Byte Register
00F0	R/W	Address Compare Value Low Byte Register
0030	R/W	Programmable I/O Address Low Byte Register
0031	R/W	Programmable I/O Address high Byte Register

OTI042 INDEX PORT I/O MAP

I/O ADDRESS	ACCESS	FUNCTION NAME
001E	R/W(0-7)	OAKADR : OAK PORTS INDEX Register
001F	R/W(0-7)	OAKDAT : OAK PORTS DATA Register

NOTE: To access any OTI special port, write the index to port 'H1E first, then perform READ/WRITE operation to data port 'h1F. After each access to port 'H1F, the index value inside port 'H1E is automatically reset to 'H00.

6.0 FUNCTIONAL DESCRIPTION

OTI042 functions can be categorized as follows:

1. Interrupt Control Logic
2. Timer Controller
3. Serial Communication Controller
4. Parallel Port Controller
5. Floppy Disk Decode & Control Logic
6. Hard Disk Decode Logic
7. System Control & Status Registers
8. Co-processor Interface
9. Memory Parity Check & Generation
10. Real Time Clock
11. Programmable I/O chip select
12. Data and Command Buffers
13. Automatic Wakeup
14. 80385SX Support
15. Speed Control

6.1 Interrupt Control Logic

The interrupt control logic includes two Intel 8259A compatible interrupt controllers. It has 16 levels of interrupt that are handled according to programmed priority in the OTI042 chip. The following table shows the hardware interrupts and their availability to the I/O channel.

Level	OTI042 chip	System Board	I/O channel
IRQ0	Timer Channel 0	Not available	Not available
IRQ1	Not used	Keyboard interface	Not available
IRQ2	Slave	Not Available	Not available
IRQ3	Not used	COM2	Available
IRQ4	Not used	COM1	Available
IRQ5	Not used	Parallel port 2	Available
IRQ6	Not used	Diskette drive	Available
IRQ7	Not used	Parallel port	Available
IRQ8	Real Time Clock	Not used	Not Available
IRQ9	Not used	Software redirects to INT 0AH (IRQ2)	Available
IRQ10	Not used	Not used	Available
IRQ11	Not used	Not used	Available
IRQ12	Not used	Mouse(PS2)	Available(AT)
IRQ13	Coprocessor	Not used	Not Available
IRQ14	Not used	Fixed Disk Controller	Available
IRQ15	Not used	Not used	Available

The I/O address for each register in the interrupt controllers is defined in the following table :

ADDRESS	W/R	Function
Master Interrupt Controller		
		*** Initialization Mode ***
0020	W	initialization command word ICW1
0021	W	initialization command word ICW2, ICW3, ICW4
		*** Operation Mode ***
0021	W	operation control word OCW1
0020	W	operation control word OCW2, OCW3

*** Read Status Register (Operation Mode) ***

0021 R interrupt mask register (IMR)

0020 R interrupt request register (IRR) and
interrupt service register (ISR), IRR and ISR
is selected through b0 and b1 in OCW3

ADDRESS	W/R	Function

Slave Interrupt Controller

*** Initialization Mode ***

00A0 W initialization command word ICW1

00A1 W initialization command word ICW2, ICW3, ICW4

*** Operation Mode ***

00A1 W operation control word OCW1

00A0 W operation control word OCW2, OCW3

*** Read Status Register (Operation Mode) ***

00A1 R interrupt mask register (IMR)

00A0 R interrupt request register (IRR) and
interrupt service register (ISR), IRR and ISR
is selected through b0 and b1 in OCW3

The interrupt acknowledge cycle will require one wait states.

6.2 Timer Controller

The timer controller is compatible with Intel 8254. It is a programmable interval timer/counter, or equivalent. It is used as a constant system timer and to control the tone of speaker. This controller contains three timer channels. Each channel is described as follows :

Channel 0 :

This channel is a general purpose timer providing a constant time base for the operating system. The input clock (CLK IN 0) will be running at 1.19 MHz frequency. The enable clock input (GATE 0) is always enabled after power up. The output (CLK OUT 0) of this channel will be connected to interrupt channel 0 (IRQ0) of the interrupt controller.

Channel 1 :

This channel is used to control the DRAM refresh cycles. The input clock (CLK IN 1) will be running at 1.19 MHz. The enable clock input (GATE 1) is always enabled after power up. The output (CLK OUT 1) of this channel goes to the OTI041 as DRAM refresh request.

Channel 2 :

This channel is to control the tone of speaker. The input clock (CLK IN 2) will be running at 1.19 MHz. The enable clock input (GATE 2) is turned on/off by bit 0 of system control register 061h. When bit 0 of I/O PORT 061h is set to one, the frequency of tone is controlled by the counting number in the counter register 2. The output (CLK OUT 2) of this channel is connected to the driver of speaker. After power on or reset, bit 0 of I/O port 061h is reset to zero. More detailed information will be described in the section of system control register (061h).

The I/O address for each register in the timer controller is defined in the following table :

ADDRESS	W/R	Function
0040	W/R	counter register 0
0041	W/R	counter register 1
0042	W/R	counter register 2
0043	W	control mode register

The control mode register is to select the operation mode for each channel in the timer controller. There are six different modes. They are listed as follows :

- mode 0 : interrupt on terminal count
- mode 1 : programmable one-shot
- mode 2 : rate generator
- mode 3 : square wave rate generator
- mode 4 : software triggered strobe

- mode 5 : hardware triggered strobe

More detailed information can be found in Intel 8254 data sheet.

6.3 Serial Communication Controller

The OTI042 chip has two serial communication controller chip select signals which can be optionally set to be COM1(3F8-3FF) or COM2(2F8-2FF) by programming the POS registers.

6.4 Parallel Port Controller

The printer port chip select signal can be configured into either LPT1(3BC-3BF),LPT2(378-37B) or LPT3(278-27B).

6.5 Floppy Disk Controller Address Decode & Control Registers

The OTI042 is capable of decoding the I/O address and generating the select signal for the on-board floppy disk controller. The OTI042 can also control the data buffer between I/O extended bus and I/O Channel during I/O cycle or DMA cycle for the floppy disk controller.

The detailed information of all the floppy control & status registers can be found in the specification of floppy controller chip and NEC floppy controller (NEC 765) data sheet.

6.6 Address Decode for Hard Disk Controller

The OTI042 is capable of decoding the I/O address and generating the select signal for the on-board hard disk controller. The OTI042 also controls the data buffers between I/O extended bus and I/O Channel during I/O cycle or DMA cycle for the hard disk controller. The OTI042 supports Conner's AT hard disk drive. The I/O range for the Conner's drive is 1F0-1F7 and 3F6-3F7 hex.

6.7 System Control & Status Registers

These I/O ports reside in the OTI042 and are used to either control the system or provide the various system status.

System Control Register PORT B (061h)

The system control register (061h) is used for speaker control, I/O Channel check, and memory parity check enable on the system board. This register is a read/write port and whose bit definitions are defined as follows :

SYSCNLB: I/O Port 0061 R/W :

Bit		Function
7	R	Memory parity check
6	R	I/O Channel Check

5 R Timer 2 output

4 R Toggles with each memory refresh request

3 R/W DIS/EN- IOCHCK signal. When set to 1, this bit disables IOCHCK from generating an NMI. When cleared to 0, an NMI is generated when IOCHCK goes active.

2 R/W DIS/EN- memory parity check. When set to 1, this bit disables parity error generation caused by system memory including the EMS memory from generating an NMI. When cleared to 0, an NMI is generated when a memory parity error is sensed.

1 R/W EN/DIS- Beeper Data output. This bit gates the output of timer 2. It is used to disable the timer's sound source or modify its output. When set to 1, this bit enables the output, when cleared, it forces the output to zero.

0 R/W EN/DIS- Timer 2 Gate. This line is routed to the timer input at gate 2. When this bit is cleared to 0, the timer operation is halted. This bit and bit 1 control the operation of the timer's sound source.

At power on or reset, SYSCNTL = 00.

NMICTL: I/O Port 0070 W :

Bit	Function
7	DIS/EN- NMI to the CPU.
6-0	Not used. Reserved as 0's.

At power on or reset, NMICTL is set disabled (bit 7 = 1).

SYSCTLA: System Control Port A is an 8 bit I/O read & write port used to control the security lock and Gate A20.

SYSCNLA: I/O Port 0092 R/W :

Bit	Function
7-4	Reserved
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Reserved

At power on or reset, SYSCNLA reads as 00.

6.8 Co-processor Interface

The OTI042 supports both the 80287 and the 80387SX coprocessor. When the 80286 is used as CPU, only 80287 is supported. When the 80386SX is used , either 80287 or 80387SX could be used as the co-processor.

The OTI042 decodes I/O address range 0F8-0FF hex for the co-processor. During hardware reset, the OTI042 latches the status of NPERRn from the co-processor into bit 6 of the control/status port 2. If the latched bit is low, that implies an 80387SX is used; if the bit is high, 80287 is assumed. BIOS should then detect the existence of the co-processor and set bit 3 of the system/status register 2.

The OTI042 generates IRQ13 and drive BUSYCPUn low when NPERRn is active. And if the 80386SX is used, CPEREQ & NPCSn will be forced high. INTAn signal is used to clear the above latched error condition. The BIOS can also write to F0 & F1 to clear it. IRQ13 will be reset to low only by writing to F0 or F1.

6.9 Memory Parity Check & Generation

Memory parity is generated by the OTI042 during an onboard memory write. During an onboard memory read, the OTI042 also checks the parity bit against the memory data. The parity error information is latched into port 61 hex.

6.10 Real Time Clock

The Real Time Clock is compatible to DALLAS DA1276 with the following exceptions:

- 128 Bytes of CMOS RAM total

- no CKFS (clock select input)

- no SQW (square wave output).

For detailed description of the Real Time Clock, refer to the specification of DA1276.

Power to the Real Time Clock can be backed up by a 3V battery. When the system power is turned off, battery power is routed to the Real Time Clock , so that the Real Time Clock can still continue to run. Battery power is conserved, since it does not go the other circuitry of the chip.

A total of 128 Bytes of CMOS RAM are implemented in the Real Time Clock. The extra 64 bytes can be accessed the same way as through the index register. The index range is 0 - 7F.

RT/CMOS & NMI Mask I/O Port 0070 hex W:

Bit	Function
7	Non-maskable Interrupt (NMI)
	0 - NMI enabled
	1 - NMI disabled
6-0	RT/CMOS RAM

address register to access the CMOS RAM

CMOS RAM Data Register I/O Port 0071 hex R/W:

To access the CMOS RAM, first write the index to port 70 hex, then perform READ/WRITE to port 71.

6.11 Programmable I/O Chip Select

The OTI042 provides one programmable I/O chip select output pin which can be optionally enabled. The I/O address for the I/O chip select can be programmed 8-bit at a time. Two indexed ports are provided to program the 10-bit I/O address and IORD or IOWR qualification enable.

6.12 Data and Command Buffers

The OTI042 integrates the data and command buffers necessary for the PC data bus, CPU data bus and the XD Bus which is used to access onboard peripherals. It also contains the logic for byte swapping. All data and command buffers have a propagation delay of 25ns. The PC data bus loading is designed for 120pF with 12mA IOL. The SD bus has 4mA IOL.

6.13 Automatic Wakeup

The OTI042 supports three modes of automatic wakeup which will resume CPUCLK to the value programmed in index port 3 before shutdown or sleep mode:

- Self-timed wakeup : an internal 16-bit counter clocked once a minute allows the user to program the system to wake up automatically in up to 11 days.

- WAKEUP pin wakeup : wakeup signal coming from the WAKEUP pin which may be connected to RING signal of the MODEM will awaken the system automatically if the wakeup count exceeded the value programmed in the wakeup counter. This counter will be automatically cleared if the wakeup pin doesn't trigger for more than 4 seconds.

- INTR wakeup : INTR signal can be optionally enabled to wakeup the system if it is desired to wakeup the system when any interrupt level is active.

6.14 82385SX Support

When this chip set is used in a 82385SX based cache system, the OTI042 provides 2 pins to facilitate maintaining cache coherency, which are FGA20 and FLUSH.

External gates are needed to gate A20 sending to the 82385SX so that software using 8086-type address wrap around feature can be executed in the cache system. Two gate signals, one from keyboard controller 8042,and another from the OTI042 are OR'ed together to do the job.

When EMS is enabled, writing to IO address 13H or 17H will cause the mapper to be updated. This level of address translation makes the cache invalid every time the mapper is changed. The OTI042 provides FLUSH signal to flush the cache once the above happens.

6.15 Speed Control

The OTI042 provides a TURBO switch input whose level can be read through an index port and will be sent to the OTI041 during refresh period.