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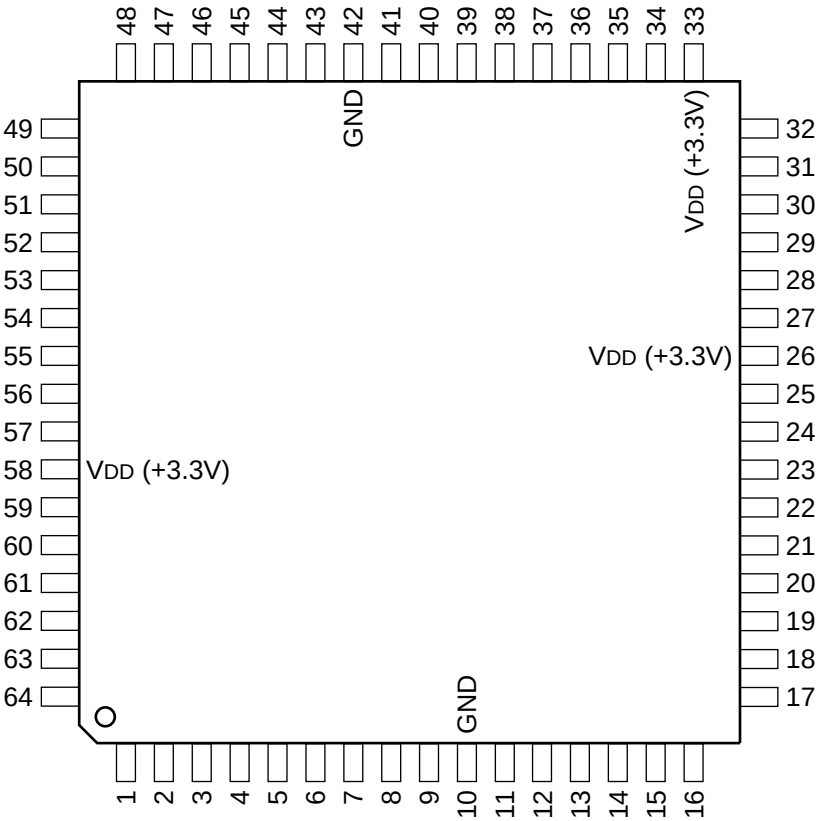
IL08

C-MOS ELECTRONIC ZOOMING/ELECTRICAL IMAGE STABILIZER

-TOP VIEW-



VDD (+3.3V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	CIN1	17	O	TESOUT4	33	O	DFFQ2	49	O	YOUT4
2	I	CIN2	18	O	VSTART	34	I	DFFCLK2	50	O	YOUT5
3	I	CIN3	19	O	NWB	35	I	DFFD2	51	O	YOUT6
4	I	CIN4	20	I	TESIN5	36	O	ANDOUT	52	O	YOUT7
5	O	COUT1	21	I	XCE	37	I	ANDIN	53	O	YOUT8
6	O	COUT2	22	I	SCK	38	I	ANDINB	54	I	YIN1
7	O	COUT3	23	I	SI	39	O	DFFQ1	55	I	YIN2
8	O	COUT4	24	O	HCHDBO	40	I	DFFCLK1	56	I	YIN3
9	I	TESIN1	25	I	VKSCI	41	I	DFFD1	57	I	YIN4
10	—	GND	26	—	VDD	42	—	GND	58	—	VDD
11	I	TESIN2	27	O	CEB	43	O	NME	59	I	YIN5
12	I	TESIN3	28	O	INVOUT	44	I	CHD	60	I	YIN6
13	I	TESIN4	29	I	INVIN	45	I	FP	61	I	YIN7
14	O	TESOUT1	30	O	EXOROUT	46	O	YOUT1	62	I	YIN8
15	O	TESOUT2	31	I	EXORIN1	47	O	YOUT2	63	I	DICK
16	O	TESOUT3	32	I	EXORIN2	48	O	YOUT3	64	I	NRYBY

INPUT

ANDIN	; AND-GATE INPUT
ANDINB	; AND-GATE INPUT
CHD	; HORIZONTAL SYNC PULSE
CIN1-CIN4	; COLOR DIFFERENCE SIGNAL BEFORE ZOOM PROCESSING
DFFCLK1, DFFCLK2	; LATCH CLOCK INPUTS
DFFD1, DFFD2	; LATCH INPUTS
DICK	; Y/C REFERENCE PHASE PULSE
EXORIN1, EXORIN2	; EXCLUSIVE OR-GATE INPUTS
FP	; FRAME PULSE
INVIN	; INVERTING INPUT
NRYBY	; R-Y/B-Y IDENTIFICATION PULSE
SCK	; SERIAL DATA TRANSFER CLOCK
SI	; SERIAL DATA TRANSFER DATA
TESIN1-TESIN5	; TEST (NORMALLY CONNECT TO GROUND)
VKSCI	; VERTICAL INTERPOLATING VALUE LATCH PULSE
XCE	; SERIAL DATA TRANSFER LOAD PULSE
YIN1-YIN8	; LUMINANCE SIGNAL INPUT AFTER ZOOM PROCESSING

OUTPUT

ANDOUT	; AND-GATE OUTPUT
CEB	; CHIP ENABLE
COUT1-COUT4	; COLOR DIFFERENCE SIGNAL AFTER ZOOM PROCESSING
DFFQ1, DFFQ2	; NON-INVERTING OUTPUTS
EXOROUT	; EXCLUSIVE OR-GATE OUTPUT
HCHDBO	; INVERTED CHD AFTER DELAYING
INVOUT	; INVERTING OUTPUT
MWB	; MEMORY WRITE BLANKING PULSE
NME	; VIDEO SIGNAL CONTROL PULSE IN VERTICAL DIRECTION
TESOUT1-TESOUT4	; TEST
VSTART	; V START PULSE
YOUT1-YOUT8	; LUMINANCE SIGNAL OUTPUT BEFORE ZOOM PROCESSING