CML Semiconductor Products

PRODUCT INFORMATION

FX611 Subscriber Private Metering (SPM) Detector

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Provisional Issue

Features/Applications

- Meets 12kHz and 16kHz SPM Specifications
- Tone Follower and SPM Packet Detection Modes
- Adjustable Input Gain
- Low-Power 5V CMOS Process
- PABX and Payphone Applications
- General Purpose Pulse Detection
- Surface Mount and DIL Package Styles
- Crystal Controlled

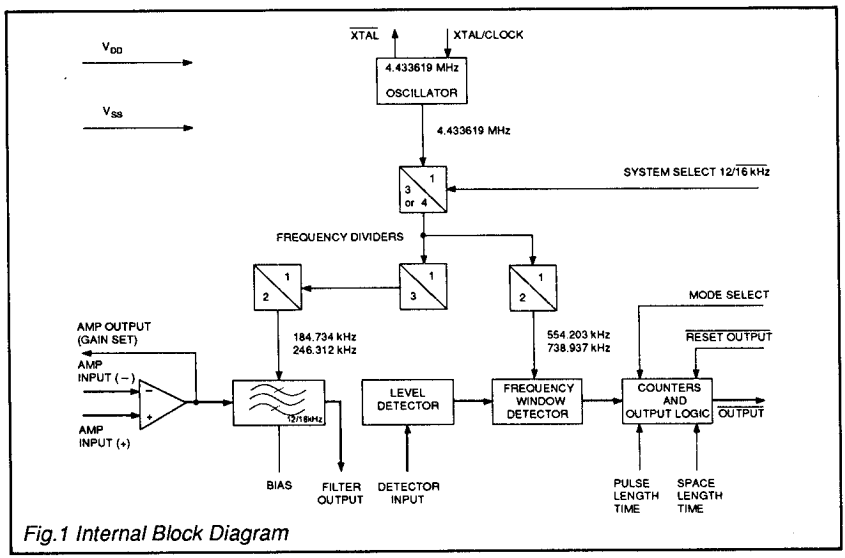


Fig.1 Internal Block Diagram

FX611

Brief Description

The FX611 is a single-chip, low-power CMOS tone detector designed for use in both the PABX and general payphone applications for Subscriber Private Metering. The Decode and Not-Decode band edges are accurately defined by the use of an external 4.433619MHz crystal.
Operation to either of the 12kHz or 16kHz SPM systems is pin programmable, with system amplitude sensitivities and pulse period timing being provided by the use of external components.

The FX611 has 2 modes of operation :

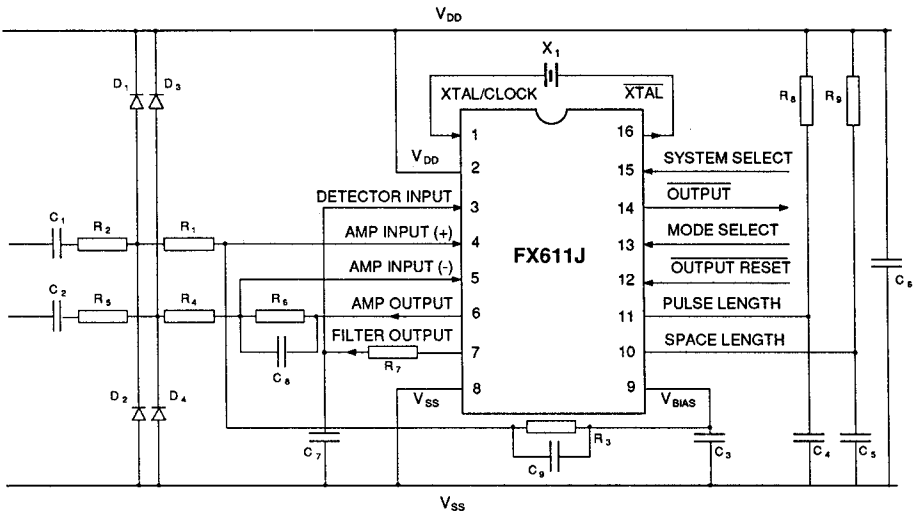
1) Tone Follower Mode.
2) SPM Packet Mode.

1) Tone Follower Mode.
   A logic '0' is output whenever a tone of the correct frequency and period is detected.
2) SPM Packet Mode.
   In this mode an output is obtained only when both the mark and space timing criteria of an SPM pulse have been fulfilled.

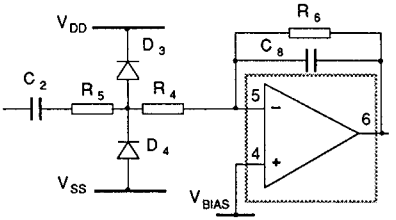
This device, which is available in DIL and SMT packages, requires only a single 5-volt power supply, a 4.433619MHz crystal and external gain and timing components to meet most SPM specifications.

Pin Number		Function
DIL FX611J	Quad FX611LG/LS	
1	1	**Xtal/Clock :** Input to the clock oscillator inverter. A single 4.33619MHz Xtal or external clock pulse is required at this input (see Figure 2).
2	2	V_{DD} : The positive supply rail, a single +5-volt supply is required.
3	5	**Detector Input :** "Schmitt Trigger" level detector circuitry, whose input thresholds are set internally. This input must be connected to the Filter Output pin using the external integration components R_7 and C_7, as shown in Figure 2.
4	6	**Amplifier Input (+) :** The positive and negative amplifier inputs. With single or differential inputs the amplifier and its external circuitry are used to provide the gain required to set the device to the user's National Level Specification. The external diodes are used at both inputs (if in use) to provide protection when the line input level exceeds the supply rails (ie above the Absolute Maximum Rating), see Figures 2 and 3.
5	7	**Amplifier Input (–) :**
6	8	**Amplifier Output :** The output of the input stage amplifier and is used with gain setting components as described above (see Figures 2 and 3).
7	11	**Filter Output :** The switched (12kHz/16kHz) bandpass filter output. This output must be connected to the Detector Input pin using the external integration components R_7 and C_7, as shown in Figure 2.
8	12	V_{SS} : The negative supply rail, (GND).
9	13	V_{BIAS} : The analogue bias point, requires to be externally decoupled to V_{SS} via capacitor C_3.
10	14	**Space Length Time :** Active only in the 'SPM Packet' mode, this input, using an external RC network, sets the minimum valid No-Tone (Space) period for the incoming packet. The minimum valid No-Tone length is set using the formula : $t_S = 0.7\ (R_9 \times C_5)$. If the 'SPM Packet' mode is not required, these timing components may be omitted. See Figure 2.
11	17	**Pulse Length Time :** Active only in the 'SPM Packet' mode, this input, using an external RC network, sets the minimum valid Tone period for the incoming packet. The minimum valid Tone length is set using the formula : $t_M = 0.7\ (R_8 \times C_4)$. If the 'SPM Packet' mode is not required, these timing components may be omitted. See Figure 2.
12	18	$\overline{\text{Output Reset}}$: This input is used only in the 'SPM Packet' mode. Once an SPM Packet has been detected and an output generated (logic "0") from this device the output remains set until this input is set to a logic "0" (note the minimum reset period t_{RESET}, shown on Figure 4). This input has an internal 1MΩ pullup resistor.
13	19	**Mode Select :** A control pin to select either the 'Tone Follower' mode or the 'SPM Packet' mode. A logic "1 " selects 'Tone Follower', a logic "0" selects 'SPM Packet'. This input has an internal 1MΩ pullup resistor (Tone Follower).
14	20	$\overline{\text{Output}}$: The digital output of the SPM Detector. In the 'Tone Follower' mode, a valid Tone gives a logic "0" and No-Tone gives a logic "1." Tonebursts and tone dropouts of less than 16 cycles are ignored. In the 'SPM Packet' mode, the output is set to a logic "0" when a valid 'packet' is measured. The output remains so until reset by a logic "0" at the $\overline{\text{Output Reset}}$ function, see Figure 4.
15	23	**System Select :** A control pin to set the device to work on either a 12kHz (logic "1") or 16kHz (logic "0") SPM system. This input has an internal 1MΩ pullup resistor (12kHz).
16	24	$\overline{\text{Xtal}}$: The output of the clock oscillator inverter, see Figure 2.
	3, 4, 9, 10, 15, 16, 21, 22.	No internal connection. Leave open circuit.

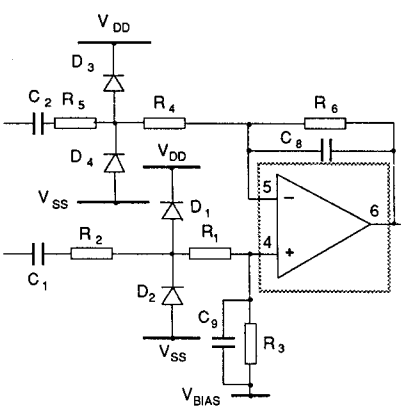
External Components



Component	Reference	Component	Reference
R_1	Figure 3	C_1	Figure 3
R_2	Figure 3	C_2	Figure 3
R_3	Figure 3	C_3	1.0µF ± 20%
R_4	Figure 3	C_4	Note 1
R_5	Figure 3	C_5	Note 1
R_6	Figure 3	C_6	1.0µF ± 20%
R_7	47kΩ ± 1%	C_7	100pF ± 1%
R_8	Note 1	C_8	Note 5
R_9	Note 1	C_9	Note 5
D_1 to D_4	1N4148 or equivalent	X_1	4.433619MHz



(a) Single Input



(b) Differential Input

Fig.2 External Component Connections

Notes

1. Component values (R_8, C_4), set the minimum tone 'Mark' period and (R_9, C_5), set the minimum 'Space' period in the SPM Packet mode and are calculated as :-

$t_M = 0.7\ (R_8 \times C_4)$. $t_S = 0.7\ (R_9 \times C_5)$.

– Mark and Space calculations should be made taking into consideration response times – t_R and t_D (Figure 4). Current consumption will increase if low values of timing resistor are used. –

2. Input Amplifier gain components (Figure 2 (a & b) – these components set the gain required (Figure 3) to achieve the various National Level Specifications.

3. Protection diodes – as most telephone systems operate at voltages in excess of the Absolute Maximum Limits for damage, diodes $D_1 – D_4$ are essential for device protection.

4. Example component values for the West German 'FTZ' Specification (16kHz) :–

"Will Decode" Sensitivity (Min.) **-21dB**

"Will Not Decode" Sensitivity **-27dB**

Calculated gain range: 0 to 3dB. Selected gain: 1.4dB.

R_1– 47kΩ , R_2 – 47kΩ, R_3–130kΩ, R_4 – 47kΩ, R_5– 47kΩ, R_6– 130kΩ.
C_1– 330pf, C_2– 330pf, C_8– 39pf, C_9– 39pf.

Tolerances : Resistors = 1%. Capacitors = 10%.

5. C_8, C_9, are anti-aliasing components and should be set for a cut-off frequency of approximately 32kHz.

Amplitude and Timing

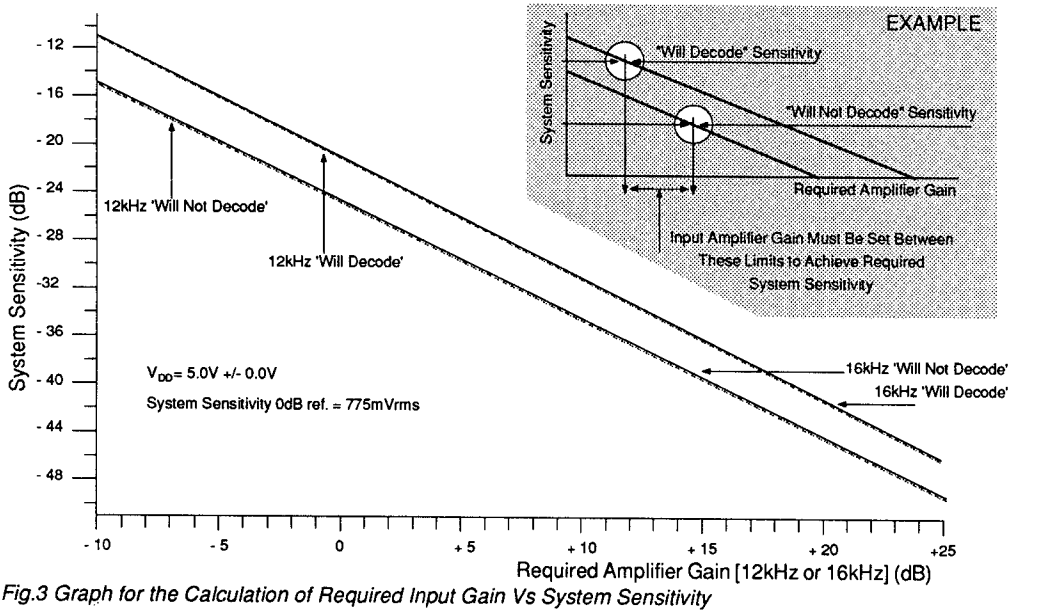


Fig.3 Graph for the Calculation of Required Input Gain Vs System Sensitivity

Input Gain Calculation

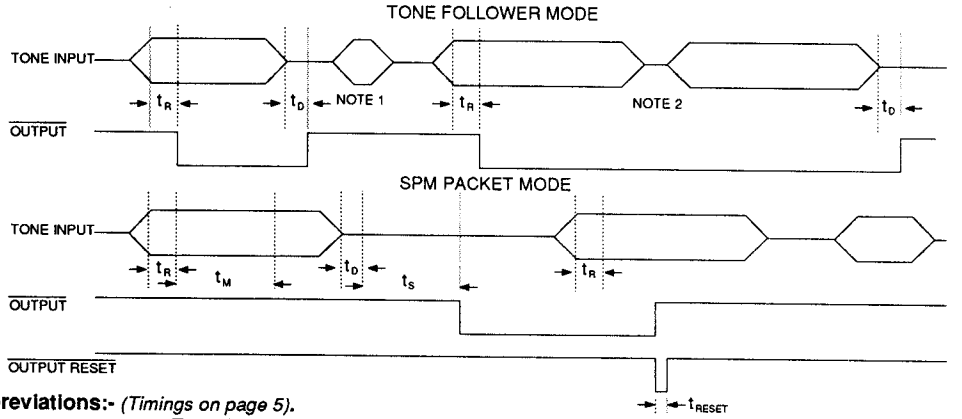
Apply the system 'Will' and 'Will-Not' Decode sensitivity values ('Y' axis) to the relevant graph in Figure 3. The 'X' axis indicates the input gain area required.

Gain is calculated as :–

$$\frac{Z_{feedback}}{Z_{input}} = \frac{R_6 \,//\, X(C_8)}{R_4 + R_5 + X(C_2)}$$

and $R_3 = R_6$, $R_1 = R_4$, $R_2 = R_5$ — if the differential amplifier is used. $C_9 = C_8$, $C_1 = C_2$

Input resistor, $R_{protect}$ (R_1 or R_4) is intended to prevent the amplifier input pins going beyond the supply rail voltages, therefore when calculating the input gain the value of $R_{protect}$ must be greater or equal to 0.15 $R_{feedback}$ (R_3 or R_6).
It is recommended that the input time constant is set as a highpass value between audio and the SPM tone frequencies, with C_1 or C_2 being calculated with input resistors to achieve both time and gain requirements.



Abbreviations:- *(Timings on page 5).*

t_R – Tone Response Time
t_D – Tone De–response Time
t_M – Pulse Length Time
t_S – Space Length Time
t_{RESET} – SPM Output Reset Time

Note 1 – No reaction to pulses with periods less than 'Tone Response Time'.
Note 2 – No reaction to drop-outs with periods of less than 'Tone De-response Time'.

Fig.4 Timing Information

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply Voltage		-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		± 30mA
(other pins)		± 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX611J**	-30°C to + 85°C (ceramic)
	FX611LG/LS	-30°C to + 70°C (plastic)
Storage temperature range:	**FX611J**	-55°C to +125°C (ceramic)
	FX611LG/LS	-40°C to + 85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified :- V_{DD} = 5.0V, T_{AMB} = 25°C, Xtal/Clock f_0 = 4.433619MHz, Audio level 0dB ref: = 775mV rms.

Signal to Noise Ratio ≥18dB.

Characteristics	System	See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage (V_{DD})			4.5	5.0	5.5	V
Supply Current (I_{DD})			–	3.0	–	mA
Analogue Input Impedance (at pins)			1.0	–	–	MΩ
Digital Input Impedance			–	1.0	–	MΩ
Digital Output Impedance			–	–	10.0	kΩ
Dynamic Values						
Sensitivity	12kHz	7	–	-24.0	–	dB
Sensitivity	16kHz	7	–	-25.5	–	dB
Signal to Noise Ratio		4	18.0	–	–	dB
Detector Threshold (Upper)		8	2.95	3.0	3.05	V
Detector Threshold (Lower)		8	1.95	2.0	2.05	V
Bandpass Filter						
Passband Gain	12kHz		–	16.5	–	dB
Passband Gain	16kHz		–	16.5	–	dB
Passband Ripple	12kHz	6	–	–	1.0	dB
Passband Ripple	16kHz	6	–	–	1.0	dB
Audio Band Attenuation (< 3.4kHz)	12kHz		–	40.0	–	dB
	16kHz		–	50.0	–	dB
Frequency Discrimination						
'Will Decode' Frequency Limits	12kHz		11.82	–	12.18	kHz
	16kHz		15.76	–	16.24	kHz
'Will-Not Decode' Frequency						
Upper Limits	12kHz		12.48	–	50.0	kHz
	16kHz		16.64	–	50.0	kHz
Lower Limits	12kHz		0	–	11.52	kHz
	16kHz		0	–	15.36	kHz
Timing Information						
Valid Toneburst Length (t_M)	12kHz/16kHz	1,2	16.0	–	–	cycles
Valid 'Space' Length (t_S)	12kHz/16kHz	2	5.0	–	–	ms
Tone Response Time (t_R)	12kHz	1,3,4	1.7	–	3.0	ms
	16kHz	1,3,4	1.2	–	2.0	ms
De-response Time (t_D)	12kHz	4,5,9	1.7	–	30.0	ms
	16kHz	4,5,9	1.2	–	20.0	ms
SPM Output Reset Time (t_{RESET})	12kHz/16kHz	2	150.0	–	–	ns

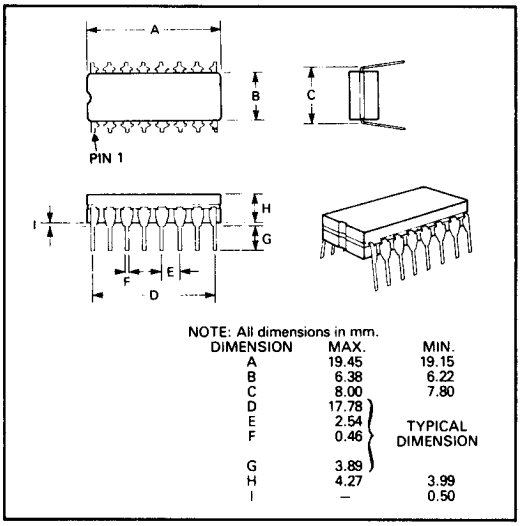
Notes:

1. Tone Follower mode.
2. SPM Packet mode – in this mode the minimum valid Pulse (Space) length is programmable by means of an RC network on the Pulse (Space) Length Time pin. If no RC network is used, the minimum valid tone length reverts to16 cycles.
3. The time for the circuit to recognise a valid 'Tone' in the Tone Follower mode.
4. With the noise level at the input < -11.0dB (100kHz noise bandwidth).
5. The time for the circuitry to recognize a valid 'no tone' in the tone follower mode.
6. Over the 'Will Decode' bandwidth of the frequency discriminator.
7. With the input gains set to unity. Input gain requirements are calculated with reference to Figure 3.
8. These thresholds are measured at 5-volt V_{DD}, any supply variation will alter thresholds accordingly.
9. As the Noise or Gain is increased the de-response time increases.

Package Outline

The FX611J, the cerdip package, is shown in Figure 5. The 'LG' version is shown in Figure 6, and the 'LS' version in Figure 7.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4.
Pins number anti-clockwise when viewed from the top (indent side).

Fig. 5 **FX611J** *16-pin DIL Package*



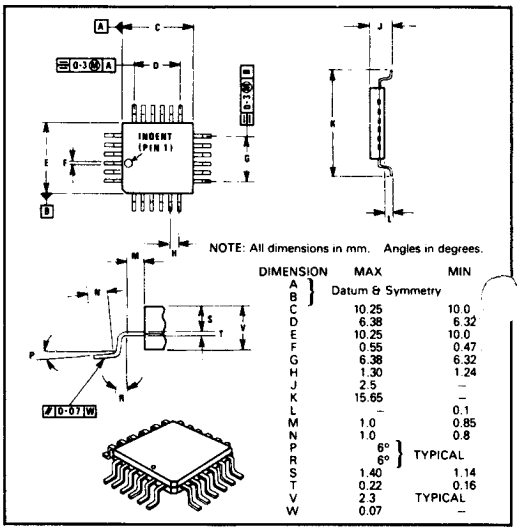
NOTE: All dimensions in mm.

DIMENSION	MAX.	MIN.
A	19.45	19.15
B	6.38	6.22
C	8.00	7.80
D	17.78	
E	2.54	TYPICAL DIMENSION
F	0.46	
G	3.89	
H	4.27	3.99
I	–	0.50

Handling Precautions

The FX611 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

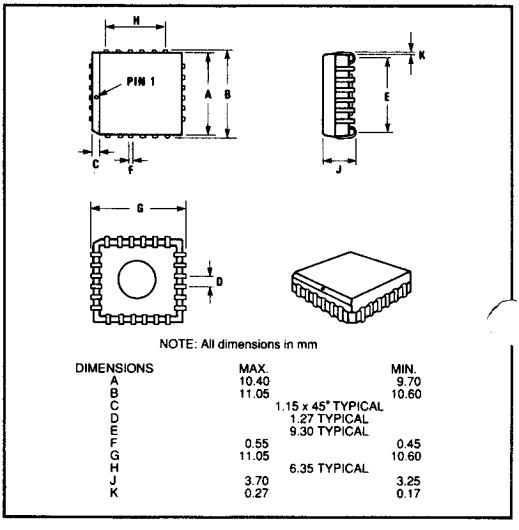
Fig. 6 **FX611LG** *24-pin Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX	MIN
A	Datum & Symmetry	
B		
C	10.25	10.0
D	6.38	6.32
E	10.25	10.0
F	0.55	0.47
G	6.38	6.32
H	1.30	1.24
J	2.5	–
K	15.65	–
L	–	0.1
M	1.0	0.85
N	1.0	0.8
P	6°	TYPICAL
R	6°	
S	1.40	1.14
T	0.22	0.16
V	2.3	TYPICAL
W	0.07	–

Fig. 7 **FX611LS** *24-lead Package*



NOTE: All dimensions in mm

DIMENSIONS	MAX.	MIN.
A	10.40	9.70
B	11.05	10.60
C	1.15 x 45° TYPICAL	
D	1.27 TYPICAL	
E	9.30 TYPICAL	
F	0.55	0.45
G	11.05	10.60
H	6.35 TYPICAL	
J	3.70	3.25
K	0.27	0.17

Ordering Information

FX611J	**16-pin cerdip DIL**
FX611LG	**24-pin quad plastic encapsulated bent and cropped**
FX611LS	**24-lead plastic leaded chip carrier**