19-0667; Rev 0; 10/06

USB 2.0 Full-Speed Transceiver with UART Multiplexing Mode

General Description

The MAX3349EA ±15kV ESD-protected, USB transceiver provides a full-speed USB interface to a lower voltage microprocessor or ASIC. The device supports enumeration, suspend, and VBUS detection. A special UART multiplexing mode routes external UART signals (Rx and Tx) to D+ and D-, allowing the use of a shared connector to reduce cost and part count for mobile devices.

The UART interface allows mobile devices such as PDAs, cellular phones, and digital cameras to use either UART or USB signaling through the same connector. The MAX3349EA features a separate UART voltage supply input to support legacy devices using +2.75V signaling. The MAX3349EA supports a maximum UART baud rate of 921kbaud.

Upon connection to a USB host, the MAX3349EA enters USB mode and provides a full-speed USB 2.0 compliant interface through VP, VM, RCV, and $\overline{OE}$. The MAX3349EA features internal series termination resistors on D+ and D-, and an internal 1.5kΩ pullup resistor to D+ to allow the device to logically connect and disconnect from the USB while plugged in. A suspend mode is provided for low-power operation. D+ and D- are protected from electrostatic discharge (ESD) up to ±15kV.

The MAX3349EA is available in 16-pin TQFN (4mm x 4mm) and 16-bump UCSP™ (2mm x 2mm) packages, and is specified over the -40°C to +85°C extended temperature range.

Applications

Cell Phones

PDAs

Digital Cameras

MP3 Players

Features

- ±15kV ESD HBM Protection on D+ and D-
- UART Mode Routes External UART Signals to D+/D-
- Internal Linear Regulator Allows Direct Powering from the USB Cable
- Separate Voltage Input for UART Transmitter/Receiver (V_{UART})
- Internal 1.5kΩ Pullup Resistor on D+ Controlled by Enumerate Input
- Internal Series Termination Resistors on D+ and D-
- Complies with USB Specification Revision 2.0, Full-Speed 12Mbps Operation
- Built-In Level Shifting Down to +1.4V, Ensuring Compatibility with Low-Voltage ASICs
- V_{BUS} Detection
- Combined VP and VM Inputs/Outputs
- No Power-Supply Sequencing Required
- Available in 16-Bump UCSP (2mm x 2mm) Package

Ordering Information

PART	PIN-PACKAGE	PKG CODE
MAX3349EAEBE+T	16 UCSP	B16-1
MAX3349EAETE**	16 TQFN-EP*	T1644-4

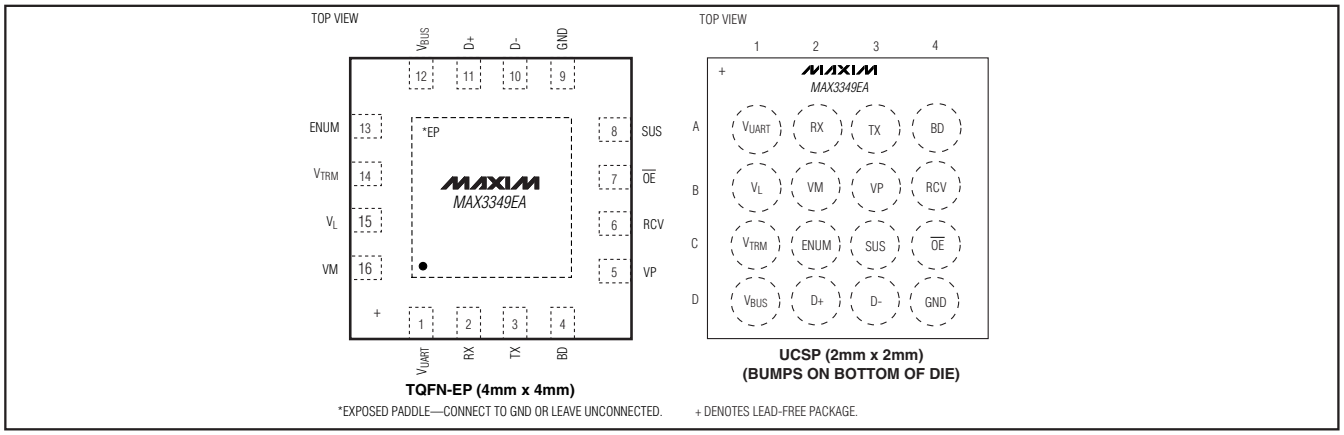
Note: *All devices specified for the -40°C to +85°C extended temperature range.*

***Future product—contact factory for availability.*

**EP = Exposed paddle.*

+Indicates lead-free package.

Pin Configurations



TQFN-EP (4mm x 4mm)

*EXPOSED PADDLE—CONNECT TO GND OR LEAVE UNCONNECTED.

UCSP (2mm x 2mm)
(BUMPS ON BOTTOM OF DIE)

+ DENOTES LEAD-FREE PACKAGE.

UCSP is a trademark of Maxim Integrated Products, Inc.

USB 2.0 Full-Speed Transceiver with UART Multiplexing Mode

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
V_{UART}, V_L, V_{BUS}, D+, D- .....-0.3V to +6V
V_{TRM} .....-0.3V to (V_{BUS} + 0.3V)
VP, VM, SUS, RX, TX, ENUM, RCV, $\overline{OE}$, BD, -0.3V to (V_L + 0.3V)
Short Circuit Current (D+ and D-).....±150mA
Maximum Continuous Current (all other pins) .....±15mA
Continuous Power Dissipation (T_A = +70°C)
16-Bump UCSP (derate 8.2mW/°C above +70°C) 659.5mW
16-Pin 4mm x 4mm TQFN (derate 25.0mW/°C above +70°C).....2000mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Bump Temperature (soldering, reflow).....+235°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BUS} = +4.0V to +5.5V, V_{UART} = +2.7V to +3.3V, V_L = +1.40V to +2.75V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BUS} = +5V, V_L = +1.8V, V_{UART} = +2.75V (UART Mode), and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY INPUTS/OUTPUTS (V_{BUS}, V_{UART}, V_{TRM}, V_L)						
V_{BUS} Input Range	V_{BUS}	USB mode	4.0		5.5	V
V_L Input Range	V_L		1.40		2.75	V
V_{UART} Input Range	V_{UART}	UART mode	2.7		3.3	V
Regulated Supply-Voltage Output	V_{TRM}	Internal regulator, USB mode	3.0		3.6	V
Operating V_{BUS} Supply Current	I_{BUS}	Full-speed transmitting/receiving at 12Mbps, C_L = 50pF on D+ and D-			10	mA
Operating V_{UART} Supply Current	I_{VUART}	UART transmitting/receiving at 921kbaud, C_L = 200pF			2.5	mA
Static V_{UART} Supply Current	$I_{VUART(STATIC)}$	UART mode		3.5	5	µA
Operating V_L Supply Current	I_{VL}	Full-speed transmitting/receiving at 12Mbps, C_L = 50pF on D+ and D-			6	mA
Full-Speed Idle and SE0 Supply Current	$I_{VBUS(IDLE)}$	Full-speed idle, V_{D+} > +2.7V, V_{D-} < +0.3V		290	400	µA
		SE0: V_{D+} < +0.3V, V_{D-} < +0.3V		340	450	
Static V_L Supply Current	$I_{VL(STATIC)}$	Full-speed idle, SE0, suspend mode, or static UART mode		2	10	µA
Sharing Mode V_L Supply Current	$I_{VL(OFF)}$	V_{BUS} and V_{UART} not present		2	5	µA
USB Suspend V_{BUS} Supply Current	$I_{VBUS(SUS)}$	$\overline{VM}$, VP unconnected; $\overline{OE}$ = 1, SUS = 1		38	65	µA
V_{BUS} DETECTION (BD)						
USB Power-Supply Detection Threshold	V_{TH_VBUS}	V_L = +1.8V	1.8	2.7	3.4	V
		V_L = +2.5V	2.3	3.2	4.0	
USB Power-Supply Detection Hysteresis	V_{HYS_VBUS}	V_L = +1.8V		80		mV
		V_L = +2.5V		100		
V_L Power-Supply Detection Threshold	V_{TH_VL}			0.7		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{BUS} = +4.0V to +5.5V, V_{UART} = +2.7V to +3.3V, V_L = +1.40V to +2.75V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BUS} = +5V, V_L = +1.8V, V_{UART} = +2.75V (UART Mode), and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{UART} Power-Supply Detection Threshold	V_{TH_UART}		0.4 x V_L	0.65 x V_L	0.9 x V_L	V
DIGITAL INPUTS/OUTPUTS (VP, VM, RCV, SUS, $\overline{OE}$, RX, TX, ENUM, BD)						
Input Voltage Low	V_{IL}				0.3 x V_L	V
Input Voltage High	V_{IH}		0.7 x V_L			V
Output Voltage Low	V_{OL}	I_{OL} = +2mA, V_L > 1.65V I_{OL} = +1mA, V_L < 1.65V			0.4	V
Output Voltage High	V_{OH}	I_{OH} = +2mA, V_L > 1.65V I_{OH} = +1mA, V_L < 1.65V	V_L - 0.4			V
Input Leakage Current	I_{LKG}		-1		+1	µA
ANALOG INPUTS/OUTPUTS (D+, D- in USB Mode)						
Differential Input Sensitivity	V_{ID}	$\lvert V_{D+} - V_{D-} \rvert$	0.2			V
Differential Common-Mode Voltage	V_{CM}	Includes V_{ID} range	0.8		2.5	V
Single-Ended Input Low Voltage	V_{ILSE}				0.8	V
Single-Ended Input High Voltage	V_{IHSE}		2.0			V
USB Output Voltage Low	V_{USB_OLD}	R_L = 1.5kΩ connected to +3.6V			0.3	V
USB Output Voltage High	V_{USB_OHD}	R_L = 15kΩ connected to GND	2.8		3.6	V
Off-State Leakage Current	I_{LZ}		-10		+10	µA
Driver Output Impedance	Z_{DRV}	Steady-state drive	29.0	38	43.5	Ω
Transceiver Capacitance	C_{IND}	Measured from D+/D- to GND		20		pF
Input Impedance	Z_{IN}	Driver off	0.9	1.3	2.0	MΩ
D+ Internal Pullup Resistor	R_{PU}	ENUM = 1	1425	1500	1575	Ω
ANALOG INPUTS/OUTPUTS (D+, D- in UART Mode)						
Input Voltage High	V_{UART_IH}	UART mode, +2.70 < V_{UART} < +2.85V	2.0			V
Input Voltage Low	V_{UART_IL}	UART mode, +2.70V < V_{UART} < +2.85V			0.8	V
Output Voltage High	V_{UART_OH}	UART mode, +2.70V < V_{UART} < +2.85V I_{UART_OH} = -2mA	2.2			V
Output Voltage Low	V_{UART_OL}	UART mode, +2.70V < V_{UART} < +2.85V I_{UART_OL} = +2mA			0.4	V

USB 2.0 Full-Speed Transceiver with UART Multiplexing Mode

ELECTRICAL CHARACTERISTICS (continued)

(V_{BUS} = +4.0V to +5.5V, V_{UART} = +2.7V to +3.3V, V_L = +1.40V to +2.75V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BUS} = +5V, V_L = +1.8V, V_{UART} = +2.75V (UART Mode), and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION (D+, D-)						
Human Body Model		(Figures 9 and 10)		±15		kV
IEC 61000-4-2 Air-Gap Discharge				±8		kV
IEC 61000-4-2 Contact Discharge				±8		kV

TIMING CHARACTERISTICS

(V_{BUS} = +4.0V to +5.5V, V_{UART} = +2.7V to +3.3V, V_L = +1.4V to +2.75V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BUS} = +5V, V_L = +1.8V, V_{UART} = +2.75V (UART Mode), and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB DRIVER CHARACTERISTICS (C_L = 50pF)						
Rise Time	t_{FR}	10% to 90% of | V_{USB_OHD} - V_{USB_OLD} | (Figures 1 and 7)	4		20	ns
Fall Time	t_{FF}	90% to 10% of | V_{USB_OHD} - V_{USB_OLD} | (Figures 1 and 7)	4		20	ns
Rise/Fall Time Matching	t_{FR}/t_{FF}	Excluding the first transition from idle state (Note 2) (Figures 1 and 7)	90		110	%
Output Signal Crossover Voltage	V_{CRS_F}	Excluding the first transition from idle state (Note 2) (Figure 2)	1.3		2.0	V
Driver Propagation Delay	t_{PLH_DRV}	V_L > +1.65V (Figures 2 and 7)			22.5	ns
		+1.4V < V_L < +1.65V (Figures 2 and 7)			25	
	t_{PHL_DRV}	V_L > +1.65V (Figures 2 and 7)			22.5	
		+1.4V < V_L < +1.65V (Figures 2 and 7)			25	
Driver Disable Delay	t_{PHZ_DRV}	High-to-off transition (Figures 3 and 6)			25	ns
	t_{PLZ_DRV}	Low-to-off transition (Figures 3 and 6)			25	
Driver Enable Delay	t_{PZH_DRV}	Off-to-high transition (Figures 3 and 7)			25	ns
	t_{PZL_DRV}	Off-to-low transition (Figures 3 and 7)			25	
USB RECEIVER CHARACTERISTICS (C_L = 15pF)						
Differential Receiver Propagation Delay	t_{PLH_RCV}	V_L > +1.65V (Figures 4 and 8)			25	ns
		+1.4V < V_L < +1.65V (Figures 4 and 8)			30	
	t_{PHL_RCV}	V_L > +1.65V (Figures 4 and 8)			25	
		1.4V < V_L < +1.65V (Figures 4 and 8)			30	
Single-Ended Receiver Propagation Delay	t_{PLH_SE}	V_L > +1.65V (Figures 4 and 8)			28	ns
		+1.4V < V_L < +1.65V (Figures 4 and 8)			35	
	t_{PHL_SE}	V_L > +1.65V (Figures 4 and 8)			28	
		+1.4V < V_L < +1.65V (Figures 4 and 8)			35	

TIMING CHARACTERISTICS (continued)

(V_{BUS} = +4.0V to +5.5V, V_{UART} = +2.7V to +3.3V, V_L = +1.4V to +2.75V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BUS} = +5V, V_L = +1.8V, V_{UART} = +2.75V (UART Mode), and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Receiver Disable Delay	t_{PHZ_SE}	High-to-off transition, V_L > +1.65V (Figure 5)			10	ns
		High-to-off transition, +1.4V < V_L < +1.65V (Figure 5)			12	
	t_{PLZ_SE}	Low-to-off transition, V_L > +1.65V (Figure 5)			10	
		Low-to-off transition, +1.4V < V_L < +1.65V (Figure 5)			12	
Single-Ended Receiver Enable Delay	t_{PZH_SE}	Off-to-high transition, V_L > +1.65V (Figure 5)			20	ns
		Off-to-high transition, +1.4V < V_L < +1.65 (Figure 5)			20	
	t_{PZL_SE}	Off-to-low transition, V_L > +1.65V (Figure 5)			20	
		Off-to-low transition, +1.4V < V_L < +1.65V (Figure 5)			20	
UART DRIVER CHARACTERISTICS (C_L = 200pF)						
Rise Time (D-)	t_{FR_TUART}	10% to 90% of $\lvert V_{OHD} - V_{OLD} \rvert$ (Figure 13)		60	200	ns
Fall Time (D-)	t_{FF_TUART}	90% to 10% of $\lvert V_{OHD} - V_{OLD} \rvert$ (Figure 13)		60	200	ns
Driver Propagation Delay	t_{PLH_TUART}	(Figure 13)		70	200	ns
	t_{PHL_TUART}	(Figure 13)		70	200	
UART RECEIVER CHARACTERISTICS (C_L = 15pF)						
Receiver (Rx) Propagation Delay	t_{PLH_RUART}	(Figure 14)			60	ns
	t_{PHL_RUART}	(Figure 14)			60	
Receiver (Rx) Rise/Fall Time	t_{FR_RUART}	(Figure 14)			45	ns
	t_{FF_RUART}	(Figure 14)			45	

Note 1: Parameters are 100% production tested at T_A =+25°C, unless otherwise noted. Limits over temperature are guaranteed by design.

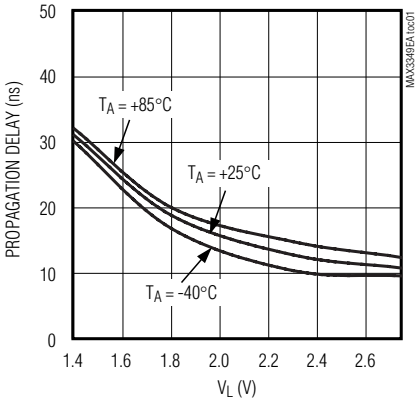
Note 2: Guaranteed by design, not production tested.

USB 2.0 Full-Speed Transceiver with UART Multiplexing Mode

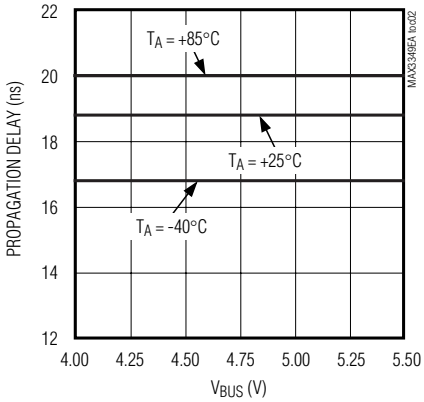
Typical Operating Characteristics

(V_{BUS} = +5V, V_L = +3.3V, V_{UART} = +2.75V, T_A = +25°C, unless otherwise noted.)

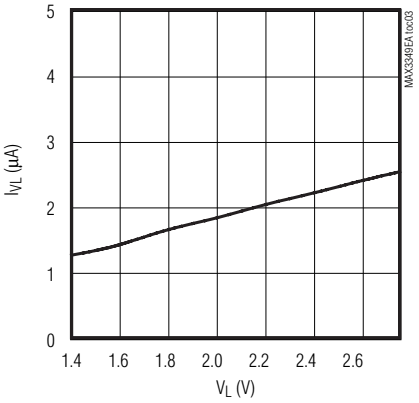
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_L



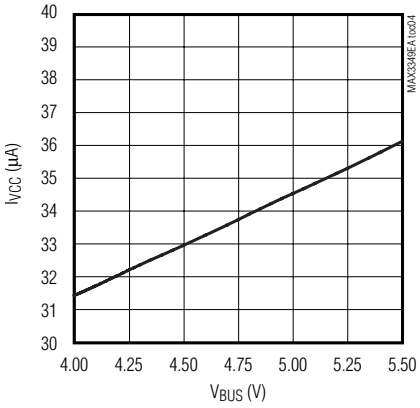
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_{BUS}



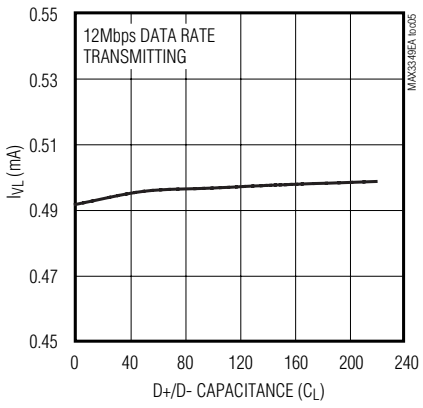
LOGIC CURRENT CONSUMPTION IN SUSPEND MODE



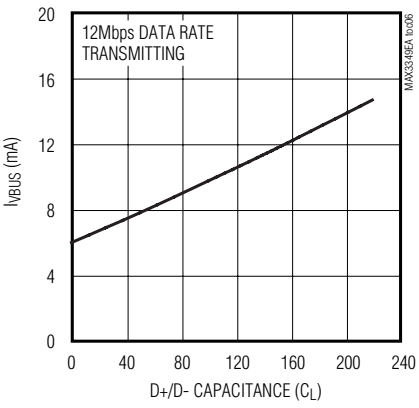
V_{BUS} CURRENT CONSUMPTION IN SUSPEND MODE



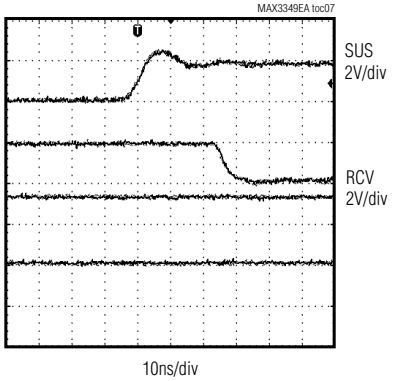
V_L CURRENT DURING USB OPERATION vs. D+/D- CAPACITANCE



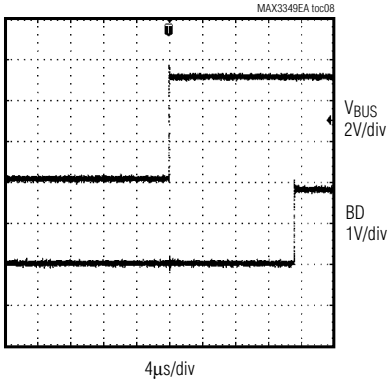
V_{BUS} CURRENT DURING USB OPERATION vs. D+/D- CAPACITANCE



SUSPEND MODE



BUS DETECT RESPONSE



Pin Description

PIN		TYPE	NAME	FUNCTION
UCSP	TQFN			
A1	1	POWER	V_{UART}	UART Supply Voltage. V_{UART} powers the internal UART transmitter and receiver. Connect a regulated voltage between +2.7V and +3.3V to V_{UART}. Bypass V_{UART} to GND with a 0.1µF ceramic capacitor.
A2	2	OUTPUT	RX	UART Receive Output. In UART mode, RX is a level-shifted output that expresses the logic state of D+.
A3	3	INPUT	TX	UART Transmit Input. In UART mode, D- follows the logic state on TX.
A4	4	OUTPUT	BD	USB Detect Output. When V_{BUS} exceeds the V_{TH-BUS} threshold, BD is logic-high to indicate that the MAX3349E is connected to a USB host. The MAX3349E operates in USB mode when BD is logic-high, and operates in UART mode when BD is logic-low.
B1	15	POWER	V_L	Digital Logic Supply. Connect a +1.4V to +2.75V supply to V_L. Bypass V_L to GND with a 0.1µF or larger ceramic capacitor.
B2	16	I/O	VM	Receiver Output/Driver Input. VM functions as a receiver output when $\overline{OE}$ = V_L. VM follows the logic state of D- when receiving. VM functions as a driver input when $\overline{OE}$ = GND (Tables 2 and 3).
B3	5	I/O	VP	Receiver Output/Driver Input. VP functions as a receiver output when $\overline{OE}$ = V_L. VP follows the logic state of D+ when receiving. VP functions as a driver input when $\overline{OE}$ = GND (Tables 2 and 3).
B4	6	OUTPUT	RCV	Differential Receiver Output. In USB mode, RCV is the output of the USB differential receiver (Table 3).
C1	14	POWER	V_{TRM}	Internal Regulator Output. V_{TRM} provides a regulated +3.3V output. Bypass V_{TRM} to GND with a 1µF ceramic capacitor. V_{TRM} draws power from V_{BUS}. Do not power external circuitry from V_{TRM}.
C2	13	INPUT	ENUM	Enumerate Input. Drive ENUM to V_L to connect the internal 1.5kΩ resistor from D+ to V_{TRM} (when V_{BUS} is present). Drive ENUM to GND to disconnect the internal 1.5kΩ pullup resistor. ENUM has no effect when the device is in UART mode.
C3	8	INPUT	SUS	Suspend Input. Drive SUS low for normal operation. Drive SUS high to force the MAX3349E into suspend mode.
C4	7	INPUT	$\overline{OE}$	Output Enable. Drive $\overline{OE}$ low to set VP/VM to transmitter inputs in USB mode. Drive $\overline{OE}$ high to set VP/VM to receiver outputs in USB mode. $\overline{OE}$ has no effect when the device is in UART mode.
D1	12	POWER	V_{BUS}	USB Supply Voltage. V_{BUS} provides power to the internal linear regulator when in USB mode. Bypass V_{BUS} to GND with a 0.1µF ceramic capacitor.
D2	11	I/O	D+	USB Differential Data Input/Output. Connect D+ directly to the USB connector.
D3	10	I/O	D-	USB Differential Data Input/Output. Connect D- directly to the USB connector.
D4	9	POWER	GND	Ground
—	EP	—	EP	Exposed Paddle. Connect exposed paddle to GND.

USB 2.0 Full-Speed Transceiver with UART Multiplexing Mode

Timing Diagrams

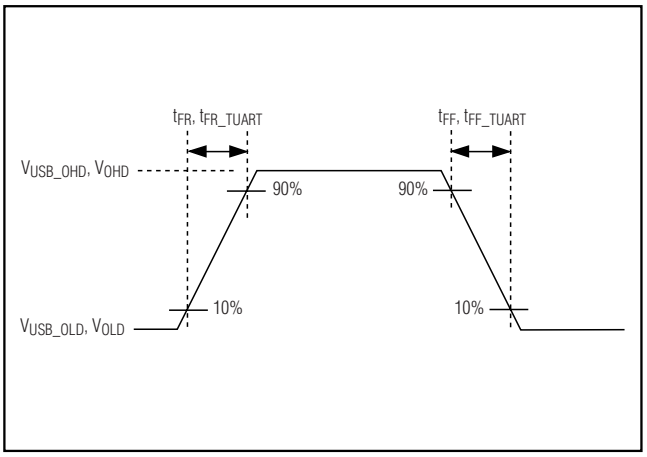


Figure 1. Rise and Fall Times

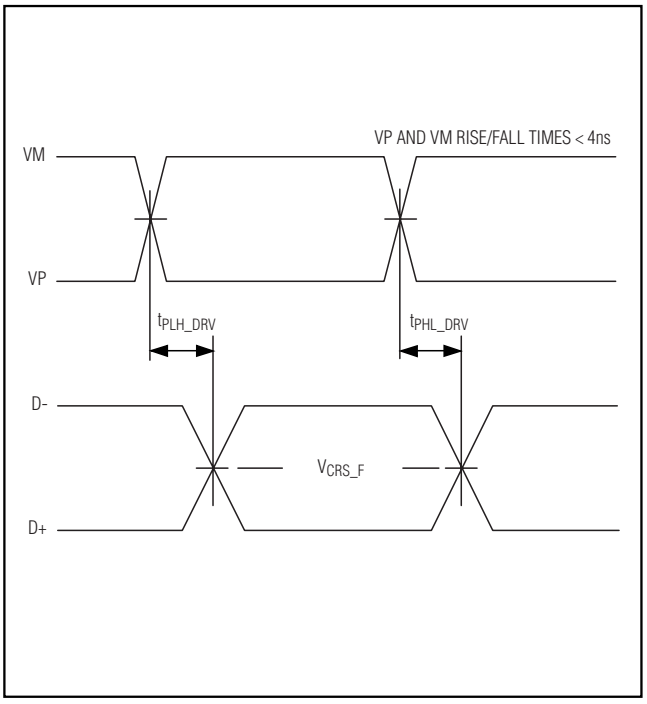


Figure 2. Timing of VP and VM to D+ and D-

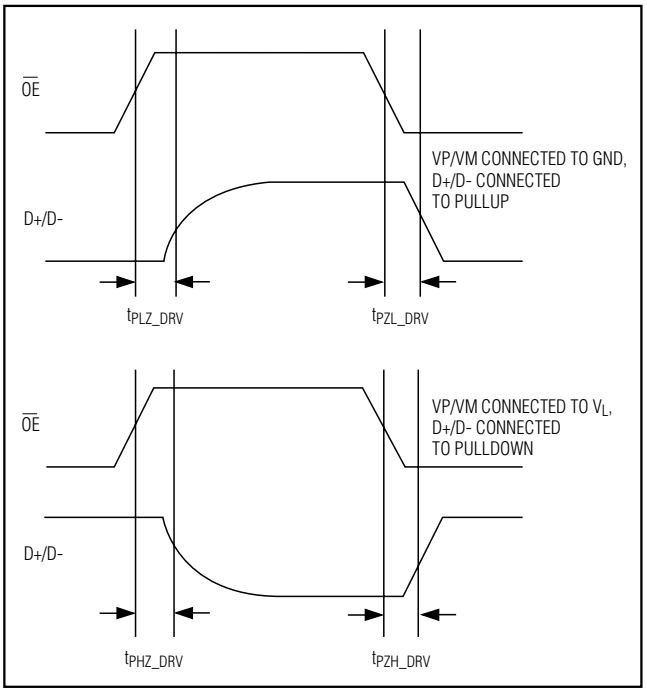


Figure 3. Driver Enable and Disable Timing

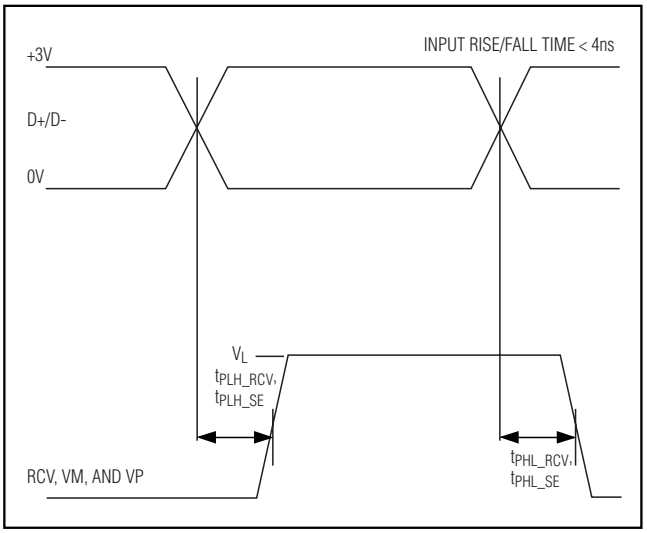


Figure 4. D+/D- Timing to VP, VM, and RCV

Timing Diagrams (continued)

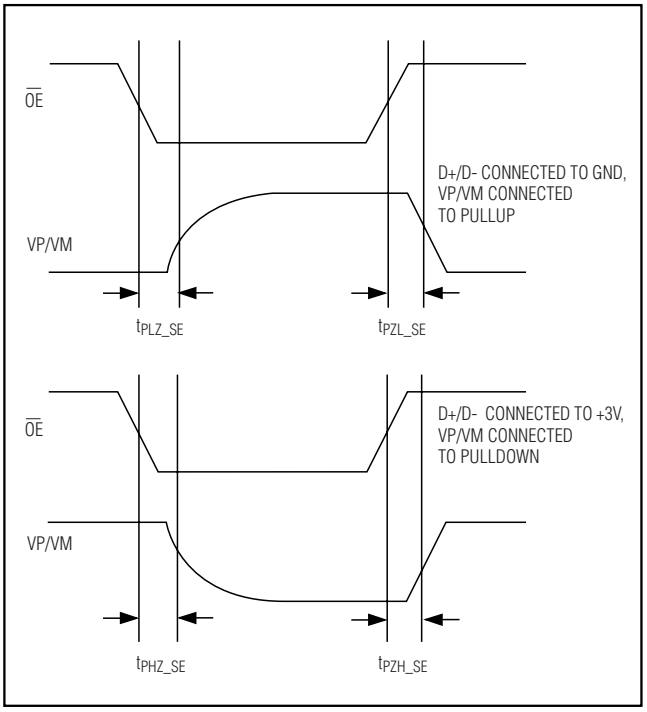


Figure 5. Receiver Enable and Disable Timing

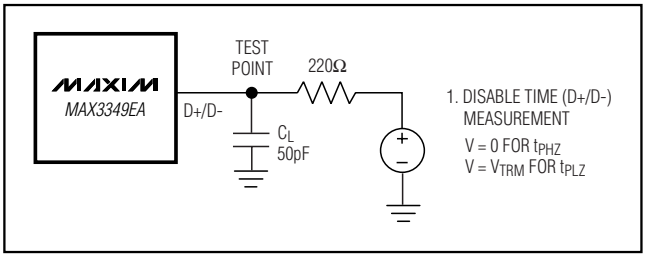


Figure 6. Test Circuit for Disable Time

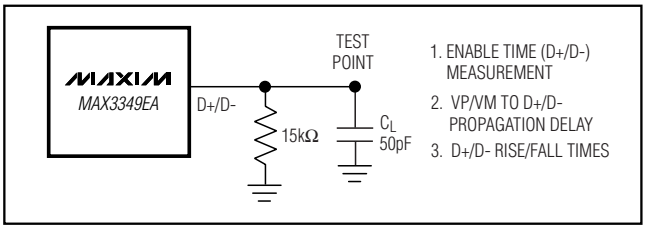


Figure 7. Test Circuit for Enable Time, Transmitter Propagation Delay, and Transmitter Rise/Fall Time

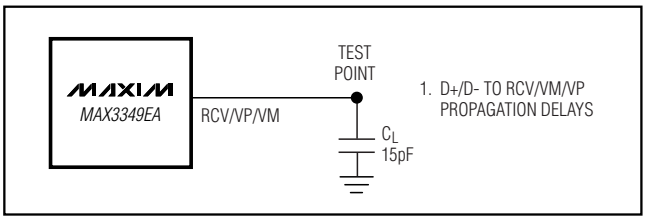


Figure 8. Test Circuit for Receiver Propagation Delay

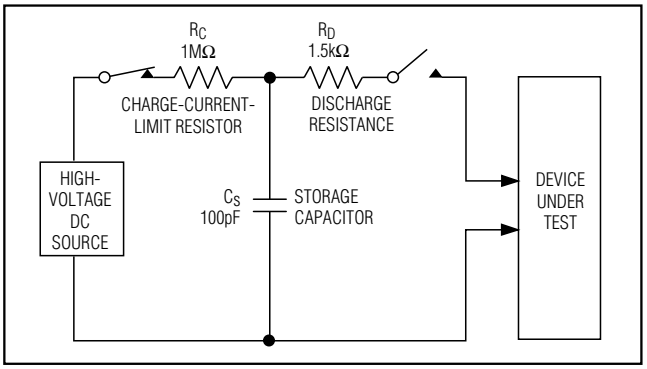


Figure 9. Human Body ESD Test Model

Detailed Description

The MAX3349EA ±15kV ESD-protected, USB transceiver provides a full-speed USB interface to a microprocessor or ASIC. The device supports enumeration, suspend, and V_{BUS} detection. A special UART multiplexing mode routes external UART signals (Rx and Tx) to D+ and D-, allowing the use of a shared connector to reduce cost and part count for mobile devices.

The UART interface allows mobile devices such as PDAs, cellular phones, and digital cameras to use either UART or USB signaling through the same connector. The MAX3349EA features a separate UART voltage supply input. The MAX3349EA supports a maximum UART baud rate of 921kbaud.

Upon connection to a USB host, the MAX3349EA enters USB mode and provides a full-speed USB 2.0 compliant interface through VP, VM, RCV, and $\overline{OE}$. The MAX3349EA features internal series resistors on D+ and D-, and an internal 1.5kΩ pullup resistor to D+ to allow the device to logically connect and disconnect from the USB bus while plugged in. A suspend mode is provided for low-power operation. D+ and D- are protected from electrostatic discharge (ESD) up to ±15kV. To ensure full ±15kV ESD protection, bypass V_{BUS} to

USB 2.0 Full-Speed Transceiver with UART Multiplexing Mode

Timing Diagrams (continued)

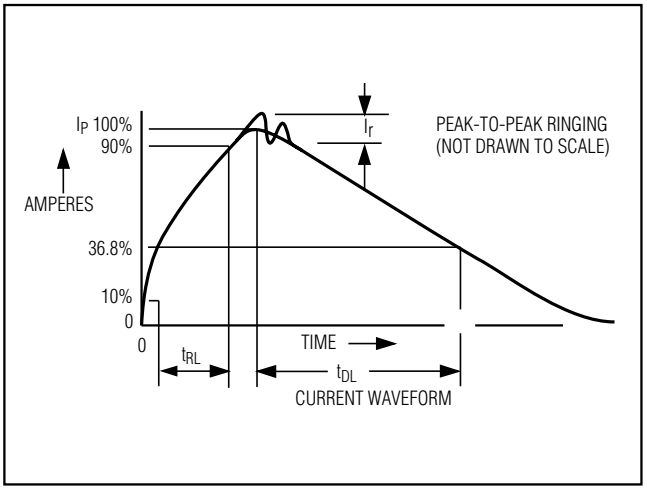


Figure 10. Human Body Model Current Waveform

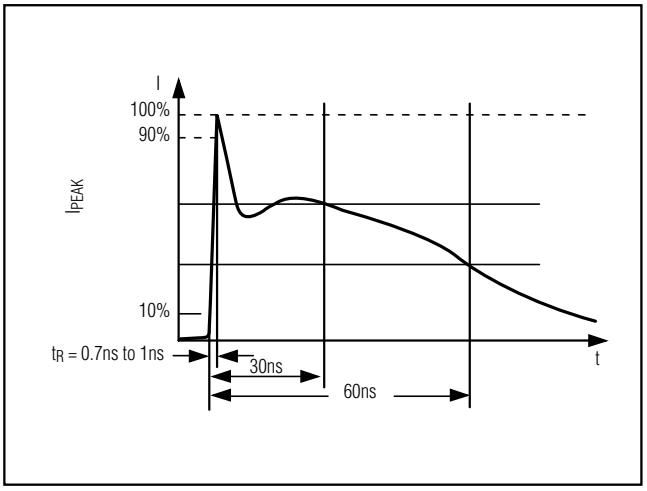


Figure 12. IEC 61000-4-2 Contact Discharge Model Current Waveform

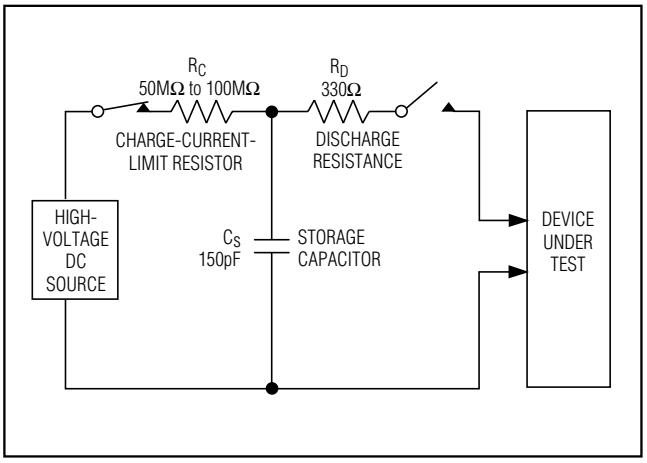


Figure 11. IEC61000-4-2 ESD Contact Discharge Test Model

GND with a 0.1µF ceramic capacitor as close to the device as possible. There are high-impedance resistors ~2MΩ to ground on D+ and D- to prevent floating nodes when in UART mode and nothing is connected.

Operating Modes

The MAX3349EA operates in either USB mode or UART mode, depending on the presence or absence of V_{BUS}. Bus detect output BD is logic-high when a voltage higher than $V_{TH-VBUS}$ is applied to V_{BUS}, and logic-low otherwise. The MAX3349EA operates in USB mode when BD is logic-high, and UART mode when BD is logic-low.

USB Mode

In USB mode, the MAX3349EA implements a full-speed (12Mbps) USB interface on D+ and D-, with enumerate and suspend functions. A differential USB receiver presents the USB state as a logic-level output RCV (Table 3a). VP/VM are outputs of single-ended USB receivers when $\overline{OE}$ is logic-high, allowing detection of single-ended 0 (SE0) events. When $\overline{OE}$ is logic-low, VP and VM serve as inputs to the USB transmitter. Drive suspend input SUS logic-high to force the MAX3349EA into a low-power operating mode and disable the differential USB receiver (Table 3b).

UART Mode

The MAX3349EA operates in UART mode when BD is logic-low (V_{BUS} not present). The Rx signal is the output of a single-ended receiver on D+, and the Tx input is driven out on D-. Signaling voltage thresholds for D+ and D- are determined by V_{UART}, an externally applied voltage between +2.7V and +3.3V.

Power-Supply Configurations

V_L Logic Supply

In both USB and UART modes, the control interface is powered from V_L. The MAX3349EA operates with logic-side voltage (V_L) as low as +1.4V, providing level shifting for lower voltage ASICs and microcontrollers.

Table 1. Power-Supply Configuration

V_{BUS}(V)	V_{TRM}(V)	V_L(V)	V_{UART}(V)	CONFIGURATION
+4.0 to +5.5	+3.0 to +3.6 Output	+1.4 to +2.75	GND, Unconnected, or +2.7V to +3.3V	USB Mode
+4.0 to +5.5	+3.0 to +3.6 Output	GND or Unconnected	GND, Unconnected, or +2.7V to +3.3V	Disable Mode
GND or Unconnected	High Impedance	+1.4 to +2.75	+2.7V to +3.3V	UART Mode

Table 2. USB Transmit Truth Table ($\overline{OE}$ = 0)

INPUTS		OUTPUTS	
VP	VM	D+	D-
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Table 3a. USB Receive Truth Table ($\overline{OE}$ = 1, SUS = 0)

INPUTS		OUTPUTS		
D+	D-	VP	VM	RCV
0	0	0	0	RCV*
0	1	0	1	0
1	0	1	0	1
1	1	1	1	X

** = Last state.*

X = Undefined.

USB Mode

The MAX3349EA is in USB mode when V_{BUS} is greater than V_{TH-BUS} and the bus detect output (BD) is logic-high. In USB mode, power for the MAX3349EA is derived from V_{BUS}, typically provided through the USB connector. An internal linear regulator generates the required +3.3V V_{TRM} voltage from V_{BUS}. V_{TRM} powers the internal USB transceiver circuitry and the D+ enumeration resistor. Bypass V_{TRM} to GND with a 1µF ceramic capacitor as close to the device as possible. Do not power external circuitry from V_{TRM}.

Disable Mode

Connect V_{BUS} to a system power supply and leave V_L unconnected or connect to ground to enter disable mode. In disable mode, D+ and D- are high impedance, and withstand external signals up to +5.5V. $\overline{OE}$, SUS, and control signals are ignored.

Table 3b. USB Receive Truth Table ($\overline{OE}$ = 1, SUS = 1)

INPUTS		OUTPUTS		
D+	D-	VP	VM	RCV
0	0	0	0	0
0	1	0	1	0
1	0	1	0	0
1	1	1	1	0

UART Mode

Connect V_L and V_{UART} to system power supplies, and leave V_{BUS} unconnected or below V_{TH-BUS} to operate the MAX3349EA in UART mode. The MAX3349EA supports V_{UART} from +2.7V to +3.3V (see Table 1).

USB Control Signals

$\overline{OE}$

$\overline{OE}$ controls the direction of communication for USB mode. When $\overline{OE}$ is logic-low, VP and VM operate as logic inputs, and D+/D- are outputs. When $\overline{OE}$ is logic-high, VP and VM operate as logic outputs, and D+/D- are inputs. RCV is the output of the differential USB receiver connected to D+/D-, and is not affected by the $\overline{OE}$ logic level.

ENUM

Drive ENUM logic-high to enable the internal 1.5kΩ pullup resistor from D+ to V_{TRM}. Drive ENUM logic-low to disable the internal pullup resistor and logically disconnect the MAX3349EA from the USB.

SUS

Operate the MAX3349EA in low-power USB suspend mode by driving SUS logic-high. In suspend mode, the USB differential receiver is turned off and V_{BUS} consumes 38µA (typ) of supply current. The single-ended VP and VM receivers remain active to detect a SE0 state on USB bus lines D+ and D-. The USB transmitter remains enabled in suspend mode to allow transmission of a remote wake-up on D+ and D-.

USB 2.0 Full-Speed Transceiver with UART Multiplexing Mode

D+ and D-

D+ and D- are either USB signals or UART signals, depending on the operating mode. In USB mode, D+/D- serve as receiver inputs when $\overline{OE}$ is logic-high and transmitter outputs when $\overline{OE}$ is logic-low. Internal series resistors are provided on D+ and D- to allow a direct interface with a USB connector. In UART mode, D+ is an input and D- is an output. UART signals on Tx are presented on D-, and signals on D+ are presented on Rx. The UART signaling levels for D+/D- are determined by V_{UART}. Logic thresholds for Rx and Tx are determined by V_L. D+ and D- are ESD protected to ±15kV HBM.

RCV

RCV is the output of the differential USB receiver. RCV is a logic 1 for D+ high and D- low. RCV is a logic 0 for D+ low and D- high. RCV retains the last valid logic state when D+ and D- are both low (SE0). RCV is driven logic-low when SUS is high. See Tables 3a and 3b.

BD

The bus-detect (BD) output is asserted logic-high when a voltage greater than V_{TH-BUS} is presented on V_{BUS}. This is typically the case when the MAX3349EA is connected to a powered USB. BD is logic-low when V_{BUS} is unconnected.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. Additional ESD-protection structures guard D+ and D- against damage from ESD events up to ±15kV. The ESD structures arrest ESD events in all operating modes: normal operation, suspend mode, and when the device is unpowered.

Several ESD testing standards exist for gauging the robustness of ESD structures. The ESD protection of the MAX3349EA is characterized to the following standards:

±15kV Human Body Model (HBM)

±8kV Air-Gap Discharge per IEC 61000-4-2

±8kV Contact Discharge per IEC 61000-4-2

Human Body Model

Figure 9 shows the model used to simulate an ESD event resulting from contact with the human body. The model consists of a 100pF storage capacitor that is charged to a high voltage, then discharged through a 1.5kΩ resistor. Figure 10 shows the current waveform when the storage capacitor is discharged into a low impedance.

IEC 61000-4-2 Contact Discharge

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2 due to lower series resistance. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is typically lower than that measured using the Human Body Model. Figure 11 shows the IEC 61000-4-2 model. The Contact Discharge method connects the probe to the device before the probe is charged. Figure 12 shows the current waveform for the IEC 61000-4-2 Contact Discharge Model.

ESD Test Conditions

ESD performance depends on a variety of conditions. Please contact Maxim for a reliability report documenting test setup, methodology, and results.

Applications Information

Data Transfer in USB Mode

Transmitting Data to the USB

To transmit data to the USB, operate the MAX3349EA in USB mode (see the *Operating Modes* section), and drive $\overline{OE}$ low. The MAX3349EA transmits data to the USB differentially on D+ and D-. VP and VM serve as differential input signals to the driver. When VP and VM are both driven low, a single-ended zero (SE0) is output on D+/D-.

Receiving Data from the USB

To receive data from the USB, operate the MAX3349EA in USB mode (see the *Operating Modes* section.) Drive $\overline{OE}$ high and SUS low. Differential data received at D+/D- appears as a logic signal at RCV. VP and VM are the outputs of single-ended receivers on D+ and D-.

Data Transfer in UART Mode

In UART mode, D+ is an input and D- is an output. UART signals on Tx are presented on D-, and signals on D+ are presented on Rx. The UART signaling levels for D+/D- are determined by V_{UART}. The voltage thresholds for Rx and Tx are determined by V_L. The voltage thresholds for D+ and D- are determined by V_{UART}.

Power-Supply Decoupling

Bypass V_{BUS}, V_L, and V_{UART} to ground with 0.1µF ceramic capacitors. Additionally, bypass V_{TRM} to ground with a 1µF ceramic capacitor. Place all bypass capacitors as close as possible to the device .

Timing Diagrams

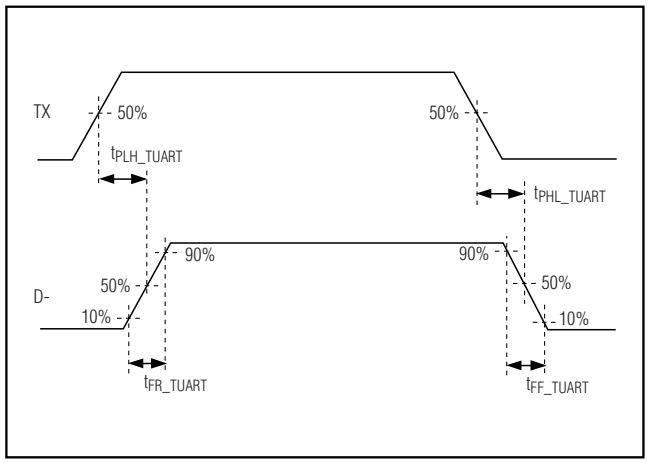


Figure 13. UART Transmitter Timing

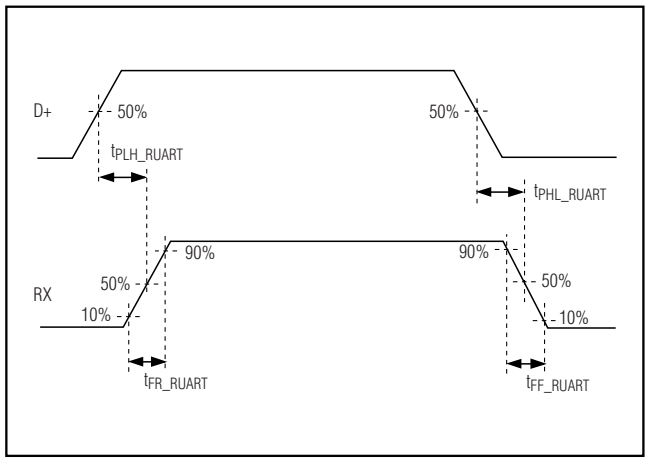


Figure 14. UART Receiver Timing

Power Sequencing

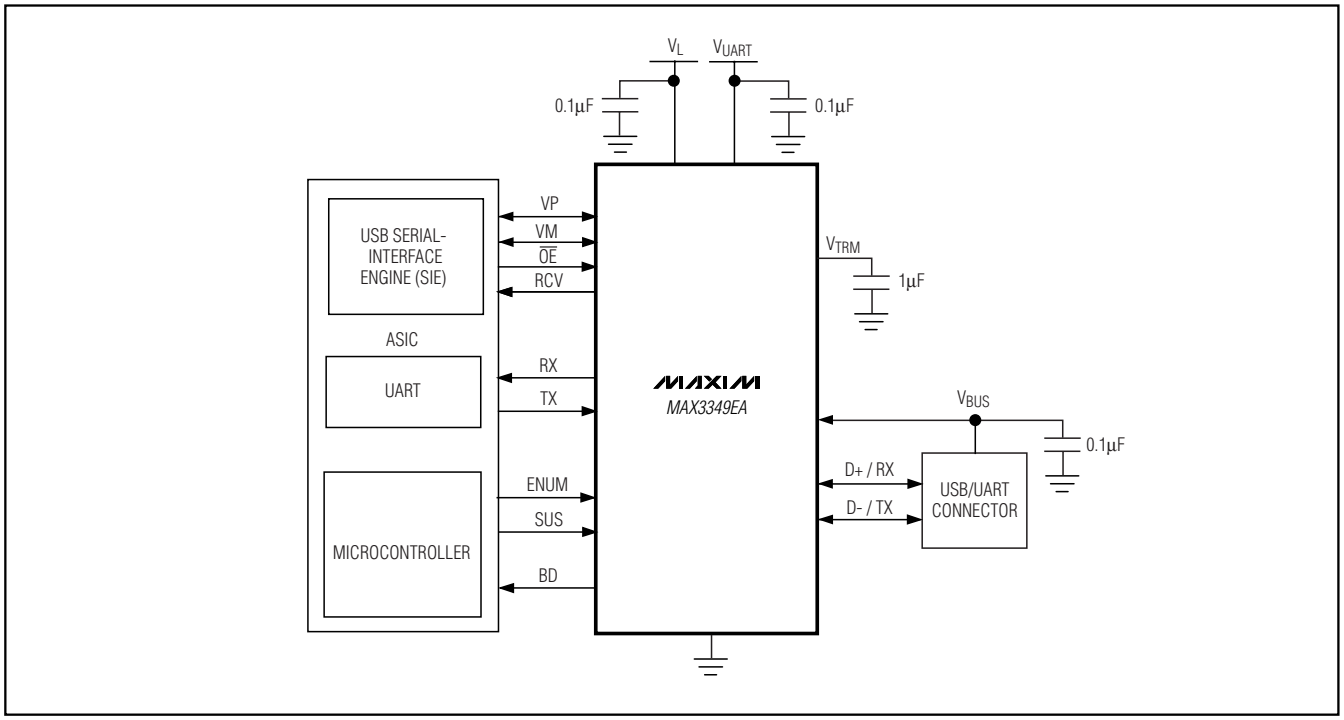
There are no power-sequencing requirements for V_L, V_{UART}, and V_{BUS}.

UCSP Application Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit-board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note *UCSP- A Wafer-Level Chip-Scale Package* available on Maxim's website at www.maxim-ic.com/ucsp.

USB 2.0 Full-Speed Transceiver with UART Multiplexing Mode

Typical Operating Circuit

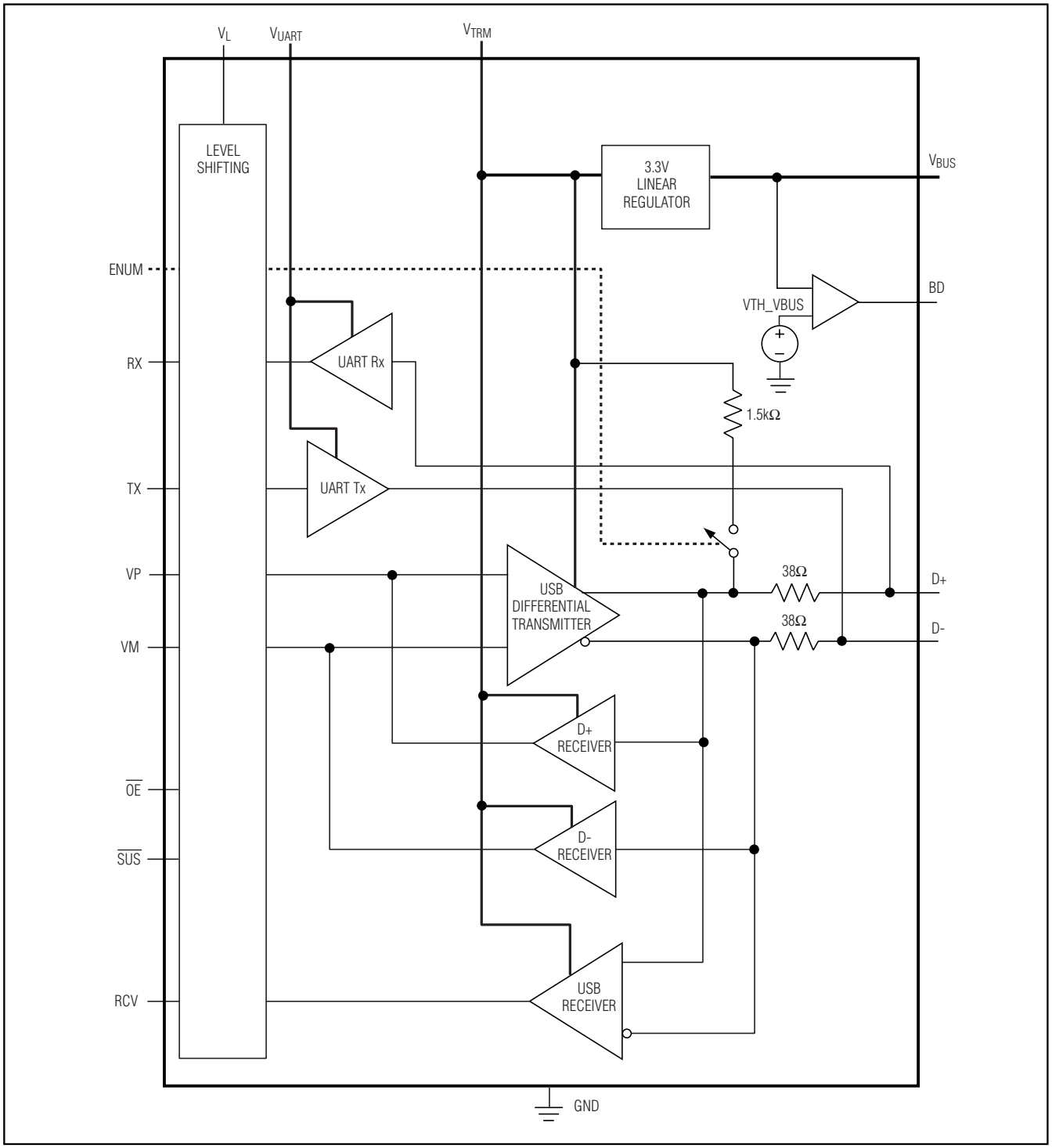


Chip Information

PROCESS: BiCMOS

USB 2.0 Full-Speed Transceiver with UART Multiplexing Mode

Functional Diagram

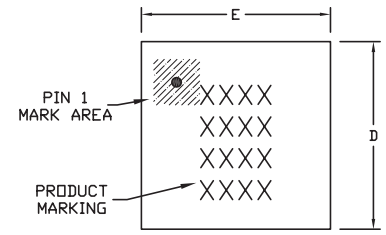


USB 2.0 Full-Speed Transceiver with UART Multiplexing Mode

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

16L,UCSP.EPS

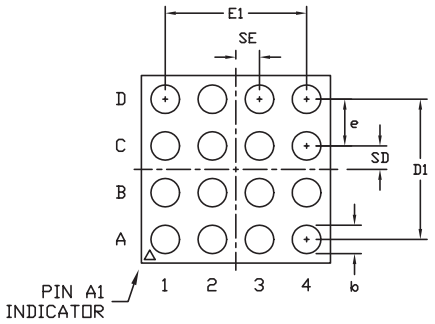


TOP VIEW

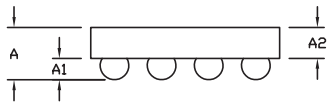
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B16-1	2.02±0.05	2.02±0.05	NONE
B16-2	2.02±0.05	2.02±0.05	B3, C3
B16-3	2.02±0.05	2.02±0.05	B3, C2
B16-4	2.02±0.05	2.02±0.05	B2, C3
B16-5	2.02±0.05	2.02±0.05	B2, B3, C2, C3
B16-6	2.02±0.05	2.02±0.05	C3

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM

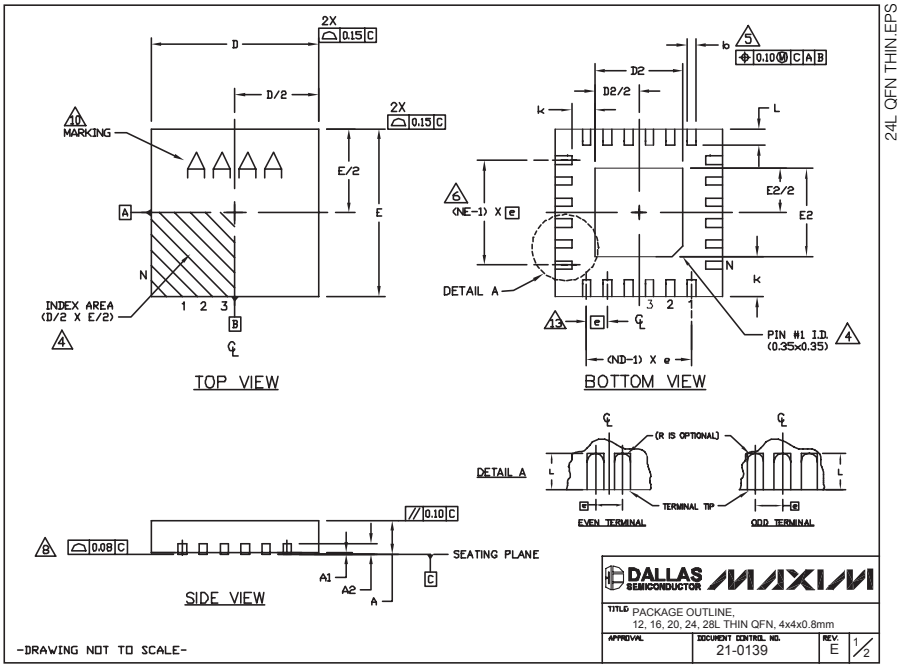
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 4x4 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0101	H	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0139
REV. E
2/2