

MN64672

A/D and D/A Converter for Digital Audio Equipment

■ Overview

The MN64672 is a 2-channel 16-bit A/D and D/A converter for digital audio equipment. It has a built-in digital filter and reference voltage generator, and uses a noise-shaping system. This device is suitable for applications such as MD and DAT players, and musical instruments. The D/A conversion section employs a switched capacitor system, minimizing the effects of clock jitter. Two modes are available: A/D conversion + simple D/A conversion mode, and D/A conversion mode.

■ Features

- Mixed analog/digital CMOS LSI for a single 3V power supply
- In A/D converter mode:
A/D conversion, D/A conversion (double oversampling digital filter, no de-emphasis function)
- In D/A converter mode:
D/A conversion (8-fold oversampling digital filter, de-emphasis function)
- Switchable between signal processing LSI format and I²S format, two's-complementary input/output
- Supports 256f_s and 384f_s system clock
- No zero-cross distortion

D/A converter section:

- Noise-shaping type D/A conversion, with built-in 8-fold oversampling digital filter
- High clock jitter tolerance (almost no degradation of characteristics due to clock jitter)
- Digital deemphasis function (for f_s=32 kHz, 44.1 kHz, or 48 kHz)

(In D/A conversion mode only)

- Digital attenuator (for microcontroller interface)

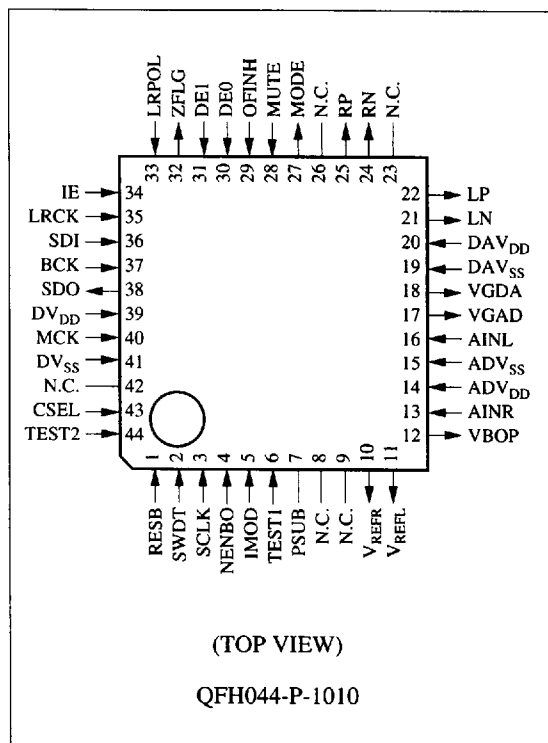
A/D converter section:

- 64-fold oversampling noise-shaping type A/D conversion
 - Sample-and-hold circuit unnecessary.
 - Built-in overflow limiter
 - SDO pin tri-state function
- In D/A conversion mode (MODE: 1)

■ Applications

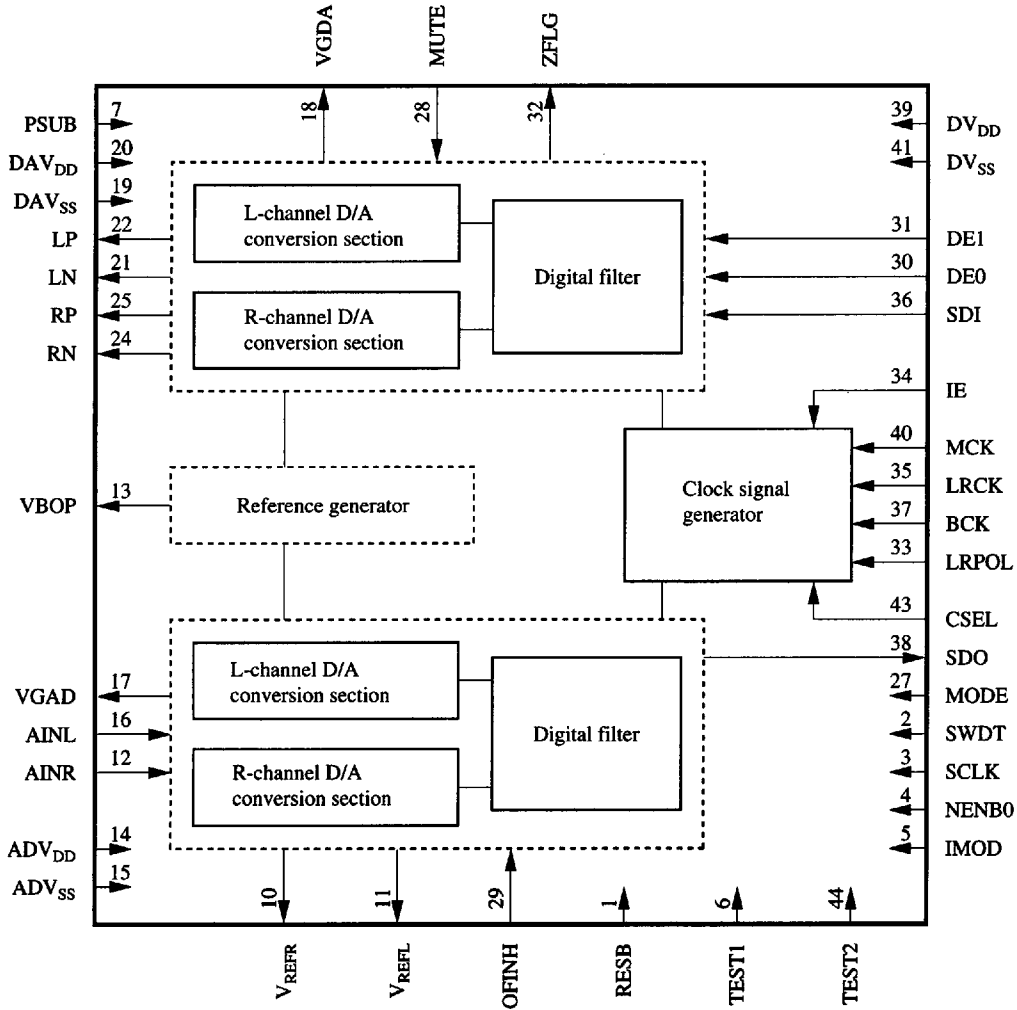
- Digital audio equipment in general, including MD and DAT players and musical instruments

■ Pin Arrangement



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■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description	
1	RESB	I	Reset pin	"0": Reset
2	SWDT	I/O	Normal input	Microcomputer I/F
3	SCLK	I/O	Normal input	Microcomputer I/F
4	NENBO	I/O	Normal input	Microcomputer I/F
5	IMOD	I/O	Normal input	Microcomputer I/F
6	TEST1	I	Test pin	Connect to 0 V
7	PSUB		Substrate voltage pin	Connect to 0 V
8	N.C.	—	No connection	
9	N.C.	—	No connection	
10	V _{REFR}	O	R-channel ADC reference voltage pin	Connect a 22μF capacitor to VGAD.
11	V _{REFL}	O	L-channel ADC reference voltage pin	Connect a 22μF capacitor to VGAD.
12	VBOP	O	Reference voltage pin for analog section	Connect a 1μF capacitor to VGAD.
13	AINR	I	R-channel ADC analog signal input pin	
14	ADV _{DD}	I	ADC analog section power supply pin	Connect to +3 V
15	ADV _{SS}	I	ADC analog section ground pin	Connect to 0 V
16	AINL	I	L-channel ADC analog signal input pin	
17	VGAD	O	ADC section reference voltage pin	Connect a 22μF capacitor to V _{SS}
18	VGDA	O	DAC section reference voltage pin	Connect a 22μF capacitor to V _{SS}
19	DAV _{SS}		DAC analog section ground pin	Connect to 0 V
20	DAV _{DD}		DAC analog section ground pin	Connect to +3 V
21	LN	O	L-channel DAC inverted output pin	
22	LP	O	L-channel DAC normal output pin	
23	N.C.	—	No connection	
24	RN	O	R-channel DAC inverted output pin	
25	RP	O	R-channel DAC normal output pin	
26	N.C.	—	No connection	
27	MODE	I	ADC/DAC operating mode switching pin	"0": ADC, "1": DAC
28	MUTE	I	DAC mute pin	"1": Mute
29	OFINH	I	ADC offset elimination circuit stop pin	"1": Hold
30	DE0	I	DAC digital de-emphasis switching pins DE1, DE0=01: OFF, 11:32kHz, 00:44.1kHz, 10:48kHz	
31	DE1	I		
32	ZFLG	O	DAC ∞ 0 input detection signal output pin	"1": ∞ 0 detection
33	LRPOL	I	LRCK polarity switching pin	"0": LRCK=0 Lch. "1": LRCK=0 Rch
34	IE	I	Serial data format switching pin	"0": Signal processing LSI format, 1: I ² S
35	LRCK	I	LR clock input pin	
36	SDI	I	DAC serial data input pin	

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■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
37	BCK	I	Bit clock input pin
38	SDO	O	ADC serial data output pin
39	DV _{DD}	I	Power supply pin for digital section Connect to +3 V
40	MCK	I	Master clock input pin
41	DV _{SS}	I	Ground pin for digital section Connection 0 V
42	N.C.	—	No connection
43	CSEL	I	Master clock frequency selection pin "0": 256f _s , "1": 384f _s
44	TEST2	I	Test pin Connect to +3 V

■ Conversion Characteristics

ADC Analog Characteristics

AV_{DD}=DV_{DD}=3.0V, AV_{SS}=DV_{SS}=PSUB=0V, Ta=25°C, f_{MCK}=11.2896MHz, CSEL="0"

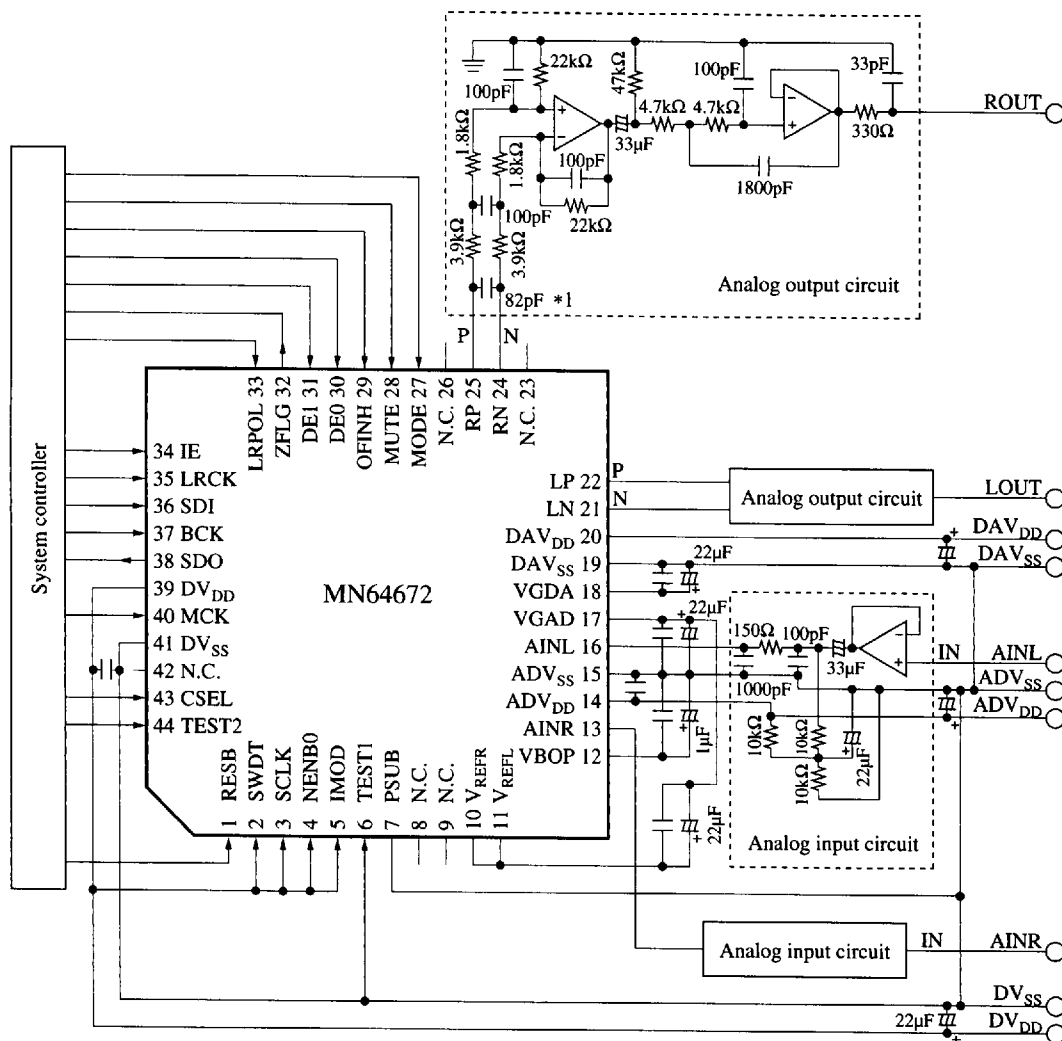
Parameter	Symbol	Test Conditions	min	typ	max	Unit
Signal-to-noise ratio	D.R.	EIAJ (1kHz)	85	91		dB
Dynamic range	D.R.	EIAJ (1kHz)	85	91		dB
Total harmonics distortion	THD+N	EIAJ (1kHz)		0.015	0.06	%
Channel separation	α	(1kHz)	72	84		dB

DAC Analog Characteristics

AV_{DD}=DV_{DD}=3.0V, AV_{SS}=DV_{SS}=PSUB=0V, Ta=25°C, f_{MCK}=11.2896MHz, CSEL="0"

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Signal-to-noise ratio	S/N	EIAJ (1kHz)	91	94		dB
Dynamic range	D.R.	EIAJ (1kHz)	88	92		dB
Total harmonics distortion	THD+N	EIAJ (1kHz)		0.012	0.03	%
Channel separation	α	(1kHz)	72	86		dB

Application Circuit Example



Notes

- 1: Capacitors without specified value are 0.1μF ceramic capacitors.
- 2: The optimal value of this capacitance (*1) depends on the wiring length. A value between 36 pF and 100 pF should be used.

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■ Package Dimensions (Unit: mm)

QFH044-P-1010

