Programmable Peripheral

PSD813FN/FH

Field-Programmable Microcontroller Peripherals with Flash Memory and Embedded Micro⇔Cells™

Preliminary

Introduction

The PSD813FH and PSD813FN devices are field-programmable microcontroller (MCU) peripherals with Flash memory. These multi-chip modules (MCM) are the first two members of a complete family of in-system-programmable (ISP) peripherals from WSI that enhance any embedded microcontroller design. These devices will interface easily with most popular MCUs and enable a simple two-chip solution that addresses virtually all of the MCUs external needs. Major features provided by the PSD813FH/FN are large Flash memory, concurrent OTP boot memory, battery backed SRAM, programmable I/O, programmable logic, address space expansion, power management, code security, and small package size.

A two-chip solution consisting of an MCU and a PSD813FN/FH reduces design and manufacturing cost, reduces board space, lowers power consumption, and shortens time-to-market while increasing design flexibility. In addition, in-system features such as concurrent Flash read and write capability, dynamically reconfigurable I/O ports, and low power management increases system performance and manufacturing flexibility.

New innovative **"microcontroller-macrocells"**, called Micro⇔Cells™, bring inexpensive programmable logic to MCU-based embedded system designs. Because the Micro⇔Cells are directly connected to the MCU address/data bus, their programmable logic is tightly coupled to the MCU software with no hardware overhead. The MCU's ability to communicate directly with the Micro⇔Cells at the flip-flop level makes PSD813FN/FH devices ideal for popular functions such as counters, serial channels, and mailboxes. When compared to industry standard CPLD implementation, this architecture can save 25% to 50% of the CPLD product term and macrocell resources.

The PSD813FN/FH devices are the first of WSI's Flash PSD8XXF product family. Starting with the PSD813FN/FH, a pin-for-pin upgrade path exists for future lower cost monolithic PSD8XXF devices that will incorporate expanded Flash-based programmable logic, Flash and EEPROM memory types, larger SRAM, and serial ISP using the industry standard JTAG protocol.

Key Features

- ❑ **MCM 5-volt only Flash Programmable Peripheral for Microcontroller-based Applications**
- ❑ **Solves Problems of In-System Flash Erase and Programming**
  - – Concurrently Operating Main Memory and Boot Memory
  - – Resolves Microcontroller Decoding Issues During Flash Update
- ❑ **Two separate non-volatile memory arrays.**

  Both 1 Mbit (128 Kbytes) of Flash memory and 256 Kbits (32 Kbytes) of Separate OTP Boot EPROM memory are available. The Boot memory allows continuous operation of the MCU while the Flash memory is being written or erased. The Flash memory is divided into eight 16 Kbyte sectors that can be mapped to different address spaces. Access time is 150 ns which includes address latching and DPLD decoding.
- ❑ **Embedded On-Chip Erase and Program Algorithms for the Flash Memory.**

  Automatically accommodates on-chip events for writing and erasing the Flash memory. The Flash memory is byte-programmable and can be erased sector by sector or by entire chip. The embedded algorithms indicate completion of program or erase cycles by using two popular methods: data polling or bit toggling. PSD813FN/FH algorithms are compatible with the standard JEDEC single-power-supply Flash command set.

Key Features (cont.)

- **Low V_{CC} write inhibit <= 3.2 V for the Flash Memory.**
- **Guaranteed Minimum 10,000 Erase/Write Cycles.**
- A simple, programmable interface to 8-bit microcontrollers using either multiplexed or non-multiplexed busses. The bus interface logic directly decodes microcontroller control signals. Supports all popular microcontrollers.
- **Three Flexible OTP PLD Sections**
  One PLD is used for internal PSD address decoding, one is used for external device address decoding, and one is used as a general-purpose design resource. The general-purpose PLD may be used to efficiently implement a variety of logic functions commonly associated with MCUs such as state machines, address decoders, address generators, serial channels, multiprocessor mailboxes, and shift registers.

  The general-purpose PLD also supports 12-Output Micro⇔Cells and 23-Input Micro⇔Cells. The MCM PSD813FN/FH dedicates seven Output and eight Input Micro⇔Cells to Flash memory usage and SRAM standby voltage control. Although the seven Output Micro⇔Cells are dedicated, an internal product term allocator redistributes any unused product terms if needed by the remaining Micro⇔Cells.
- Internal 4Kbit SRAM. The SRAM retains data if power is lost by automatically switching to an external standby power source.
- Nineteen individually configurable I/O Port Pins. The Ports may be used as microcontroller I/Os, PLD I/Os, latched microcontroller address outputs or special function I/Os.
- The programmable Power Management Unit (PMU) supports two separate, low-power modes allowing operations with as little as 25µA (at 5V V_{CC}). The device can automatically detect a lack of microcontroller activity and put the PSD into power down mode.
- **Page Logic**
  Page Logic is connected to the ZPLDs and enables address space expansion for microcontrollers with limited address space capability. Up to 16 pages are available.
- **Security Bit**
  The security bit prevents reading the PSD configuration, ZPLD, EPROM Boot array, and Flash memory contents. This inhibits copying the device on a programmer.
- **Development Tools**
  Supported by the PSDsoft™ MS-Windows® compatible development tools. Includes PSDabel as the design entry method, an efficient Fitter, and an Address Translator (see Figure 2).
- Packaging consists of a 52 pin plastic chip carrier.

Please refer to the revision block at the end of this document for updated information.

PSD813FN/FH Architectural Overview

PSD813FN/FH devices consist of several major functional blocks. Figure 1 shows the architecture of the PSD813FN/FH device. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions, and are user configurable.

PLDs

The device contains three PLD blocks each optimized for a different function as shown in Table 1. The functional partitioning of the PLDs reduces power consumption, optimizes cost/performance and ease of design entry.

The Decode PLD (DPLD) is used to decode and generate chip selects for the PSD813FN/FH internal memory, registers, and peripheral I/O mode. The External Chip Select PLD (ECSPLD) is optimized to generate chip selects for devices external to the PSD813FN/FH. The General Purpose PLD (GPLD) can implement user defined logic functions. The DPLD and ECSPLD have combinatorial outputs while the GPLD has 12 Output Micro⇔Cells. Seven of the Port C Micro⇔Cells are dedicated to Flash memory control. The PSD813FN/FH also has 23 Input Micro⇔Cells that can be configured as inputs to the PLD. The PLDs receive their inputs from the PLD Input bus.

I/O Ports

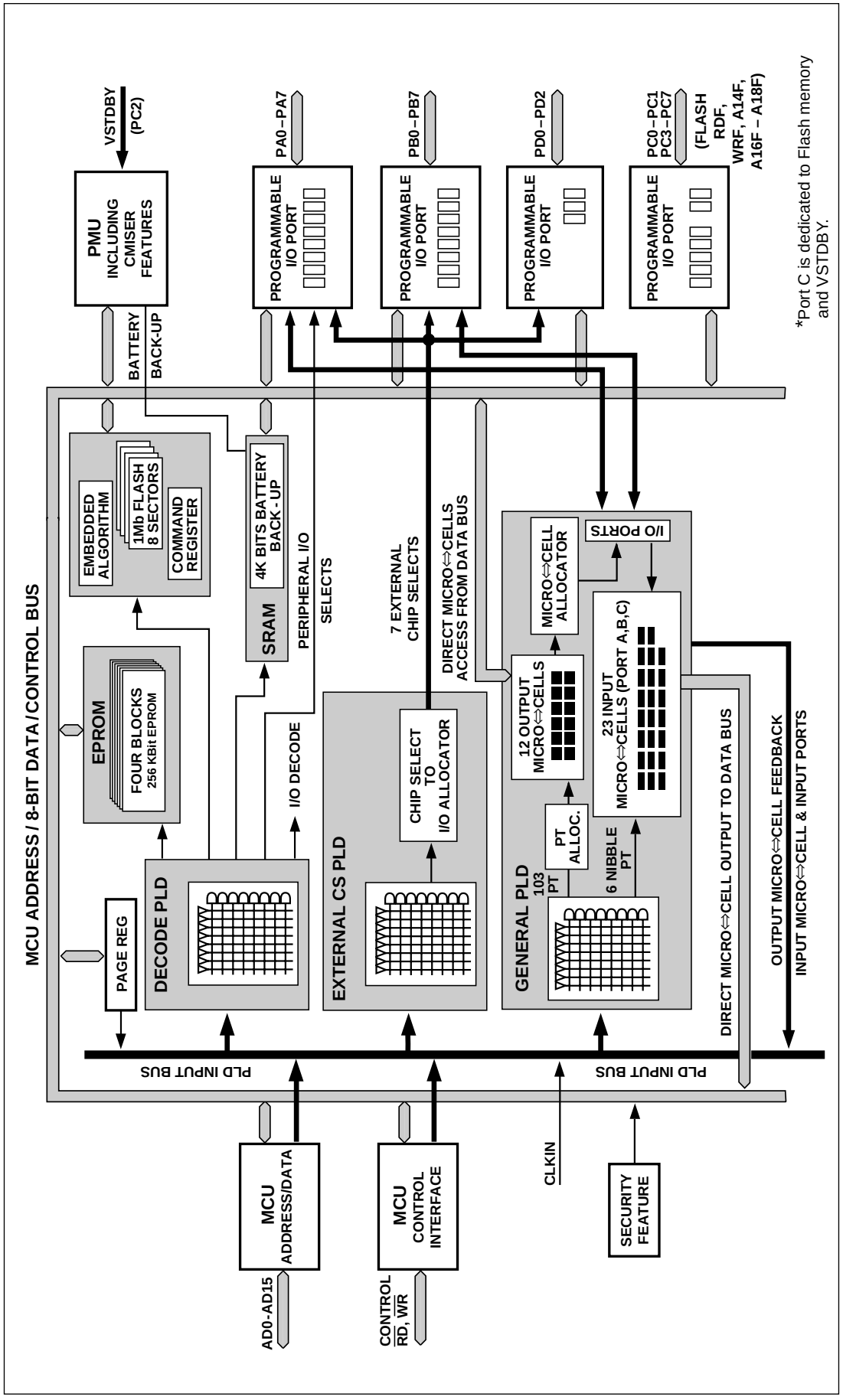
The PSD813FN/FH has 19 I/O pins divided among three ports. Each I/O pin can be individually configured to provide many functions. Ports A, B and D can be configured as standard MCU I/O ports, PLD I/O, or latched address outputs for microcontrollers using multiplexed address/data busses.

Table 1.

Name	Abbreviation	Inputs	Outputs	Product Terms
Decode PLD	DPLD	63	12	13
External Chip Select PLD	ECSPLD	24	7	7
General PLD	GPLD	63	12	109

PSD813FN/FH Architectural Overview (cont.)

Figure 1. PSD813FN/FH Block Diagram



PSD813FN/FH Architectural Overview (cont.)

Microcontroller Bus Interface

The PSD813FN/FH easily interfaces with most popular eight and sixteen-bit microcontrollers with either multiplexed or non-multiplexed address/data busses. The PSD813FH is for multiplexed applications and the PSD813FN is for non-multiplexed applications. The PSD813FN/FH can operate with 16-bit MCUs if the MCU is configured for 8-bit external data path mode. The device is configured to respond to the microcontroller control signals which are also used
as inputs to the PLDs.

Memory

The PSD813FN/FH contains a 1 Mbit Flash memory, a 256 Kbit Boot EPROM and a 4 Kbit SRAM. The EPROM space and Flash memory space are divided into four and eight equally sized blocks, respectively. Each block can be located in a different address space defined by the user. The access time of either memory includes the address latching and DPLD decoding. The Flash memory is implemented using a 4 Mbit (29040) device configured as a 1 Mbit memory. All the commands for the 29040 are applicable for operating as a 1 Mbit Flash memory.

The 4 Kbit SRAM may be used as a scratch pad memory and an extension of the microcontroller SRAM. The SRAM data is retained in the event of a system power down, provided a backup battery is connected to the Vstby pin (PC2). Switching from the V_{CC} supply to standby power occurs automatically when V_{CC} drops below Vstby voltage.

Page Register

The four-bit Page Register expands the address range of the microcontroller by sixteen times. The paged address can be used as part of the address space to access external memory and peripherals or internal EPROM, SRAM and I/O.

Power Management Unit

The Power Management Unit (PMU) in the PSD813FN/FH enables the user to control the power consumption on selected functional blocks based on system requirements. The PMU includes an Automatic Power Down unit (APD) that will turn off device functions due to microcontroller inactivity in one of two modes: the Power Down mode and Sleep mode.

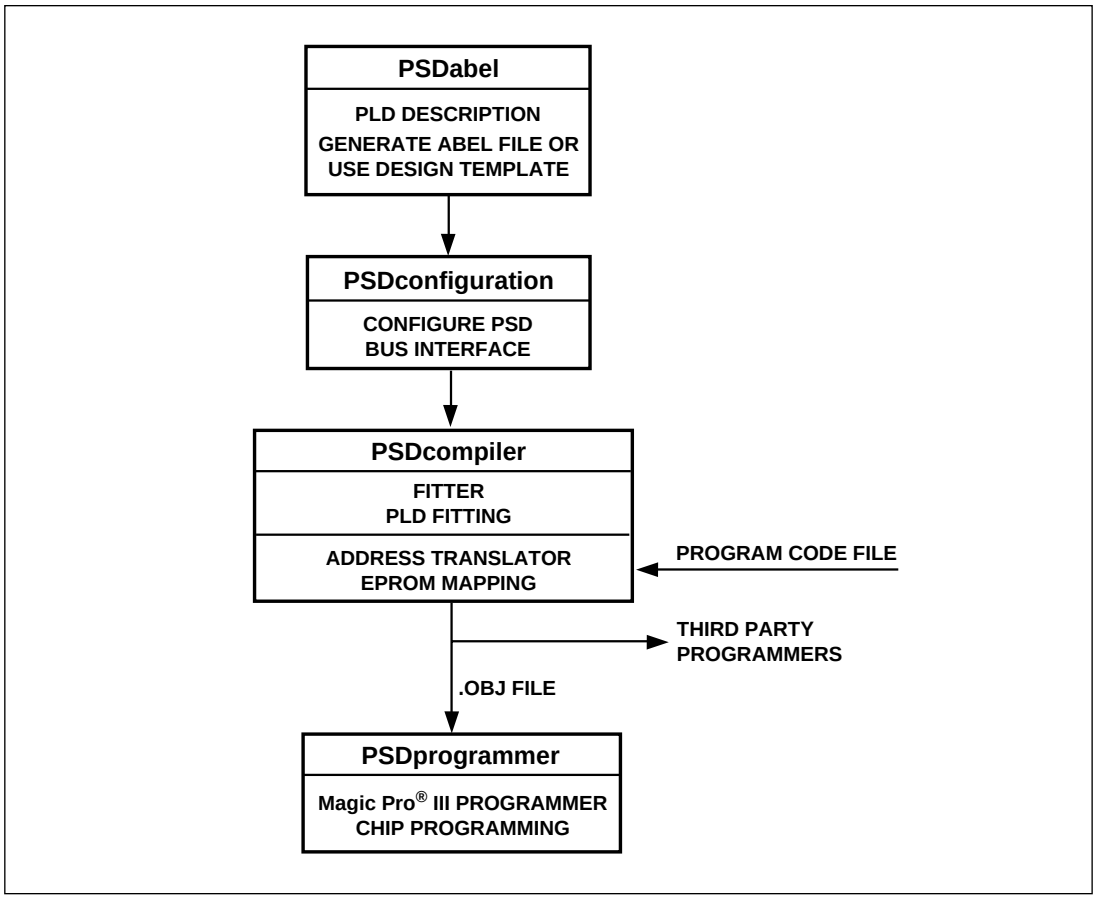
Other power saving features, such as the CMiser in the PMU, allow the EPROM/SRAM to operate at a slower rate to conserve power.

Development System

The PSD813FN/FH devices are supported by the Windows-based PSDsoft Development System. The PSDsoft design flow is shown in Figure 2. The PLD design entry is done using PSDabel, which creates a minimized logic implementation, and provides logic simulation of the PLDs. The PSD813FN/FH Bus Interface and I/O Port configuration are entered in PSDconfiguration.

The PSDcompiler, comprised of a fitter and address translator, generates an object file from the PSDabel, PSDconfiguration and MCU code files. The object file is then down loaded to a programmer (MagicPro III, Data I/O, or other third party programmer for device programming).

Figure 2. PSDsoft Development Tools



PSD813FN/FH Devices

The PSD813FN/FH are two unique devices. The part classifications are based on bus mode. The features of each part are listed in Table 2.

Table 2. PSD813FN/FH Product Matrix

Part #	Bus Bit	ZPLD DPLD + GPLD + ECSPLD		I/O Pins	PMU	Flash Memory K Bit	SRAM K Bit	Boot EPROM K Bit
		Inputs	Registered Micro⇔cells					
PSD813FH	x8/MUX	63	12	19	Yes	1024	4	256
PSD813FN	x8/Non-MUX	63	12	19	Yes	1024	4	256

NOTE: PMU = Power Management Unit.

Table 3. PSD813FN/FH Pin Descriptions

The following table describes the pin names and pin functions of the PSD813FN/FH. Pins that have multiple names and/or functions are defined by configuration.

Pin Name	Pin	Type	Function Description
ADIO0–7	30–37	I/O	Address/Data Port, interface to Microcontroller Bus 1. Input pins for multiplexed low order address/data byte. ALE or AS latches address A0-7 for input to PLDs. The PSD drives data out only if read is active and one of the internal PSD functional blocks is selected.
A8–15	39–46	I/O	Address Port, interface to Microcontroller Bus 1. Address A8-15 inputs.
CNTL0 ($\overline{WR}$, R_$\overline{W}$)	47	I	Write Input pin with multiple configurations. Depending on the MCU interface selected, this pin can be: 1. $\overline{WR}$ – active low write input 2. R_$\overline{W}$ – read/write pin, low for write bus cycle 3. Control signal (CNTL0) input to PLD
CNTL1 ($\overline{RD}$, E, DS)	50	I	Read or Data Strobe Input pin with multiple configurations. Depending on the MCU interface selected, this pin can be: 1. $\overline{RD}$ – active low read input 2. E – E clock input. During a write bus cycle, E is high and R/W is low During a read bus cycle, E is high and R/W is high 3. $\overline{DS}$ – Data Strobe, active low 4. Control signal (CNTL1) input to PLD
CNTL2 ($\overline{PSEN}$)	49	I	Read or other Control input pin with multiple configurations. Depending on the MCU interface selected, this pin can be: 1. $\overline{PSEN}$ – Program Select enable, active low in code fetch bus cycle 2. Control signal (CNTL2) input or general input to PLD
$\overline{Reset}$	48	I	Active low input. Resets I/O Ports, PLD Micro⇔Cells and some of the Configuration Registers. Must be active at power up.
PA0 PA1 PA2 PA3	29 28 27 25	I/O	Port A, PA0 – 3. This port is pin configurable and has multiple functions: 1. MCU I/O – standard output or input port 2. External chip select (ECSPLD) output, or input to GPLD 3. Latched address outputs (see Table 4) 4. As Data Bus Port (D0–3) in non-multiplexed bus configuration 5. Peripheral I/O mode

Table 3. PSD813FN/FH Pin Descriptions (cont.)

Pin Name	Pin	Type	Function Description
PA4 PA5 PA6 PA7	24 23 22 21	I/O CMOS or Open Drain	Port A, PA4–7. This port is pin configurable and has multiple functions: 1. MCU I/O – standard output or input port 2. GPLD Micro⇔Cell (McellAB) output or input 3. Latched address outputs (see Table 4) 4. As Data Bus Port (D4–7) in non-multiplexed bus configuration 5. Peripheral I/O mode
PB0 PB1 PB2 PB3	7 6 5 4	I/O	Port B, PB0–3. This port is pin configurable and has multiple functions: 1. MCU I/O – standard output or input port 2. External chip select (ECSPLD) output, or input to GPLD 3. Latched address outputs (see Table 4)
PB4 PB5 PB6 PB7	3 2 52 51	I/O CMOS or Open Drain	Port B, PB4–7. This port is pin configurable and has multiple functions: 1. MCU I/O – standard output or input port 2. GPLD Micro⇔Cell (McellAB) output or input 3. Latched address outputs (see Table 4)
PC0 ($\overline{WRF}$) PC1 ($\overline{RDF}$) PC3 (A14F) PC4 (A16F) PC5 (A17F) PC6 (A18F) PC7 ($\overline{CFS}$)	20 19 17 14 13 12 11	* 	Flash Write Flash Read Flash Address A14 Flash Address A16 Flash Address A17 Flash Address A18 Flash Select
PC2 (Vstby)	18	I	Port C pin PC2. Dedicated SRAM Standby Voltage Input. Pin should be grounded if Vstby is not required.
PD0 (ALE)	10	I/O	Port D Pin PD0 can be configured as: 1. ALE input - latches addresses on ADIO0–15 pins 2. MCU I/O 3. GPLD input 4. ECSPLD output
PD1 (CLKIN)	9	I/O	Port D Pin PD1 can be configured as: 1. MCU I/O 2. GPLD input 3. External chip select (ECSPLD) output 4. CLKIN clock input – clock input to the GPLD Micro⇔Cells, the APD power down counter and GPLD AND Array

*These pins are reserved for internal Flash memory control and should not be used as outputs.

Table 3. PSD813FN/FH Pin Descriptions (cont.)

Pin Name	Pin	Type	Function Description
PD2 ($\overline{CSI}$)	8	I/O	Port D Pin PD2 can be configured as: 1. MCU I/O 2. GPLD input 3. External (ECSPLD) output 4. $\overline{CSI}$ input – When low, the $\overline{CSI}$ enables the PSD EPROM/SRAM. When high, the EPROM/SRAM are disabled to conserve power
V_{CC}	15 38		Power pins
GND	1 16 26		Ground pins

Table 4. I/O Port Latched Address Output Assignments*

Microcontroller	Port A (3:0)	Port A (7:4)	Port B (3:0)	Port B (7:4)
8-Bit Multiplexed Bus	Address [3:0]	Address [7:4]	Address [3:0]	Address [7:4]
8-bit Non-Multiplexed Bus	N/A	N/A	Address [3:0]	Address [7:4]

N/A = Not Applicable

*Refer to the I/O Port Section on how to enable the Latched Address Output function.

PSD813FN/FH Register Description and Address Offset

Table 5 shows the offset address to the PSD813FN/FH registers relative to the CSIOP base address. The CSIOP space is the 256 bytes of address that is allocated by the user to the internal PSD813FN/FH registers.

Table 5. Register Address Offset

Register Name	Port A	Port B	Port C	Port D	Other*	Description
Data In	00	01	10	11		Reads Port pin as input, MCU I/O input mode
Control	02	03				Selects mode between MCU I/O or Address Out
Data Out	04	05	12	13		Stores data for output to Port pins, MCU I/O output mode
Direction	06	07	14	15		Configures Port pin as input or output
Drive	08	09	16	17		Configures Port pin between CMOS, Open Drain and Slew rate
Input Micro⇔Cell	0A	0B	18			Reads Input Micro⇔Cell
Enable Out	0C	0D	1A			Reads the status of the output enable to the I/O Port driver
Output Micro⇔Cell	20	20	21			Read – reads output of Micro⇔Cells (McellC, McellAB) Write – loads Micro⇔cell Flip-Flops
PMMR0					B0	Power Management Register 0
PMMR1					B2	Power Management Register 1
Page					E0	Page Register
VM					E2	8031/PIO Configuration Register

*Other registers that are not part of the I/O ports.

The PSD813FN/FH Functional Blocks

The PSD813FN/FH consists of five major functional blocks:

- ***PLD Block***
- ***Bus Interface***
- ***I/O Ports***
- ***Memory Block***
- ***Power Management Unit***

The functions of each block are described in the following sections. Many of the blocks perform multiple functions, and are user configurable.

PLDs

The PLDs bring programmable logic functionality to the PSD813FN/FH. After specifying the logic for the PLDs by using the PSDabel tool in the PSDsoft suite, the logic configuration is programmed into the device and available when power is applied.

The PLDs (DPLD, ECSPLD and GPLD) consist of an AND array. The GPLD architecture includes 12 Output Micro⇔Cells in addition to the AND array. There are 23 Input Micro⇔Cells that can be configured as inputs to the PLD. Figure 3 shows the organization of the PLDs.

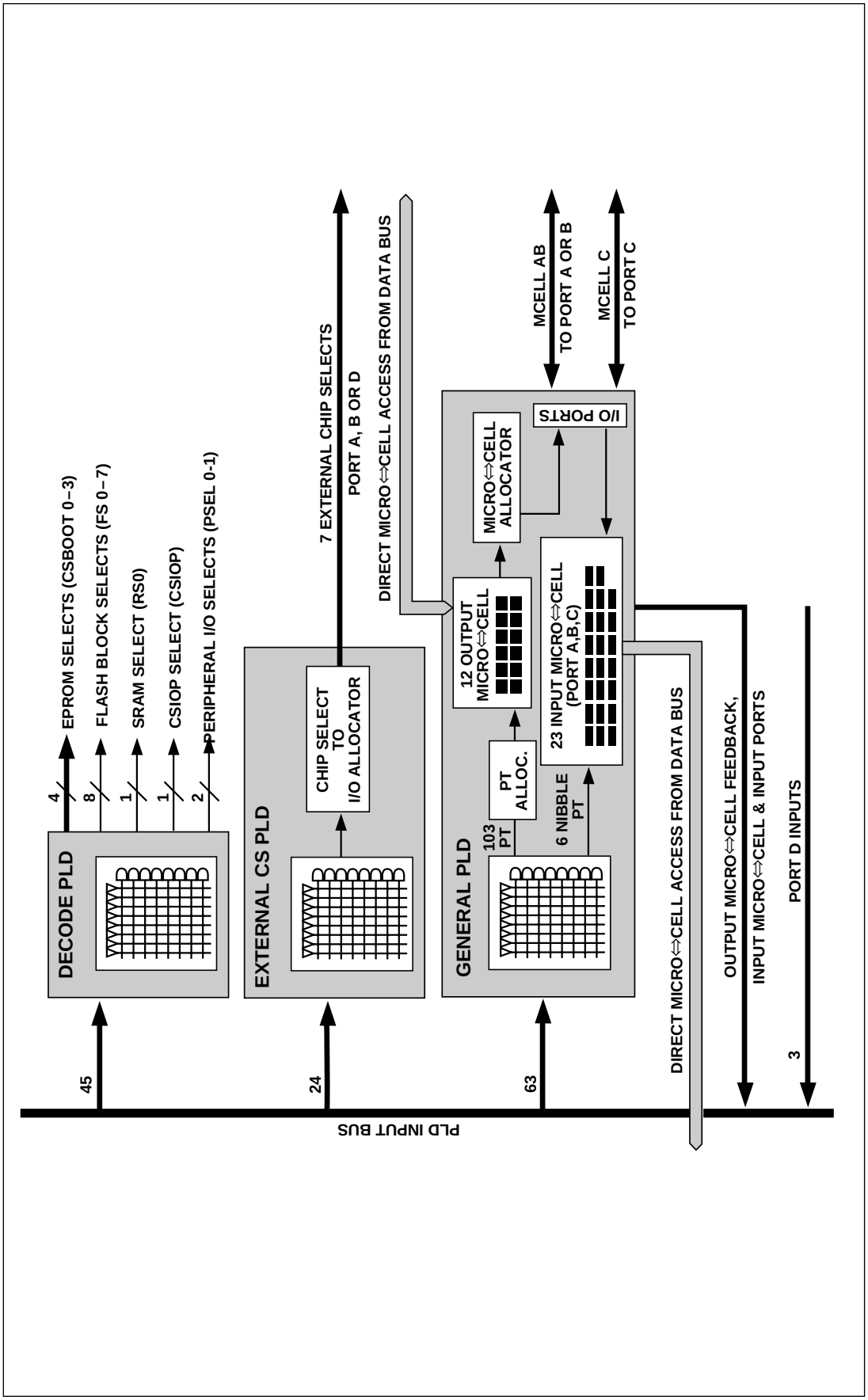
The AND array is used to form product terms specified using the PSDabel tool in the PSDsoft development system. When the inputs used in a term are true, the output is active. The GPLD Input Bus consists of 63 signals as shown in Table 6. Both the true and complement value of inputs are available to the AND array. The DPLD and ECSPLD Input Busses consists of fewer inputs and is a subset of the 63 inputs.

Table 6. GPLD Inputs

Input Source	Input Name	Number of Signals
MCU Address Bus	A[15:0]	16
MCU Control Signals	CNTL[2:0]	3
Reset	RST	1
Power Down	PDN	1
I/O Ports Inputs (Input Micro⇔Cells)	PA[7:0], PB[7:0] PC[7:3], PC[1:0]	23
Port D Inputs	PD[2:0]	3
Page Register	PGR[3:0]	4
Port A or B Micro⇔Cell Feedback	MCELLAB.FB[7:4]	4
Port C Micro⇔Cell Feedback	MCELLC.FB[7:0]	8

PLDs (cont.)

Figure 3. PLD Block Diagram



PLDs (cont.)

Each of the three PLDs has unique characteristics suited for its applications. They are described in the following sections.

Decode PLD

The Decode PLD (DPLD), shown in Figure 4, is used to select the internal PSD813FN/FH functions: Flash blocks, EPROM blocks, SRAM, Registers (CSIOP) and the Port A Peripheral Mode. All the select signals are active high and have one product term.

The CSIOP is the select line for the PSD813FN/FH internal registers that occupies 256 bytes of memory space. A second level decoder selects a register based on the address inputs A[7-0]. Each Flash memory sector has its own chip select.

The 128 Kbyte Flash memory is partitioned into eight 16 Kbyte blocks, each with its own decoded select line (FS0-FS7). The 32 Kbyte OTP boot memory is partitioned into four 8 Kbyte blocks, each with its own decoded select line (CSBOOT0-CSBOOT7).

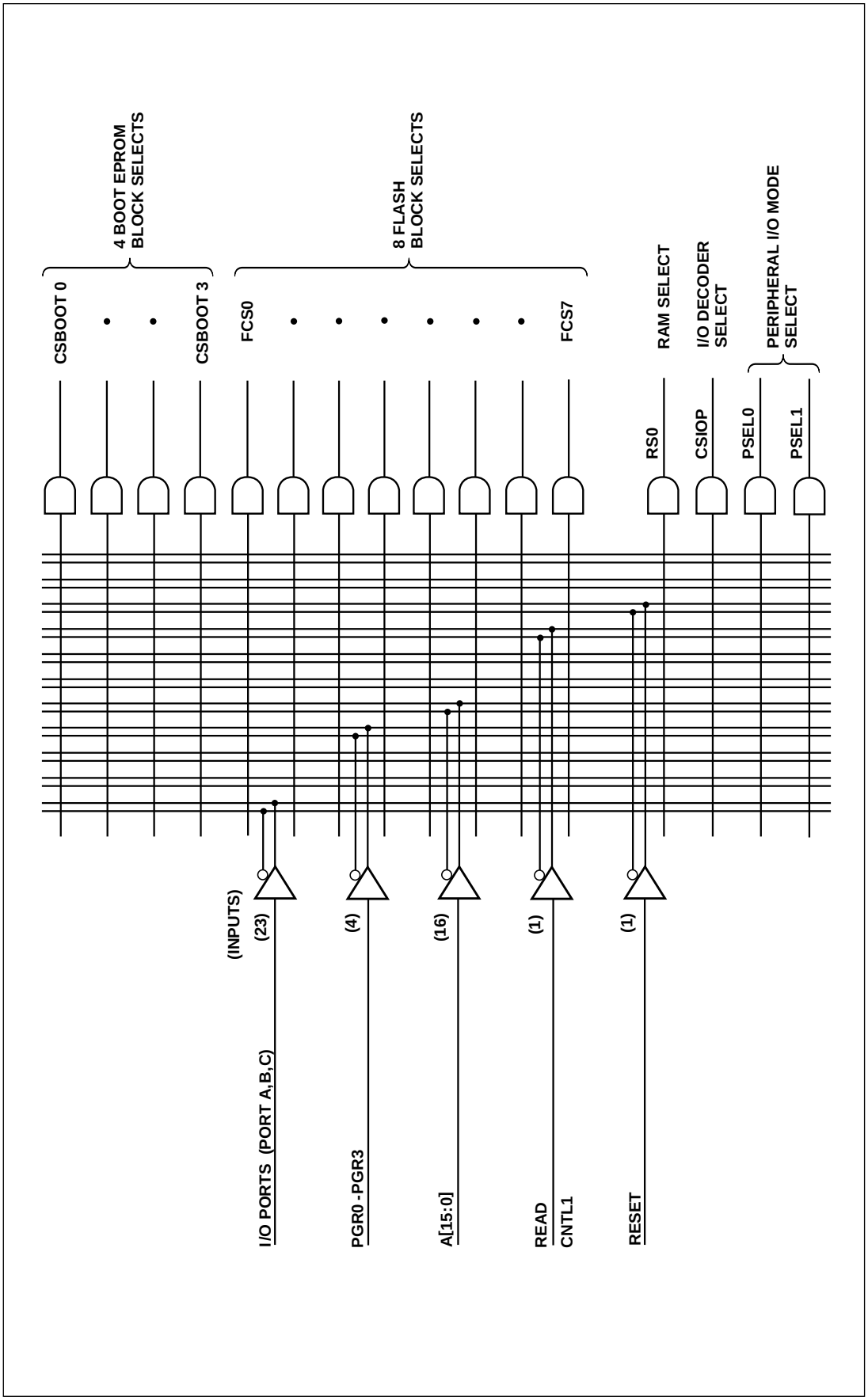
PSEL 0 & 1 are used as inputs to Port A to control the port's Peripheral I/O mode operation. Usually PSEL 0&1 are defined in term of the MCU address inputs. This mode is explained in the I/O Port section.

Table 7. DPLD Inputs

Input Source	Input Name	Number of Bits
MCU Address Bus	A[15:0]	16
I/O Ports Port A, B, C	PA[7:0], PB[7:0] PC[7:3], PC[1:0]	23
Page Register	PGR[3:0]	4
Control Signal	CNTL1 (Read)	1
Reset Pin	RST	1

PLDs (cont.)

Figure 4. DPLD Logic Array



PLDs (cont.)

External Chip Select PLD

The External Chip Select PLD (ECSPLD) provides the means to select external devices. The output buffer of the ECSPLD can be configured to operate in high slew rate by writing a “1” to the corresponding bit in the Drive Register. The slew rate is a measurement of the rise and fall times of the output. A higher slew rate means a faster output response while a lower slew rate is a slower response. Refer to Table 25 in the I/O Section for setting up the Drive Register.

Faster transitions are more likely to cause line reflections and system noise than slower rates. Adjusting the slew rate allows a trade-off between greater speed and noise sensitivity. The selection should be based on the performance requirements of the system and its noise characteristics. Set the corresponding bits in the Drive Register to “0” (for normal speed) or “1” (for fast drive). The default value is zero.

The ECSPLD has 24 inputs as shown in Table 8. Its outputs are combinatorial, of either polarity, and have one product term each as shown in Figure 5.

Table 8. ECSPLD Inputs

Input Source	Input Name	Number of Bits
MCU Address Bus	A[15:0]	16
MCU Control Signals	CNTL[2:0]	3
Power Down Signal	PDN*	1
Page Register	PGR[3:0]	4

*APD output. When PDN is high, the PSD813FN/FH is in power down mode

The seven ECSPLD outputs may be driven off the device through Ports A, B, or D, as shown in Table 9, via the Micro⇔Cell Allocator. Port selection is specified in the PSDabel file or assigned by the PSDcompiler.

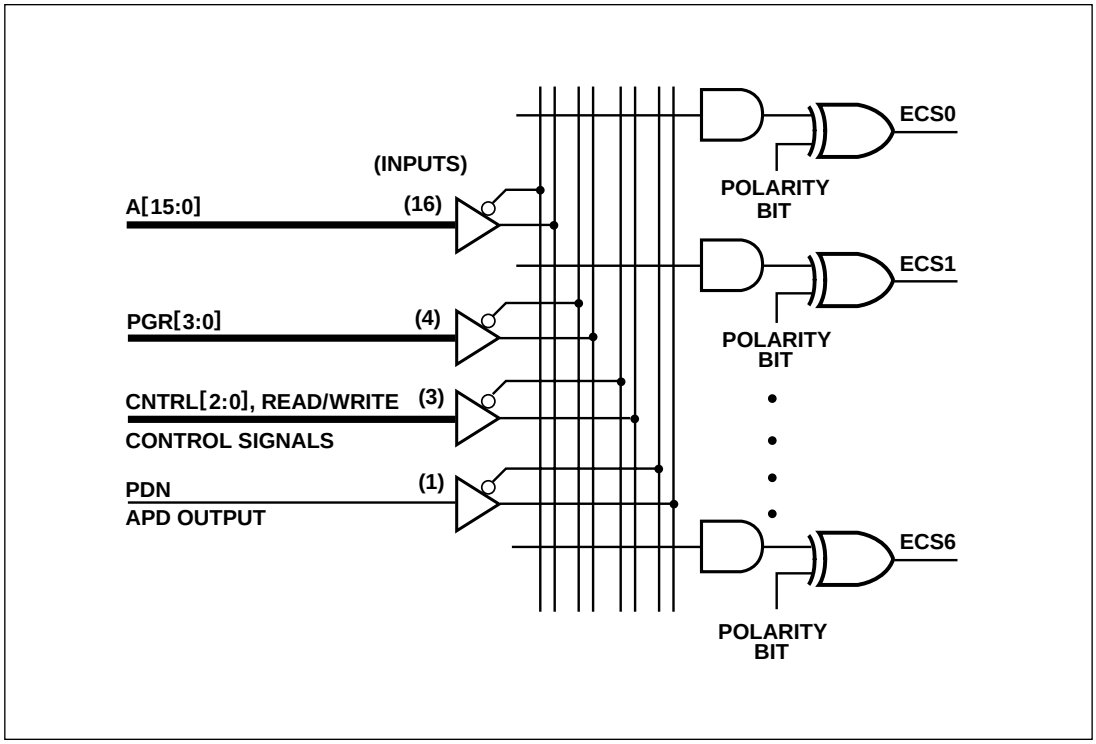
Table 9. ECSPLD Output Port Assignments

ECSPLD Output	Port A, B, or D Assignments
ECS0	PA0, PB0
ECS1	PA1, PB1
ECS2	PA2, PB2
ECS3	PA3, PB3
ECS4	PD0*
ECS5	PD1*
ECS6	PD2*

*Port D has no output enable (.oe) product terms for ECS4-6 outputs.

PLDs (cont.)

Figure 5. ECSPLD Logic Array



General PLD

The General PLD (GPLD) is used to implement system logic such as MCU loadable counters, system mailboxes or handshaking protocols. In addition, the GPLD can implement random logic and state machine functions.

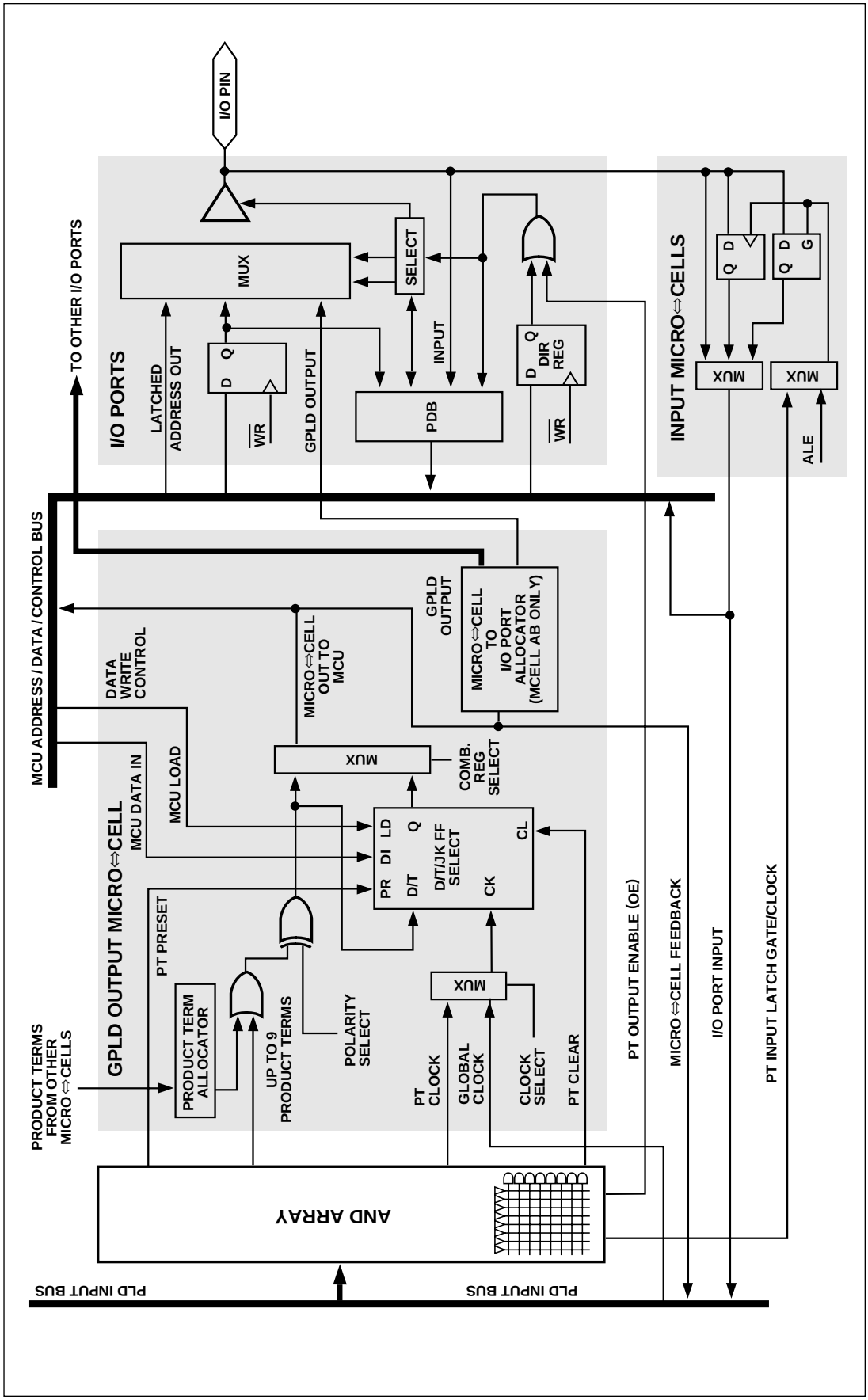
The GPLD has Output and Input Micro⇔Cells (see Figure 6). The Micro⇔Cells are configured using the PSDsoft development system. Like the other PLDs, the GPLD has an AND array which can generate up to 109 product terms, a maximum of nine product terms for each of the twelve Micro⇔Cells.

The Input and Output Micro⇔Cells are connected to the PSD813FN/FH internal data bus and can be directly accessed by the microcontroller. This enables the MCU software to load data into the Output Micro⇔Cells or read data from both the Input and Output Micro⇔Cells with no overhead visible to the user. This feature allows efficient implementation of system logic and eliminates the need to connect the data bus to the AND logic array as required in most standard PLD macrocell architectures.

Pins may also be driven as outputs by the MCU directly using MCU I/O Mode (see page 32). If the user drives pins with MCU I/O Mode, the underlying output Micro⇔Cell may be used for embedded nodes.

PLDs (cont.)

Figure 6. The GPLD and I/O Port



PLDs (cont.)

Output Micro⇔Cell

Eight of the Output Micro⇔Cells are connected to Port C pins (except PC2) and are named as McellC0-7. The remaining four Micro⇔Cells can be connected to Port A or Port B and are named as McellAB4-7. If an McellAB output is not assigned to a specific pin in PSDabel, the Micro⇔Cell Allocator will assign it to either Port A or B. Table 10 shows the Micro⇔Cells and Port assignment. Seven of the 12 output Micro⇔Cells are dedicated to controlling the Flash memory in this multi-chip module.

Table 10. Output Micro⇔Cell Port and Data Bit Assignments

Output Micro⇔Cell	Port Assignment	Native Product Terms	Max Borrowed Product Terms	Data Bit for Loading or Reading in 8-Bit Mode	PSD8XXF Assignment
McellC0	Port C0	4	5	D0	$\overline{\text{WRF}}$
McellC1	Port C1	4	5	D1	$\overline{\text{RDF}}$
McellC2	*	4	5	D2	**
McellC3	Port C3	4	5	D3	A14F
McellC4	Port C4	4	5	D4	A16F
McellC5	Port C5	4	5	D5	A17F
McellC6	Port C6	4	5	D6	A18F
McellC7	Port C7	4	5	D7	$\overline{\text{CSF}}$
McellAB4	Port A4, B4	3	6	D4	**
McellAB5	Port A5, B5	3	6	D5	**
McellAB6	Port A6, B6	3	6	D6	**
McellAB7	Port A7, B7	3	6	D7	**

*Internal node only.
**General purpose use.

The Product Term Allocator

All Micro⇔Cells have the same cell architecture except McellC0-McellC7 have four native product terms and McellAB4-McellAB7 have three native product terms. The GPLD also has a Product Term Allocator with which the PSDcompiler can automatically borrow product terms from one Micro⇔Cell to another. The McellC may borrow up to five product terms from other Micro⇔Cells for a total of nine product terms. The McellAB has three native product terms and can borrow up to six product terms. Borrowing allows Micro⇔Cell outputs needing more product terms to use the unused product terms of others and is transparent to the user.

The architecture of the 12 Output Micro⇔Cells, as shown in Figure 6, consists of native product terms and borrowed product terms from other Micro⇔Cells. The polarity of the product term input is controlled by the XOR gate. The Micro⇔Cell can implement either sequential logic, using the Flip-Flop element, or combinatorial functions. The multiplexor selects the combinatorial or the sequential logic as the Micro⇔Cell output. The multiplexor output can drive a Port pin and has also a feedback path to the AND array inputs.

Micro⇔Cell Flip-Flop Type

The Flip-Flop in the Micro⇔Cell can be configured as a D, Toggle, JK or SR type by using PSDabel in PSDsoft. The flip-flop Clock, Preset and Clear inputs are driven from a product term of the AND array. Alternatively, the device clock input (CLKIN) can be used for the flip-flop. The Preset and Clear are active high inputs; the Flip-Flop is clocked by the rising edge of the clock input.

PLDs (cont.)

Loading and Reading the Micro⇔Cells

The GPLD Micro⇔Cells occupy a memory location in the MCU address space as defined by the CSIOP (refer to the I/O section). The Flip-Flops in each of the 12 Micro⇔Cells can be loaded from the data bus by a microcontroller write bus cycle to the Micro⇔Cell (see I/O Port section for Micro⇔Cell Addresses). A “1” in the data bit that associates with the Micro⇔Cell will load a “1” to the Flip-Flop, a “0” in the data bit will load a “0” to the Flip-Flop. The loading bus cycle takes priority over other Flip-Flop inputs that include the Preset, Clear and clock. See Table 11 for the data bits that are connected to the Micro⇔Cells. The ability to load the flip-flops and read them back is useful in such applications as loadable counters, shift registers, mailboxes or handshaking protocols.

Table 11. Micro⇔Cell Flip-Flop Loading

LD	Din	Clk	In	PR	CLR	Q
1	1	X	X	X	X	1
1	0	X	X	X	X	0
0	X	Normal Flip-Flop Function				

NOTE: LD is “1” when the MCU writes to the Micro⇔Cell address

The Output Enable

The Micro⇔Cell can be connected to a PSD813FN/FH I/O pin as PLD output. The output enable of each of the Port pin output driver is controlled by a single product term (.oe) from the AND array ORed with the Direction Register output. Upon power up, if no output enable (.oe) equation is defined and the pin is declared as a PLD output in PSDsoft, the pin is enabled.

If the Micro⇔Cell output is declared as internal node and not as Port pin output in the PSDabel file, then the Port pin can be used for other I/O functions (such as MCU I/O mode). The internal node feedback can be routed as an input to the AND array.

Input Micro⇔Cell

The Input Micro⇔Cell as shown in Figure 6 is used to latch, register or pass incoming Port signals prior to driving them onto the PLD Input bus. The outputs of these Micro⇔Cells can also be read by the microcontroller through the internal Data Bus. The GPLD has 23 Input Micro⇔Cells, one for each pin of Ports A, B and C (except PC2). The Input Micro⇔Cells are individually configurable.

The enable/clock for the latch and flip-flop is driven by a multiplexor whose inputs are a product term from the GPLD AND array and the MCU address strobe (ALE). Each product term output is used to latch/clock four Input Micro⇔Cells. Port inputs [3:0] can be controlled by one product term and [7:4] can be controlled by another one.

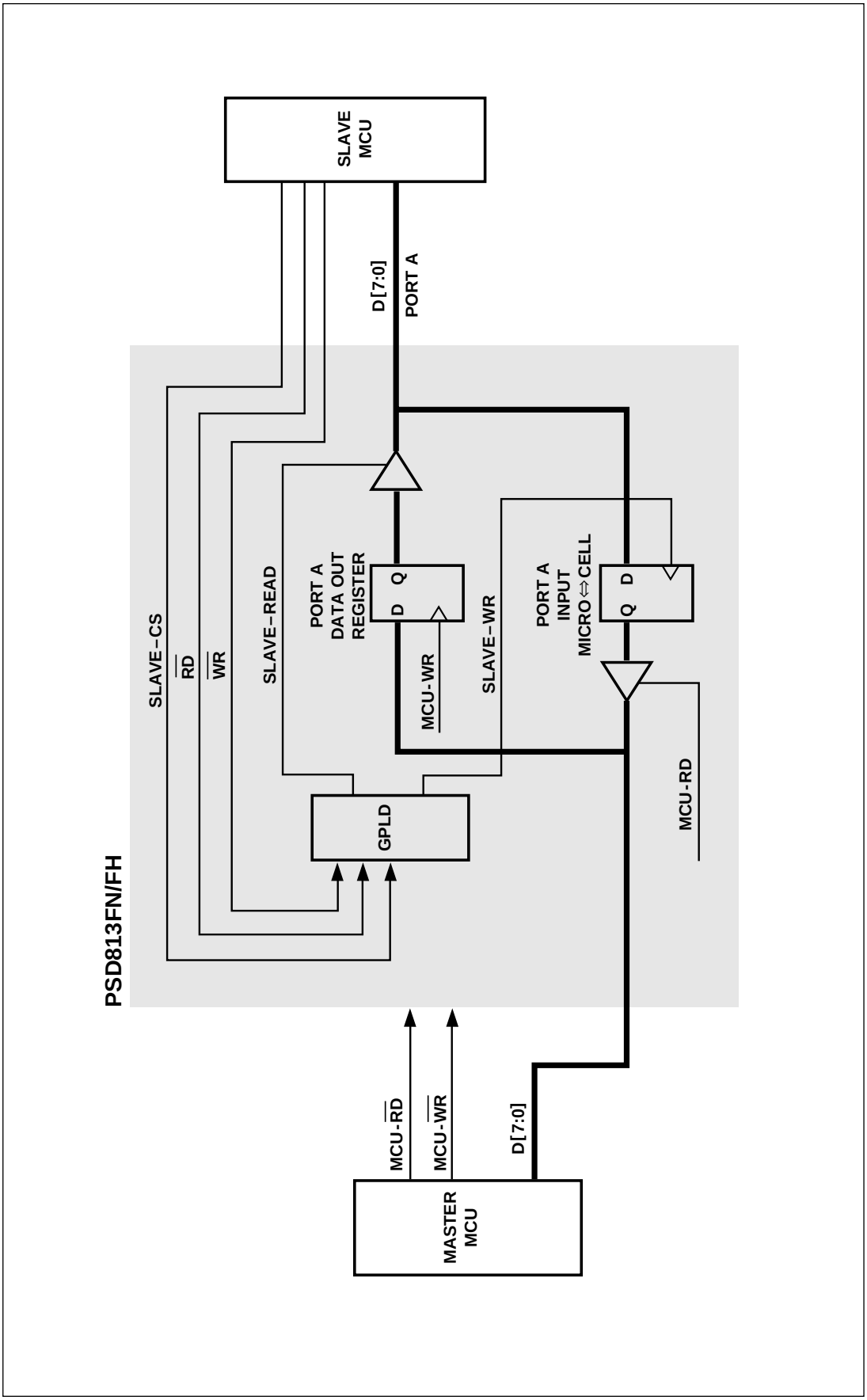
The Input Micro⇔Cell configurations are specified by equations written in PSDabel. Outputs of the Micro⇔Cells can be read by the microcontroller via the “Input Micro⇔Cell” buffer. See the I/O Port section on how to read the Micro⇔Cells.

Input Micro⇔Cells can use the ALE to latch the higher address bits (A31 – A16). The latched addresses are routed to the PLD as inputs.

The Input Micro-Cell is particularly useful in handshaking communication applications where two processors wish to pass data between each other through a commonly accessible storage. Figure 7 shows a typical configuration where the Master MCU writes to the Port A Data Out Register that is read by the Slave MCU via the activation of the “Slave-Read” output enable product term. The Slave MCU can write to Port A Input Micro⇔Cells by activating the “Slave- Wr” product term. The Master MCU can then read the Input Micro⇔Cells. The “Slave-Read” and “Slave-Wr” signals are product terms that are derived from the Slave MCU inputs of $\overline{RD}$, $\overline{WR}$, and Slave_CS.

PLDs (cont.)

Figure 7. Handshaking Communication Using Input Micro⇔Cells



Bus Interface

The “No-glue Logic” PSD813FN/FH Microcontroller Bus Interface can be directly connected to the most popular microcontrollers and their control signals. Some of these microcontrollers with their bus types and control signals are shown in Table 12. The interface type is specified using the PSDsoft tools.

Table 12. Microcontroller Busses and Control Signals

MCU	Data Bus	CNTL0	CNTL1	CNTL2	PD0**	ADIO0
8031	8	$\overline{WR}$	$\overline{RD}$	$\overline{PSEN}$	ALE	A0
68330	8	R/$\overline{W}$	$\overline{DS}$	*	ALE	A0
80198	8	$\overline{WR}$	$\overline{RD}$	*	ALE	A0
68HC11	8	R/$\overline{W}$	E	*	AS	A0
80C251***	8	$\overline{WR}$	$\overline{RD}$	$\overline{PSEN}$	ALE	A0
Z8	8	R/$\overline{W}$	$\overline{DS}$	*	*	A0
Neuron 3150	8	R/$\overline{W}$	$\overline{DS}$	*	*	A0

*Not used CNTL2 pin can be configured as GPLD input. Other not used pins (CNTL2, PD0) can be configured for other I/O functions.

**ALE/AS input is optional for microcontrollers with a non-multiplexed bus.

***8051 compatible mode only.

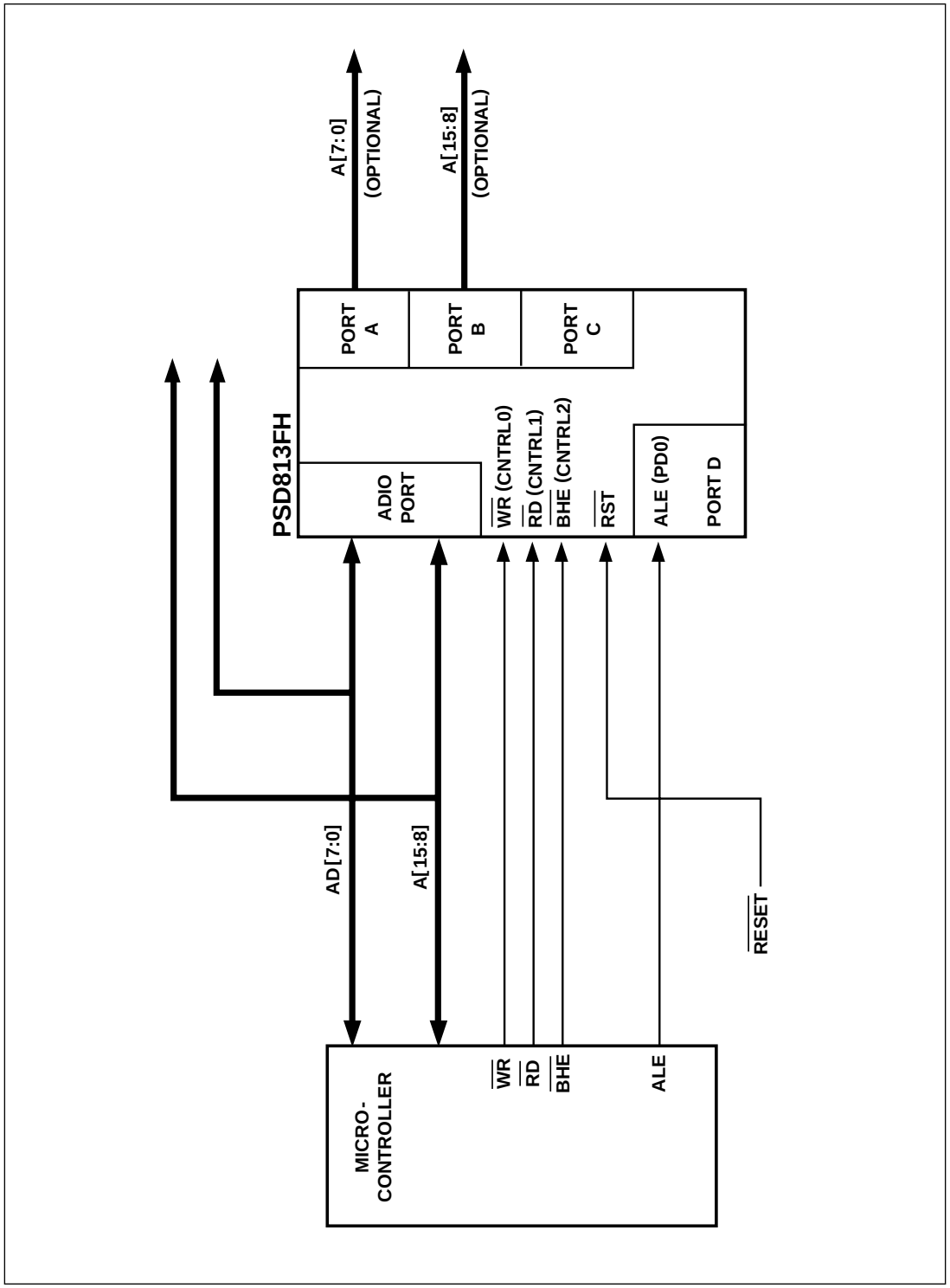
Table 12 shows the names of the PSD813FN/FH bus interface control pins and their functions. The control pins have multiple functions and can be configured to interface to many microcontrollers. Depending on the microcontroller, some of the control input pins are not required and may be used as GPLD input or other I/O functions. Specific examples of interfaces to different microcontrollers are provided in the following sections. For microcontrollers that have more than 16 address lines, Port A and B pins may be used as additional address inputs

Bus Interface (cont.)

PSD813FH Interface To a Multiplexed Bus

Figure 8 shows an example of a system using a microcontroller with a multiplexed bus and a PSD813FH. The ADIO port on the PSD813FH is connected directly to the microcontroller address/data bus. The bus may be multiplexed only on one byte (eight-bit data) or on both bytes (sixteen-bit data). The ALE latches the address lines internally; latched addresses can be brought out to Port A or B. The PSD813FH drives the ADIO data bus only when one of its internal resources is accessed and the $\overline{RD}$ input is active.

Figure 8. An Example of a Typical 8-Bit Multiplexed Bus Interface

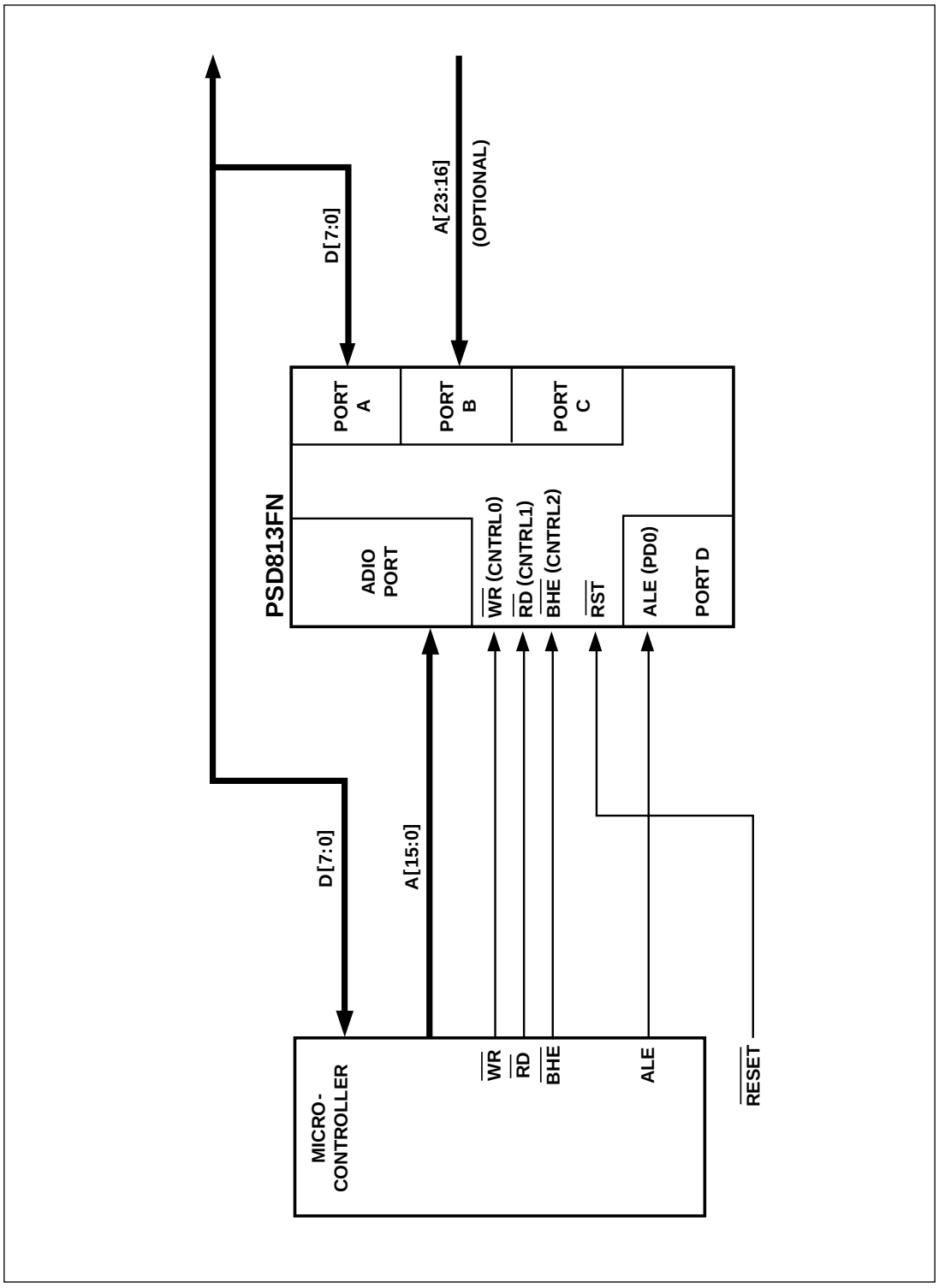


Bus Interface (cont.)

PSD813FN Interface To a Non-Multiplexed Bus

Figure 9 shows an example of a system using a microcontroller with a non-multiplexed bus and a PSD813FN. The address bus is connected to the ADIO Port, and the data bus is connected to Port A (D[7:0]). The data Ports are in tri-state mode when the PSD813FN is not accessed by the microcontroller. Should the system address bus exceed sixteen bits, Port B may be used as additional address inputs.

Figure 9. An Example of a Typical Non-Multiplexed Bus Interface, 8-Bit Data Bus



Bus Interface (cont.)

Microcontroller Interface Examples

Figures 10 and 11 show examples of the basic connections between the PSD813FN/FH and some popular microcontrollers. The PSD813FN/FH control input pins are labeled as the microcontroller function for which they are configured. The MCU interface is specified using the PSDsoft tools. The PC2 pin should be grounded if Vstby is not used.

80C31

Figure 10 shows the interface to the 80C31 which has an 8-bit multiplexed address/data bus. The lower address byte is multiplexed with the data bus. The microcontroller RD and WR signals may be used for accessing internal SRAM and I/O Ports while the PSEN signal is used to read the EPROM. The ALE input (Port D PD0) latches the address. Refer to the Memory Section for additional 80C31 operating modes.

68HC11

Figure 11 shows an interface to an 68HC11 where the PSD813FH is configured in 8-bit multiplexed mode with E and R/W settings. The ECSPLD can generate the READ and WR signals for external on board devices. The CNTL2 pin is not used and can be used as a PLD input.

80C251

The Intel 80C251 microcontroller features a user-configurable bus interface with two possible bus configurations as shown in Table 13.

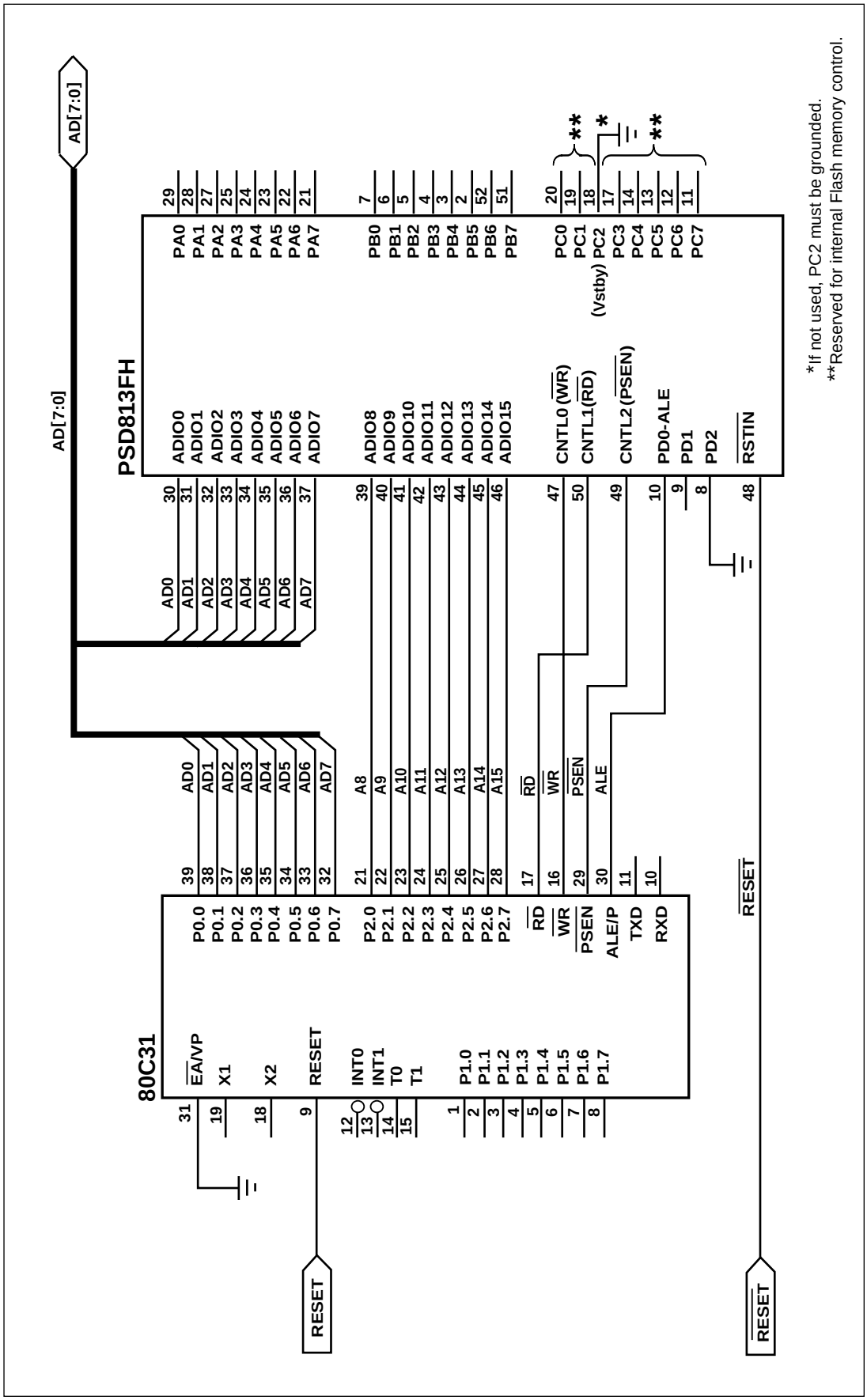
Table 13. 80C251 Configurations

Configuration	80C251 Read/Write Pins	Connecting to PSD813FN/FH Pins	Page Mode
1	$\overline{WR}$ $\overline{RD}$ $\overline{PSEN}$	CNTL0 CNTL1 CNTL2	Non-Page Mode, 80C31 compatible A[7:0] multiplex with D[7:0}
2	$\overline{WR}$ $\overline{PSEN}$ only	CNTL0 CNTL1	Non-Page Mode A[7:0] multiplex with D[7:0}

Configuration 1 is 80C31 compatible. The bus interface to the PSD813FH is identical to that shown in Figure 10. There is only one read input ($\overline{PSEN}$) connected to the CNTL1 pin on the PSD813FH. The A16 connection to the PA0 pin allows for a larger address input to the PSD813FH.

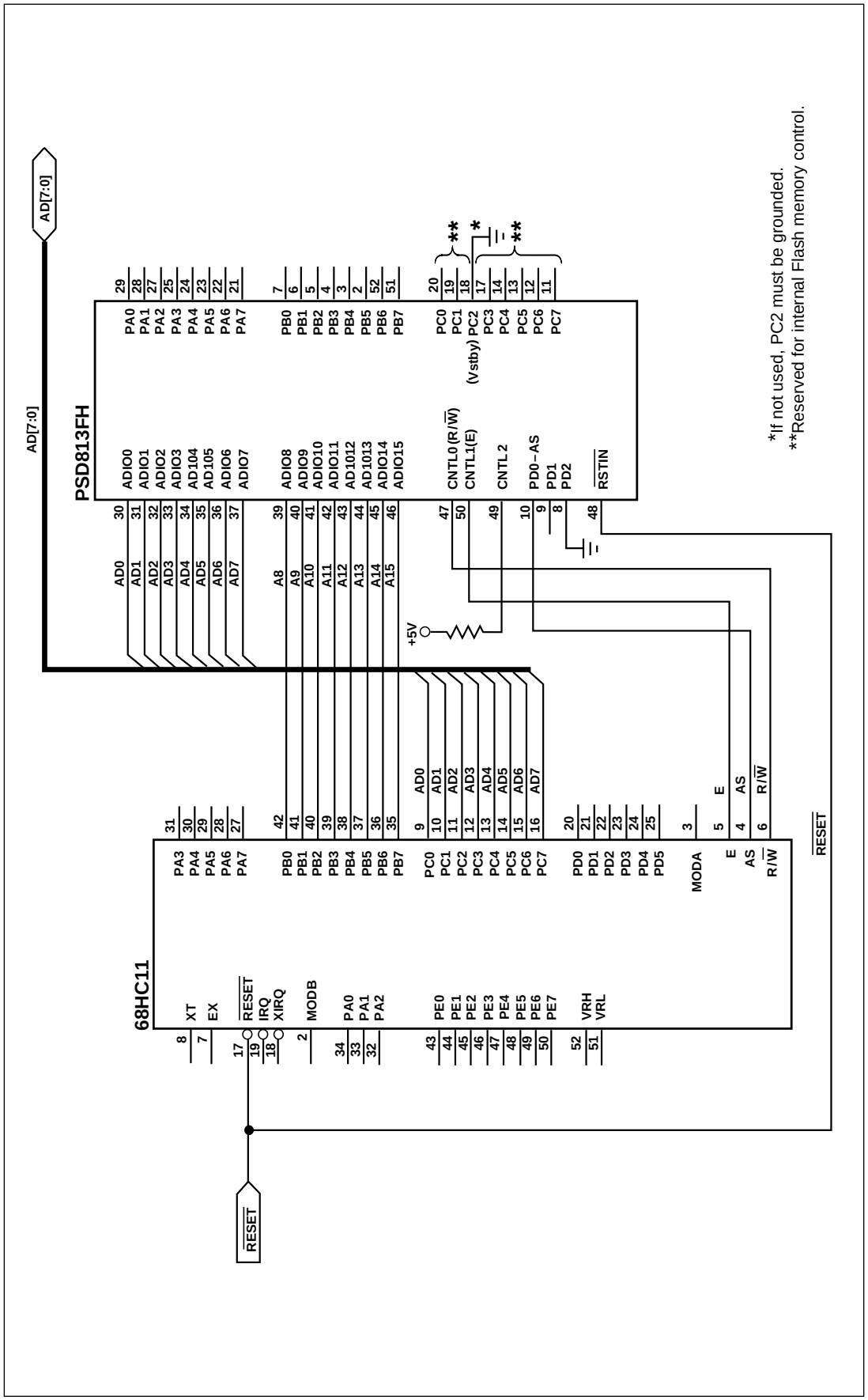
Bus Interface (cont.)

Figure 10. Interfacing the PSD813FH with an 80C31 MCU



Bus Interface (cont.)

Figure 11. Interfacing the PSD813FH with a 68HC11



I/O Ports

There are four programmable I/O ports: Ports A, B are 8 bits, Port C is seven bits and Port D is three bits. The ports can be configured to function in different modes of operation.

Each port pin is individually configurable allowing a single port to perform multiple functions. The configuration is defined either using the PSDsoft tools or by the microcontroller writing to on-chip registers.

General Port Architecture

The general architecture of the I/O Port is shown in Figure 12. Individual Port diagrams are shown in Figures 14, 15 and 16, and will be discussed in the section below. If the PSD813FN/FH is configured to a non-multiplexed bus mode, Port A and/or Port B are connected to the MCU data bus and are not available as general purpose I/O ports.

As shown in Figure 12, the port pins contain an output multiplexer whose selects are driven by the configuration defined in PSDabel and the Control Registers. Inputs to the multiplexer include the following:

- ❏ Output data from the Data Out Register in the MCU I/O output mode
- ❏ Latched address outputs
- ❏ GPLD Micro⇔Cell output or ECSPLD external chip select output
- ❏ ECSPLD external chip select output

The above inputs are also connected to the Port Data Buffer (PDB) for feedback to the Internal Data Bus that can be read by the microcontroller. The PDB is a three-state buffer operating like a multiplexer that allows only one source to be read at a time. The PDB also has inputs from the Direction Register, Control Register and direct port pin input (Data In).

The Port pin's tri-state output driver enable is controlled by a two input OR gate whose inputs come from the GPLD AND array Enable product term (.oe) and the Direction Register. If the enable product term of the array output is not defined, then the Direction Register has sole control of the buffer. Refer to Tables 14 and 15 on how the direction of a port pin is configured.

Table 14. Port Pin Direction Control, Output Enable P.T. Not Defined

Direction Register Bit	Port Pin Mode
0	Input
1	Output

Table 15. Port Pin Direction Control, Output Enable P.T. Defined

Direction Register Bit	Output Enable P.T.*	Port Pin Mode
0	0	Input
0	1	Output
1	0	Output
1	1	Output

*Port D does not have an output enable P.T.

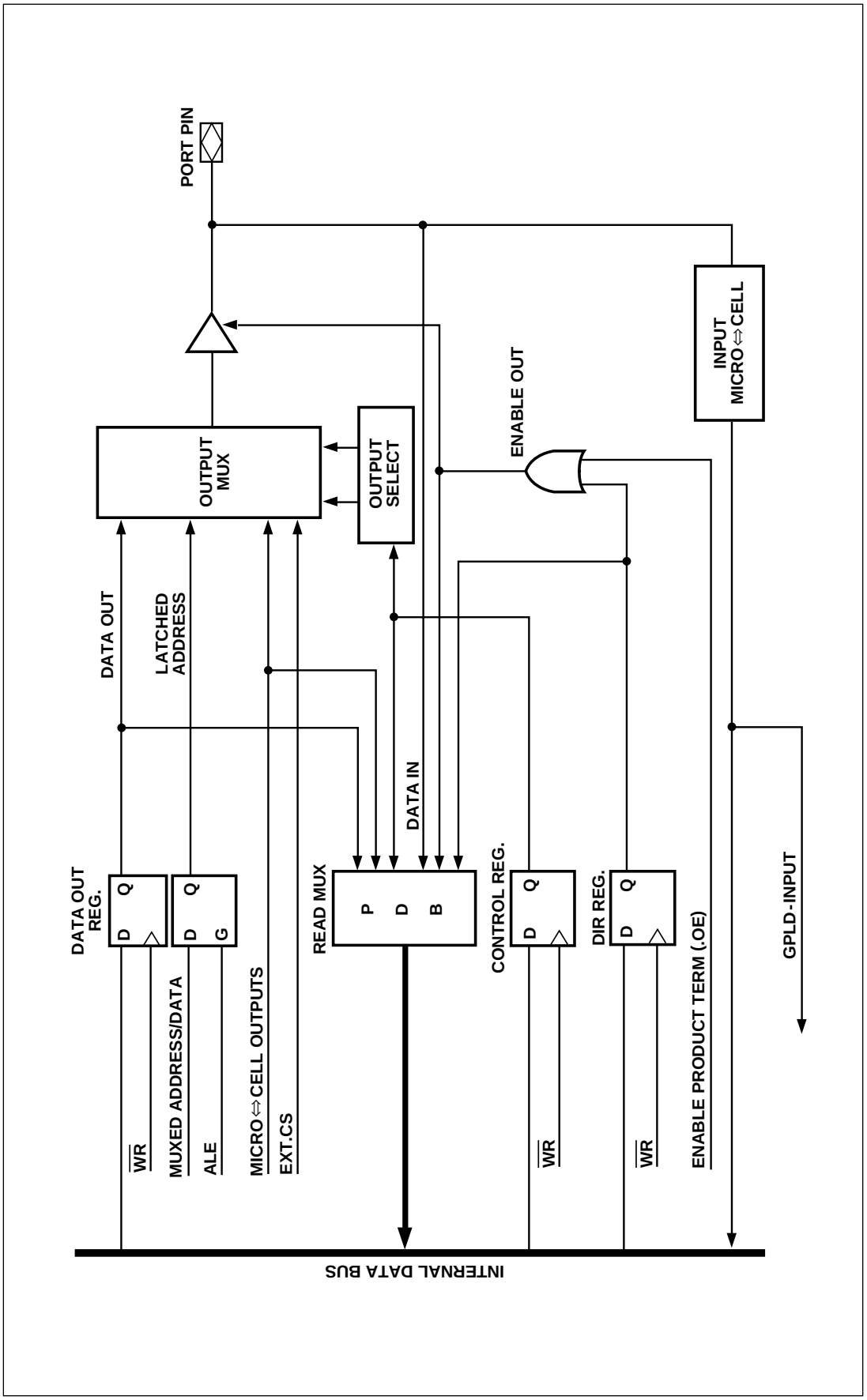
The register contents can be altered by the microcontroller. The PDB feedback path allows the microcontroller to check the contents of the registers.

The A, B and C Ports have embedded Input Micro⇔Cells which can be configured as a latch, a register or direct input to the GPLD. The latch and register are clocked by the address strobe or a product term from the GPLD AND array. The output from the Input Micro⇔Cell drives the PLD input bus and can be read by the microcontroller. Refer to the Input Micro⇔Cell description in the PLD section.

Port A has additional logic (not shown in Figure 12) that enables it to operate in Peripheral I/O mode when the PIO bit in the VM Register is set.

I/O Ports (cont.)

Figure 14. General I/O Port Architecture



I/O Ports (cont.)

Port Operating Modes

The I/O Ports have several modes of operation as shown in Table 16. Some modes may be selected using the PSDabel tool and programmed into the device using Non-Volatile Memory (NVM) that is active when power is applied and cannot be altered unless the device is reprogrammed. If a mode is not defined in PSDsoft, then other modes can be set by the microcontroller writing to the Port configuration registers at Run-Time. The PLD I/O, Data Port and Address Input modes are NVM configurations. The other modes are initiated by the microcontroller.

If the NVM modes are not selected, the port can be altered dynamically between MCU I/O or Address Out modes by writing to the Control Register. Each bit of the eight-bit Control Register may store a “1”, setting its respective bit in the port to MCU I/O, or to a “0”, setting it to Address Out. The Direction Register or the output enable product term determine if the pin is input or output.

Table 16 summarizes the operating modes of the I/O ports. Not all the functions are available to every port. Table 17 shows how and where the different modes are configured.

Table 16. Port Operating Modes

Port Mode	Port A	Port B	Port C	Port D	Configured at Run-Time
MCU I/O	Yes	Yes		Yes	Yes
PLD I/O McellAB Outputs McellC Outputs ECSPLD Outputs ZPLD Inputs	 PA7 – 4 No PA3 – 0 Yes	 PB7 – 4 No PB3 – 0 Yes	Reserved for Flash Memory Control Plus VSTBY	 No No PD2 – 0 Yes	No
Address Out	Yes (A7 – 0)	Yes (A7 – 0, A15 – 8)		No	Yes
Address In	Yes	Yes		No	No
Data Port	Yes (D7 – 0)			No	No
Open Drain	Yes (PA7 – 4)	Yes (PB7 – 4)		No	Yes
Slew Rate	Yes (PA3 – 0)	Yes (PB3 – 0)		Yes	Yes
Peripheral I/O	Yes	No		No	Yes

I/O Ports (cont.)

Port Operating Modes (cont.)

Table 17. Port Operating Mode Settings

Mode	Defined In PSDabel	Defined In PSDconfiguration	Control Register Setting	Direction Register Setting	VM Register Setting
MCU I/O	Declare pins only	NA	0	1 = output, 0 = input (Note 1)	NA
PLD I/O	Logic equations	NA	NA*	(Note 1)	NA
Data Port (Port A,B)	NA	Specify bus type	NA	NA	NA
Address Out (Port A,B)	Declare pins only	NA	1	1 (Note 1)	NA
Address In (Port A,B,C)	Logic equation for Input Micro⇔Cells	NA	NA	NA	NA
Peripheral I/O (Port A)	Logic equations (PSEL0 & 1)	NA	NA	NA	PIO bit = 1

*NA – Not Applicable

NOTE 1: The direction of the Port A, B, C pins are controlled by the Direction Register ORed with the individual output enable product term (.oe) from the GPLD AND array.

PLD I/O Mode

The PLD I/O mode uses the port as an input to the GPLD Input Micro⇔Cell, and/or as an output from the GPLD, ECSPLD. The Port assignments are shown in Tables 9 and 10. The output can be tri-stated with a control signal defined by a product term (.oe) from the PLD, or, by setting a zero in the Direction Register. The Direction Register **must not** be set to “1” if the pin is defined as a PLD input pin. The PLD I/O mode is specified in PSDabel by declaring the port pins, then writing an equation assigning it to the port.

MCU I/O Mode

In the MCU I/O Mode the microcontroller uses the PSD813FN/FH ports to expand its own I/O ports. The ports on the PSD813FN/FH are mapped into the microcontroller address space. The addresses of the ports are listed in Table 22.

A port pin will be put into MCU I/O mode by writing a zero to the corresponding bit in the Control Register. The direction may be changed by writing to the Direction Register for the port where a “1” makes it an output and a “0” an input. The output enable product term also can change the direction of the pin (see Table 14 and 15). When the pin is configured as output, the content of the Data Out Register drives the pins. In input mode, the microcontroller reads the port input through the Data In buffer

Ports C and D do not have a Control Register and are in MCU I/O mode by default for pins that are not configured as PLD I/O.

Address Out Mode

For microcontrollers with a multiplexed address/data bus, the ports in Address Out mode drive latched addresses to external devices. Address [7:0] are always assigned to Port A. See Table 23 for the address output pin assignments on Ports A and B. The Direction Register and the Control Register must be set to a “1” for port pins using Address Out mode.

In non-multiplexed 8 bit bus mode, address[7:0] are available on Port B in Address Out Mode.

I/O Ports (cont.)

Port Operating Modes (cont.)

Address In Mode

For microcontrollers that have more than 16 address lines, the higher addresses can be connected to Port A, B, or C. The address input can be latched in the Input Micro⇔Cell by ALE. Any input that is included in the DPLD equations for the PSD Flash, OTP Boot, or EPROM is considered as address input.

Data Port Mode

Port A can be used as a data bus port for a microcontroller with a non-multiplexed address/data bus. The Data Port is connected to the data bus of the microcontroller. The general I/O functions are disabled in Port A if the port is configured as Data Port. See Figure 9.

Peripheral I/O Mode

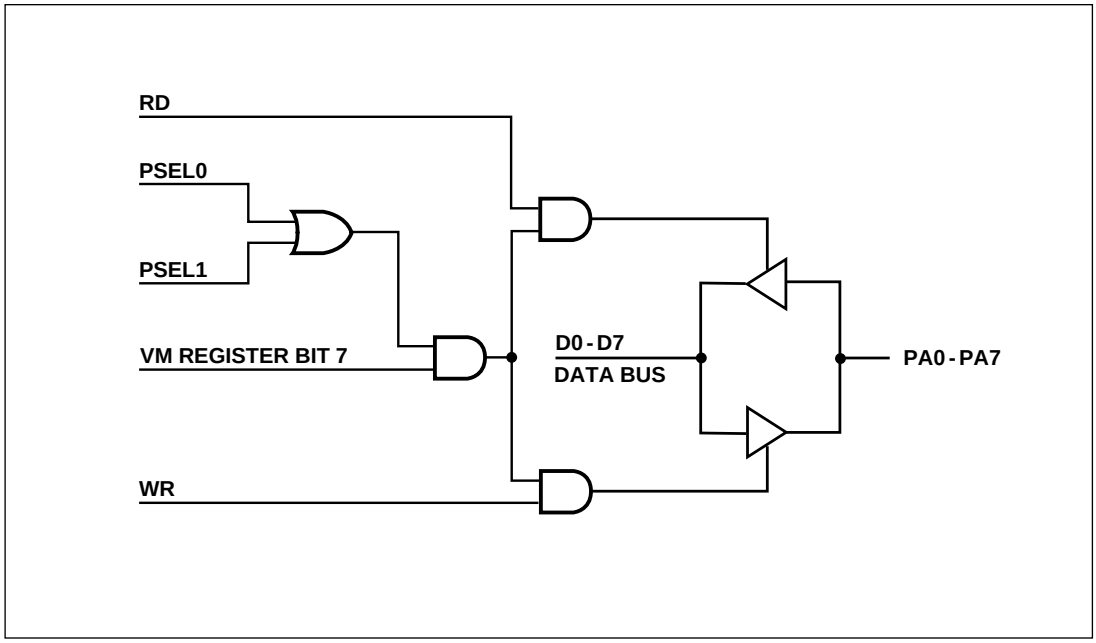
Only Port A supports the Peripheral I/O mode whereby all of Port A serves as a tri-stateable bi-directional data buffer of the microcontroller's data bus. Peripheral mode is enabled by setting Bit 7 of the VM Register to a "1". Figure 13 shows that when Peripheral mode is enabled and either PSEL0 and PSEL1 from the DPLD is active, Port A acts as a bi-directional buffer for the microcontroller D[7:0] data bus. The buffer is tri-stated when PSEL 0 or 1 is not active. The Peripheral I/O mode can be used to interface with external peripherals. Use PSDabel to write equations that contain the keyboards PSEL0 and PSEL1.

Open Drain/Slew Rate Mode

Ports A (pins PA7-4) and B (pins PB7-4) and C (except PC2) can be configured as open drain instead of CMOS outputs. The Open Drain configuration is useful for sinking large currents to operate LEDs, for example. The Open Drain mode is enabled by writing a "1" to the corresponding bit in the Drive Register.

Port A (PA3–0), Port B (PB3–0) and Port D can be configured as ECSPLD outputs that have a high slew rate. The high slew rate is enabled by writing a "1" to the corresponding bit in the Drive Register.

Figure 13. Port A Peripheral Mode



I/O Ports (cont.)

Port Registers

Each port has a set of registers used for configuration (PCR, Port Configuration Registers) and data transfers (PDR, Port Data Registers). The contents of the registers can be accessed by the microcontroller through normal read/write bus cycles at the addresses given in Table 22. The address of the registers is comprised by that of the CSIOP output from the DPLD plus an address offset as listed in the tables.

The pins of a port are individually configurable and each bit in the register controls its respective pin. For example, Bit 0 in a register refers to Bit 0 in its port. The three Port Configuration Registers, shown in Table 18, are used for setting the port configuration. Each register is set to zero at power up.

Table 18. Port Configuration Registers

Register Name	Port	MCU Access
Control	A,B	Write/Read
Direction	A,B,C,D	Write/Read
Drive*	A,B,C,D	Write/Read

*Note: See Table 20 for Drive Register bit definition.

Control Register

A “0” in the Control Register sets the Port pin to MCU I/O for Port A and B. A “1” sets the Port pin to Address Out mode. The default mode is MCU I/O.

Direction Register

Controls the direction of data flow in the I/O Ports. A “1” configures the port to be an output, and a “0” to an input. The I/O configuration can be read from the Direction Register. The default mode is input.

As shown in Figure 12, the direction of data flow in Port A,B and C pins are also controlled by the output enable (.oe) product term from the GPLD AND array. If the .oe product term is not active, the Direction Register has sole control of the pin direction.

An example of a configuration for a port with the three least significant bits set to output and the remainder set to input is shown in Table 19. The Port D register has only the three least significant bits active.

Table 19. Port Direction Assignment Example

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	1	1	1

I/O Ports (cont.)

Port Registers (cont.)

Drive Register

The Drive Register configures the pin driver as Open Drain, or in the case of ECSPLD outputs, sets the pin to operate in high slew rate. An external pull-up resistor is not required when the pin is in the slew rate mode.

For Ports A and B the register sets different functions for the lower and higher nibbles. The four upper bits set the corresponding bits the as CMOS (“0”) or Open Drain (“1”) driver. The four lower bits are used for slew rate control. The slew rate is a measurement of the rise and fall times of the output. A higher slew rate means a faster output response while a lower slew rate is a slower, lower slope, response. The pin operates in high slew rate when the corresponding bit in the Drive Register is set to “1”.

Table 20 shows the Drive Registers of Port A, B, C and D and which pin has the Open Drain or Slew Rate configuration.

Table 20. Drive Register Pin Assignment

Drive Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port A	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port B	Open Drain	Open Drain	Open Drain	Open Drain	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port C*	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	NA	Open Drain	Open Drain
Port D	NA	NA	NA	NA	NA	Slew Rate	Slew Rate	Slew Rate

NOTE: NA = Not Applicable, bit should set to “0”.

*Port C pins are dedicated to Flash memory control in this multi-chip module product.

I/O Ports (cont.)

Port Data Registers

The Port Data Registers, shown in Table 21, are used by the microcontroller to write or read data to or from the ports. Table 21 shows the register name, the ports having each register type and microcontroller access for each register. The registers are described below.

Table 21. Port Data Registers

Register Name	Port	MCU Access
Data In	A,B,C,D	Read – the input on pin
Data Out	A,B,C,D	Write/Read Feedback
Output Micro⇔Cell	A,B,C	Read – outputs of Micro⇔Cells Write – loading Micro⇔Cells Flip-Flop
Input Micro⇔Cell	A,B,C	Read – outputs of the Input Micro⇔Cells
Enable Out	A,B,C	Read – the output enable control of the port driver

Data In

Port pins are connected directly to the Data In buffer. In MCU I/O input mode, the pin input is read through the Data In buffer. The MCU can always read the state of a Port pin using this method, regardless of what is driving the pin.

Data Out Register

Stores output data written by the MCU in the MCU I/O output mode. The contents of the Register are driven out to the pins if the Direction Register or the .oe product term is set to “1”. The contents of the register can also be read back by the microcontroller.

Output Micro⇔Cell

The GPLD Output Micro⇔Cells occupy a location in the microcontroller’s address space. The microcontroller can read the output of the Micro⇔Cells. Writing to the Micro⇔Cell loads data to the Micro⇔Cell Flip-Flops. Refer to the PLD section for more detail.

Input Micro⇔Cell

The Input Micro⇔Cells can be used to latch or store external inputs. The outputs of the Input Micro⇔Cells are routed to the PLD input bus and also can be read by the microcontroller. Refer to the PLD section for detail description.

Enable Out

The Enable Out buffer allows the microcontroller to read the outputs of the “OR” gate that is the enable input to the port output driver. A “1” indicates the driver is in output mode, a “0” indicates the driver is in tri-state and the pin is in input mode.

I/O Ports (cont.)

Port Data Registers (cont.)

Register I/O Address Offset

The base address of the Registers is defined in the CSIOP equation that occupies 256 bytes of address space and is defined by the user in PSDsoft. The lower address byte A[7:0], or address offset, selects the register. Table 22 shows the address offset for all MCUs except those Motorola microcontrollers with a 16-bit data bus.

For example, when the CSIOP is defined to occupy the address range of 1000h to 10FFh in PSDabel, the address of the Port A Control Register is then 1002h.

Table 22. I/O Register Address Offset (relative to CSIOP)

Register Name	Port A	Port B	Port C	Port D
Data In	00	01	10	11
Control	02	03		
Data Out	04	05	12	13
Direction	06	07	14	15
Drive	08	09	16	17
Input Micro⇔Cell	0A	0B	18	
Enable Out	0C	0D	1A	
Output Micro⇔Cell	20	20	21	

Port A and B – Functionality and Structure

Port A and B have similar functionality and structure as shown in Figure 14. The two ports can be configured to perform one or more of the following functions:

- ❏ MCU I/O Mode
- ❏ GPLD Output – Micro⇔Cells McellAB[7:4] can be connected to Port A PA[7:4} or Port B PB[7:4].
- ❏ ECSPLD Output – External chip select output can be connected to either Port A PA[3:0] or Port PB[3:0].
- ❏ Latched Address output – Provide latched address output per Table 23.
- ❏ Address In – Additional high address inputs using the Input Micro⇔Cells.
- ❏ Open Drain/Slew Rate – pins PA[3:0] and PB[3:0] can be configured to Open Drain Mode pins PA[7:4] and PB[7:4] can be configured to fast slew rate
- ❏ Data Port – Port A to D[7:0} for 8 bit non-multiplexed bus
- ❏ Peripheral Mode – Port A only

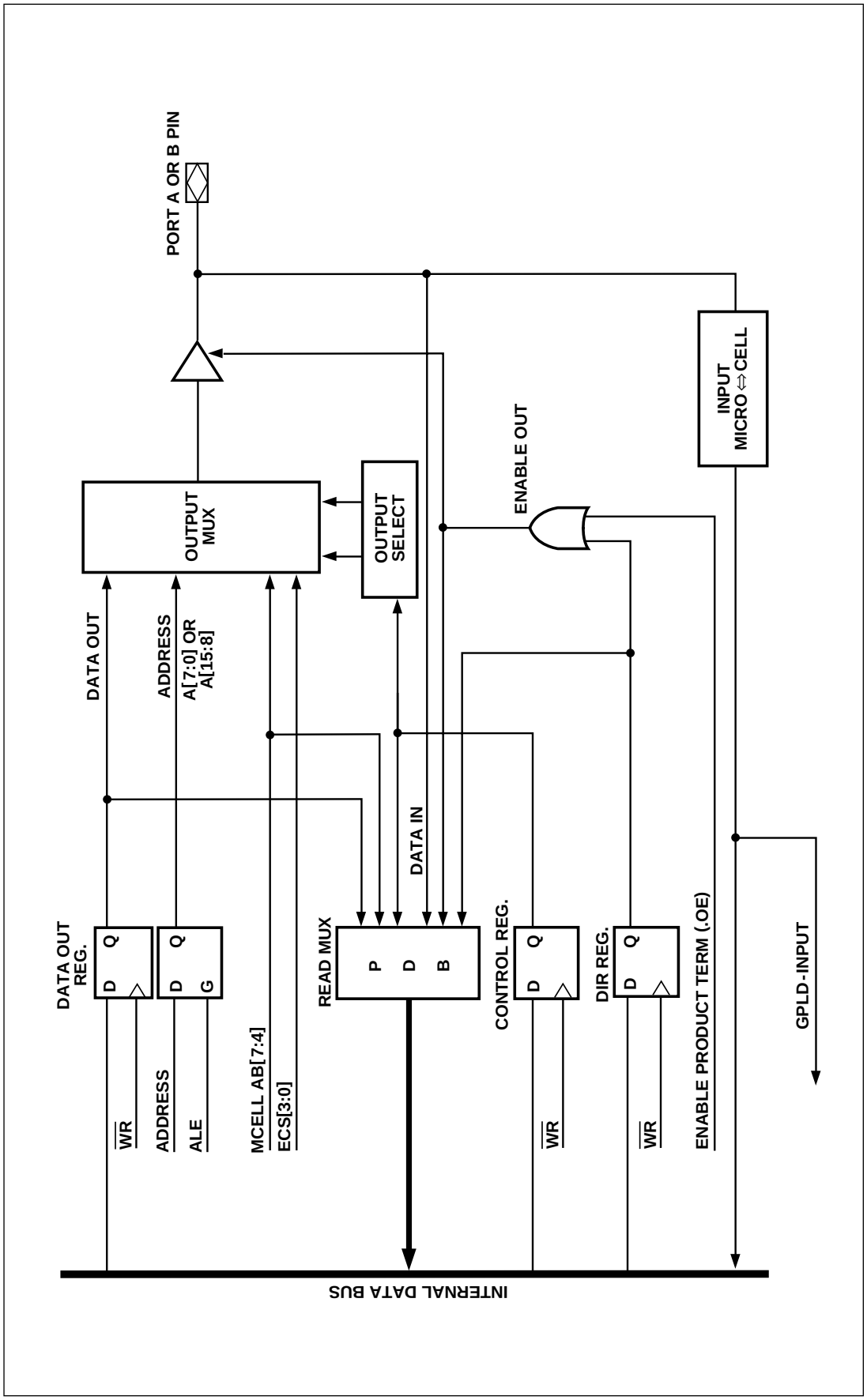
Table 23. I/O Port Latched Address Output Assignments

Microcontroller	Port A (3:0)	Port A (7:4)	Port B (3:0)	Port B (7:4)
8-Bit Multiplexed Bus (PSD813FH)	Address (3:0)	Address (7:4)	Address (3:0)	Address (7:4)
8-Bit Non-Multiplexed Bus (PSD813FN)	N/A	N/A	Address (3:0)	Address (7:4)

N/A = Not Applicable.

I/O Ports (cont.)

Figure 14. Port A and B Structure



I/O Ports (cont.)

Port C – Functionality and Structure

All Port C pins are configured as PLD I/O mode for Flash memory controls (except PC2). The other Port C I/O functions are disabled (multi-chip module only).

PC0	$\overline{WRF}$	Flash Memory Write Signal
PC1	$\overline{RDF}$	Flash Memory Read Signal
PC2	Vstby	SRAM Vstby
PC3	A14F	Flash Address A14
PC4	A16F	Flash Address A16
PC5	A17F	Flash Address A17
PC6	A18F	Flash Address A18
PC7	$\overline{CSF}$	Flash Chip Select

Port C pin PC2 is dedicated as the Vstby pin for SRAM battery backup and can not be used for other functions.

Port D – Functionality and Structure

Port D has only three I/O pins, does not support Address Out mode, and no Control Register is required. Port D can be configured to perform one or more of the following functions:

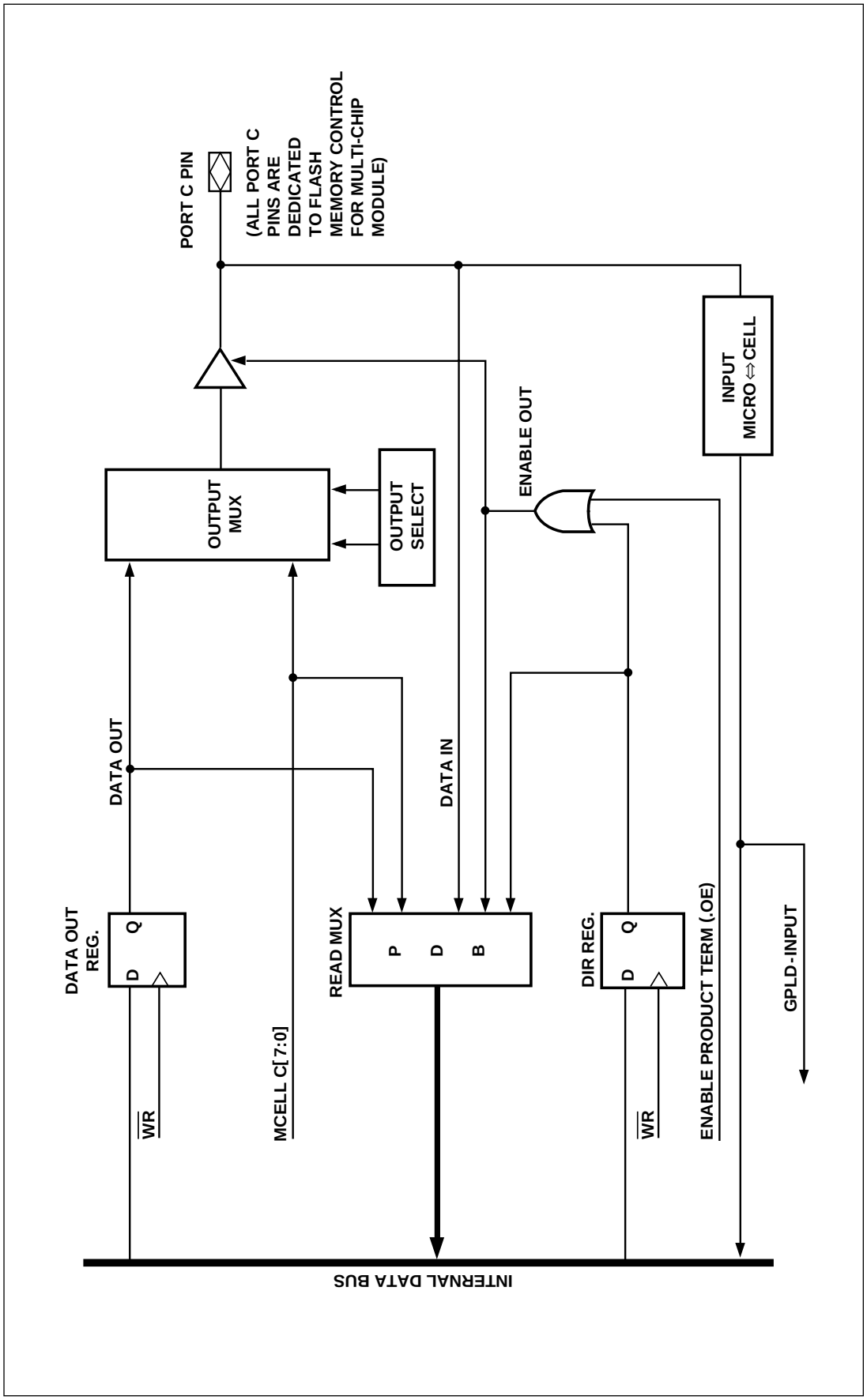
- ❏ MCU I/O Mode
- ❏ ECSPLD Output – External chip select output
- ❏ PLD Input – direct input to PLD, no Input Micro⇔Cells
- ❏ Slew rate – pins can be set up for fast slew rate

Port D pins can be configured in PSDsoft as input pins for other dedicated functions:

- ❏ PD0 – ALE, as address strobe input
- ❏ PD1 – CLKIN, as clock input to the Micro⇔Cells Flip-Flops and APD counter
- ❏ PD2 – CSI, as active low chip select input. A high input will disable the PSD EPROM/SRAM.

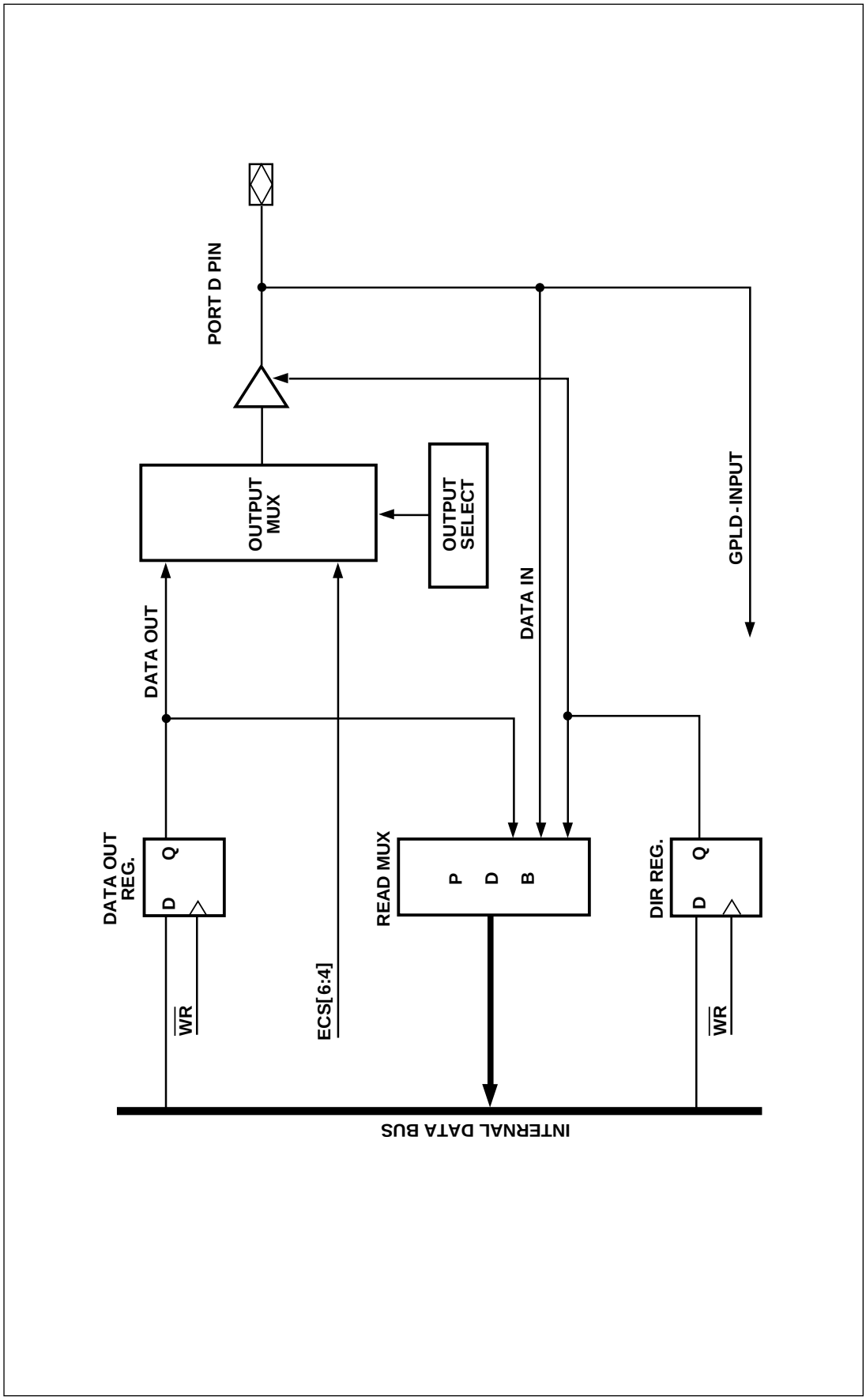
I/O Ports (cont.)

Figure 15. Port C Structure



I/O Ports (cont.)

Figure 16. Port D Structure



Memory Block

The PSD813FN/FH are a multi-chip module that includes a PSD6XX die and a 4 megabit Flash memory die configured to operate as a 1 Mb device. The PSD813FN/FH includes 32 Kbytes of OTP Boot EPROM; the Flash die provides 128 Kbytes of Flash memory. The OTP Boot EPROM is used for system boot up and for storing the Flash memory programming algorithm. The Flash erase and programming algorithms are compatible to the AMD and SGS-Thomson Embedded Erase and Programming Algorithm™. The Flash memory can be erased or programmed while the microcontroller is executing code from the Boot EPROM.

Chip selects for the memory blocks come from the DPLD and GPLD decoding logic and are defined by the user in the PSDsoft software. Figure 17 shows the organization of the Memory Block.

Boot EPROM

The chip selects (CSBOOT0–3) for the OTP Boot EPROM are generated from the DPLD address decoder. The CSBOOT0–3 are defined in 8 Kbyte boundaries and should not overlap the Flash memory address space.

Flash Memory

The Flash die that is used on this MCM is a 4 Mbit Flash device but only 1 Mbit will be addressed. Address lines A14 and A15 are inactive during Flash reads. This leaves address lines A16, A17, and A18 to page through eight 16 Kbyte sectors of Flash memory. Each 16 Kbyte sector of Flash is addressed by the address lines A0–A13. This Flash paging is simplified by the configuration of the DPLD and the GPLD. FS0–7 are the chip selects for each block that is defined in the DPLD at 16 Kbyte boundaries. The designer may custom configure Flash addressing schemes by the HDL equations developed in PSDsoft. The use of the internal PSD Page register is very effective in this application. See Figure 17 and Table 24.

NOTE: Unlike Flash reads, whenever the embedded Flash algorithms are exercised (write, erase, ID, etc), address line A14 to the Flash is enabled (as configured by the HDL) to pass commands from the MCU to the Flash die. Address line A15 to the Flash die is permanently grounded.

Seven of the pins and Micro⇔Cells on the PSD6XX die are reserved for generation of Flash memory control signals. The address lines A14F, A16F, A17F, A18F, and the chip select CSF are generated based on the FS0–7 inputs to the GPLD.

Refer to Appendix A for the operation and programming algorithm for the Flash memory.

SRAM

The SRAM has 4 Kbits of memory, organized as 512 x 8. The SRAM is enabled by the chip select signal RS0 from the DPLD. The SRAM has a battery back-up (STBY) mode. This back-up mode is automatically invoked when the V_{CC} voltage drops under the Vstdby voltage. The Vstdby voltage is connected only to the SRAM and cannot be lower than 2.0 volts.

Memory Select Map

The Boot EPROM, Flash memory, and SRAM chip select equations are defined in the ABEL file in terms of address and other DPLD inputs. The memory space for the Flash chip select (FS0–7) should not be larger than the 16K Flash block it is selecting. The Boot EPROM block should not be larger than 8 Kbytes.

The following rules govern how the PSD813F memory selects/space are defined:

- ❏ The Flash blocks address space cannot overlap among blocks.
- ❏ The Flash blocks address space cannot overlap the Boot EPROM, the SRAM and I/O address space.
- ❏ SRAM and internal I/O address space cannot overlap.
- ❏ SRAM and internal I/O space can overlap Boot EPROM space, with priority given to SRAM or I/O. The portion of Boot EPROM which is overlapped cannot be accessed.

Memory Block (cont.)

Figure 17. PSD813FN/FH Memory Block

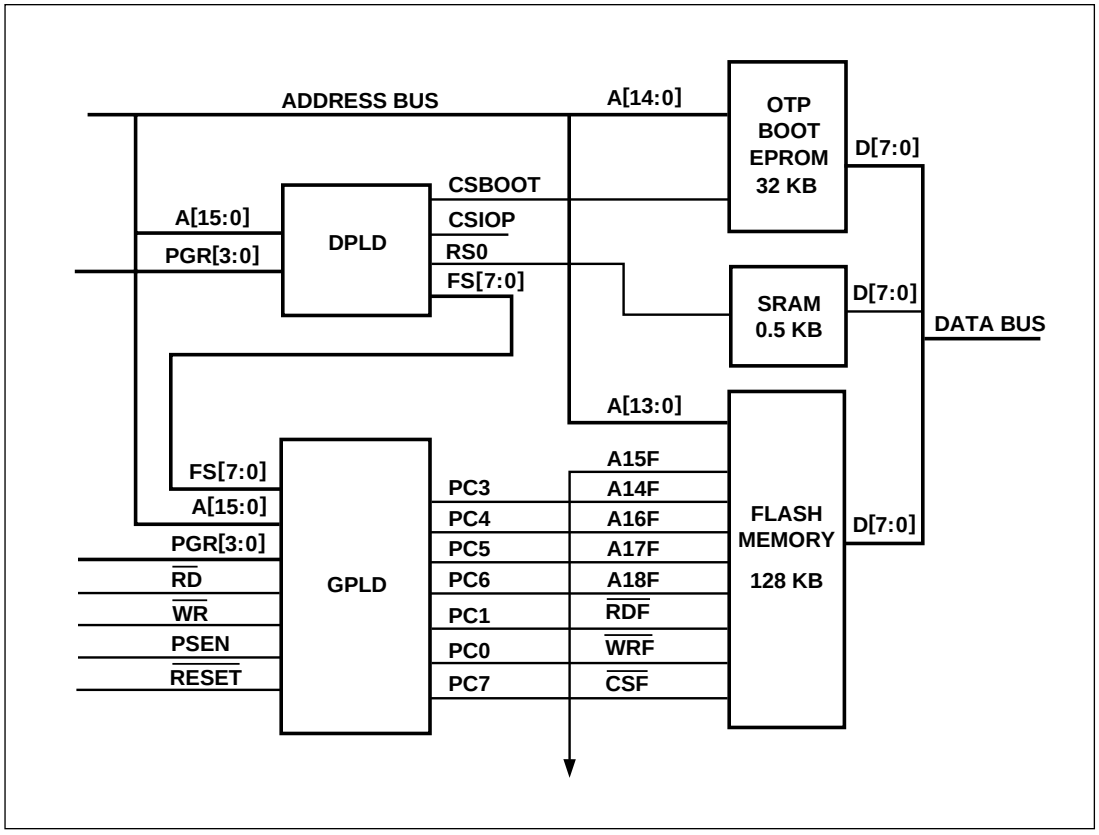


Table 24. Flash Memory Control Signals

Signal Name	Pin/Macrocell	Function	Example Equations Based on the 8031 Bus
$\overline{WRF}$	Pin PC0	Write input	WRF = wr;
$\overline{RDF}$	Pin PC1	Read input	RDF = ! (!rd # !psen);
A14F	Pin PC3	Flash memory A14 input	A14F = A14 & PGR3
A16F	Pin PC4	Flash memory A16 input	A16F = FCS1 # FCS3 # FCS5 # FCS7;
A17F	Pin PC5	Flash memory A17 input	A17F = FCS2 # FCS3 # FCS6 # FCS7;
A18F	Pin PC6	Flash memory A18 input	A18F = FCS4 # FCS5 # FCS6 # FCS7;
$\overline{CSF}$	Pin PC7	Flash memory select	!CSF = FCS0 # FCS1 # FCS2 # FCS3 # FCS4 # FCS5 # FCS6 # FCS7;

Memory Blocks (cont.)

Memory Select for 8031 Microcontrollers

The 8031 family of microcontrollers have a separate address space for program memory (enabled by PSEN) and data memory (enabled by RD). Normally, the Boot EPROM would lie in program address space and the SRAM would lie in data address space. The PSD813FN/FH allows the Boot EPROM and SRAM address space to reside in program space, data space or both. This flexibility enables several system designs. For example, if the user desires to execute a program that resides in SRAM, the SRAM would have to occupy program address space (enabled by PSEN). Likewise, the user may devote a block of Boot EPROM to contain data lookup tables, requiring the Boot EPROM to occupy data address space (enabled by RD).

The internal PSD Boot EPROM and SRAM each have their own output enable. Combinations of PSEN and RD drive these output enables and are determined by bits set at Run-Time by the MCU in the VM register (see Table 25). The schematic representation can be seen in Figure 19 and the action of bit 0 and bit 1 of the VM register is shown.

There are four modes of operation that can be selected by the MCU at Run-Time as shown in Table 25. All of these modes assume there are no overlapping address assignments for blocks of Boot EPROM and SRAM. These blocks of memory may reside in the same 64K program or data space, but not share any physical addresses within the 64K. Example 1: Boot EPROM block 0 and SRAM cannot both start at address 0000. Example 2: Boot EPROM block 2 in program space and Boot EPROM block 3 in data space cannot both start at address 8000).

- **Separate Space Mode**

  Program memory space is separate from data memory space. This default state ties the Boot EPROM output enable to PSEN only, and ties the SRAM output enable to RD only.

- **Combined Program Space Mode**

  This mode allows the SRAM to reside in program space (to be enabled by PSEN as well as RD).

- **Combined Data Space Mode**

  This mode allows the Boot EPROM to reside in data space (to be enabled by RD as well as PSEN).

- **Combined Space Mode**

  This mode allows both the Boot EPROM and SRAM to reside in either program space or data space (either memory may be accessed by PSEN or RD).

Table 25. VM Register

VM Reg Bit 1 RD_EN	VM Reg Bit 0 PSEN_EN	Run-Time Mode
0	0	Separate Space Mode (default at reset)
0	1	Combined Program Space Mode
1	0	Combined Data Space Mode
1	1	Combined Space Mode

NOTE: Bits 6-2 are not used. Use of bit 7 is described in the Peripheral I/O mode section.

Memory Blocks (cont.)

Memory Select for 8031 Microcontrollers (cont.)

Mixed Mode is another mode of operation that is not set by the MCU at Run-Time but is set by an NVM bit from the PSD device programming file that PSDsoft creates. This mode deals with overlapping Boot EPROM addresses such as when two PSD Boot EPROM blocks start at address 8000, but one is in program space and the other is in data space.

❑ **Mixed Mode**

This mode allows individual Boot EPROM blocks with overlapping addresses to be configured in either program space or data space. The CSBOOTx chip select equations for the overlapping blocks must be qualified with the 8031 RD input. An active low RD will select Boot EPROM blocks in data space and disable the blocks in program space. The NVM bit is automatically set by PSDsoft if the keyword RD is used in any CSBOOTx equation. This NVM bit is equivalent to setting Bit 1 in the VM register, only it is there from system power-up. Here are some example CSBOOTx equations:

```
CSBOOT0  =  address >= ^h8000 & address <= ^h1FFF & RD; “resides program space
CSBOOT1  =  address >= ^h8000 & address <= ^h1FFF & !RD; “resides data space
```

There are two reasons to use this mode. First, this mode must be used if PSD Boot EPROM addresses overlap each other but reside in different spaces. Second, this mode can be used if PSD Boot EPROM block addresses do not overlap but it is desired to have one or more Boot EPROM blocks reside in data space and the designer wants this to be set in NVM configuration from power up (not set at Run-Time). IMPORTANT: For Boot EPROM blocks that reside in data space, the access time is calculated from RD valid to data valid. The designer must ensure that EPROM access time is sufficient for the system, or else use the VM register bit 1 without overlapping addresses.

Memory Blocks (cont.)

Figure 18. 8031 Memory Modes – Separate Space Mode

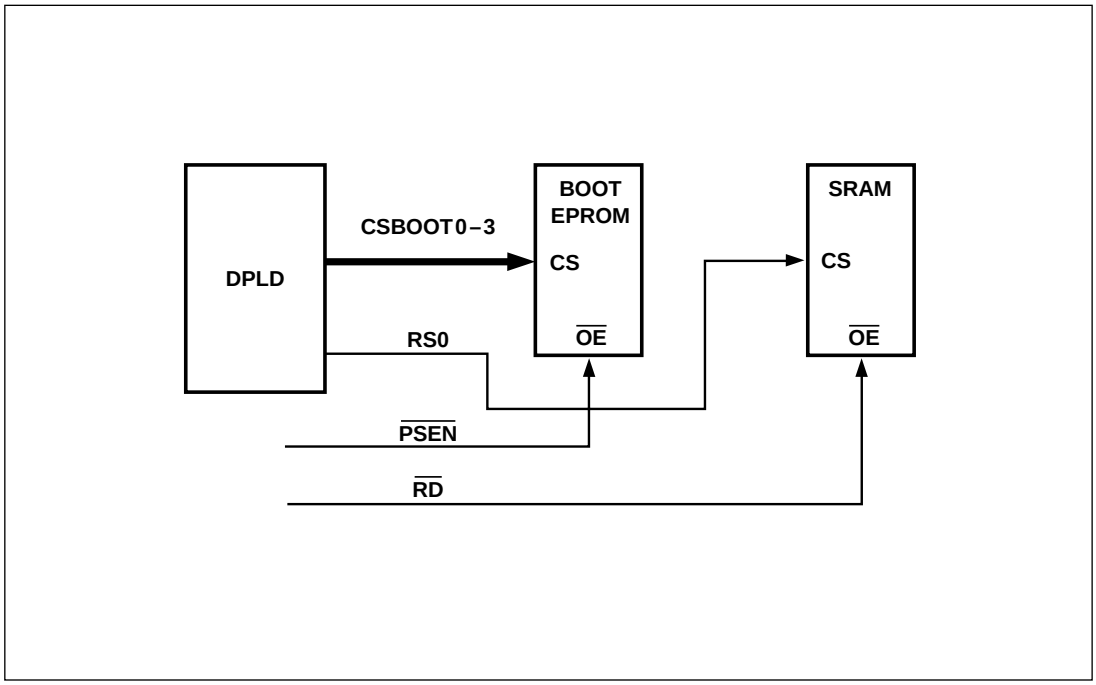
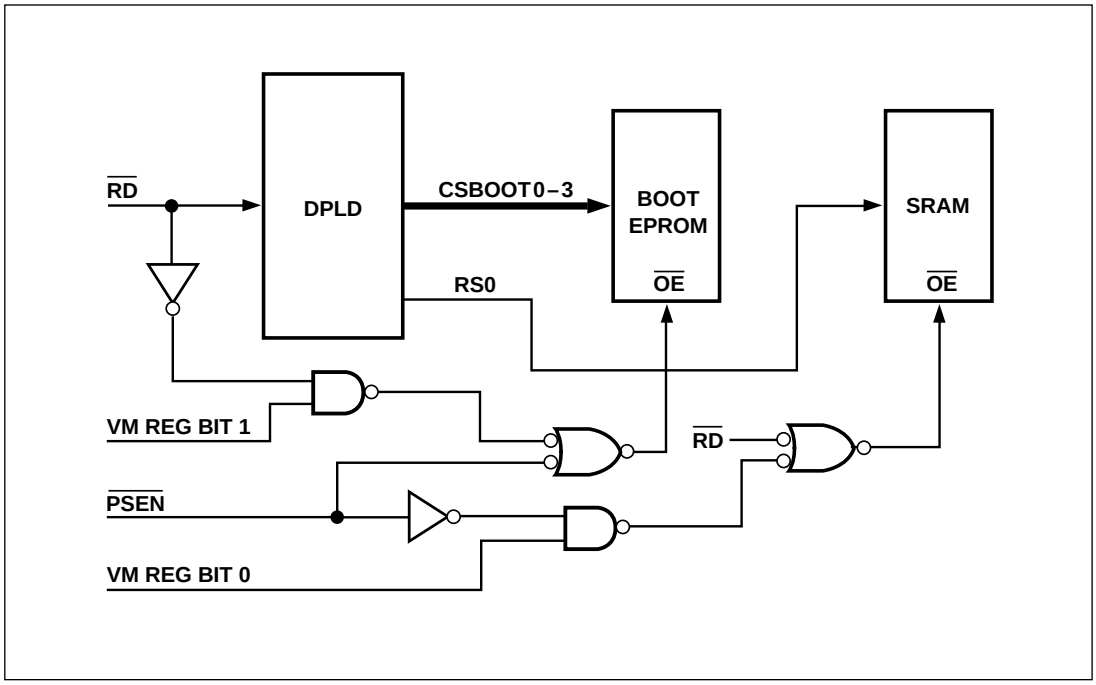


Figure 19. 80C31 Memory Mode – Combined Space Mode



Power Management Unit

The PSD813FN/FH offers a number of configurable power savings options. The designer may choose a wide array of options that range from excellent power savings with no performance loss to maximum power savings at the expense of a slight performance loss. These power saving functions are designed to occur automatically in the background and most can be set up by the MCU at Run-Time. Note that these features only apply to the PSD6XX portion of this Multi-Chip Module. The monolithic PSD8XXF members will apply these power reduction features to the NVM sections as well.

The Automatic Power Down (APD) Mode

APD logic puts the PSD813FN/FH into power savings mode by monitoring the activity of the address strobe (ALE/AS). The APD unit is a down-counter that is reset by the active state of ALE/AS. See Figure 20. This APD counter is clocked by an external free running clock signal that is routed in on the CLKIN pin (Port D-PD1). The APD counter will reach terminal count after 15 transitions of CLKIN. If ALE/AS is not active for 15 cycles of CLKIN, the APD counter will reach terminal count and force Power Down Mode if enabled. The PSD will come out of Power Down mode immediately after the first active pulse of ALE/AS with no performance penalty.

During Power Down mode, the PSD Boot EPROM, SRAM, and MCU bus interface is disabled. The GPLD and ECSPLD sections operate as normal during Power Down mode. Table 26 shows the effects of Power Down mode on PSD I/O.

Table 26. Power Down Effect on Ports

Port Function	Pin Level
MCU I/O	No Change
PLD Out	No Change
Address Out	Undefined
Data Port	Hi-Z Tri-State
Peripheral I/O	Hi-Z Tri-State

APD functions are enabled by the MCU at Run-Time using the Power Management Mode Registers PMMR0 and PMMR1 as shown in Table 28. Figure 21 shows a typical flow for mode setup. Power Down mode may also be achieved by deasserting the CSI input as described later.

Sleep Mode

Sleep Mode is an extension of Power Down mode which provides maximum power savings at the expense of a small performance loss. If Sleep mode is enabled, Sleep mode will occur when Power Down mode occurs and exit when Power Down mode exits.

In Sleep mode, the GPLD and ECSPLD still monitor inputs and respond to them, however, the GPLD and ECSPLD propagation delays are extended to t_{PD4}. When Sleep mode is exited, the GPLD and ECSPLD will continue to have the extended delay of t_{PD4} for a "wake-up" period of t_{PD5}. Also, the first access of Boot EPROM or SRAM that occurs while coming out of sleep mode will incur an extended access time of t_{LVDV1}. After that, PSD EPROM and SRAM access times will be normal.

Sleep mode is enabled by the MCU at Run-Time using the Power Management Mode Register PMMR1 as shown in Table 28. Figure 21 also shows a typical flow for mode setup.

Power Management Unit (cont.)

CMiser Bit

The CMiser function reduces DC power consumption of the Boot EPROM and SRAM and is independent of APD logic. When CMiser is enabled, the lowest level of DC power is consumed, however, Boot EPROM and SRAM access times will be extended an additional 10 ns. See the PSD DC Characteristics and MCU read timing specifications in this document for more details.

The CSI Input

Pin PD2 of Port D can be configured in PSDsoft as the PSD chip select input CSI. If configured as such, the CSI pin will invoke Power Down mode (as described above) when its level is a logical one. When CSI is logic zero, the PSD functions normally. The CSI function is independent of any Run-Time power saving options. If Power Down mode is activated from CSI, exit from this mode is identical to Power Down mode activated by the APD logic.

Input Clock

If the PSD is configured to use the CLKIN pin (Port D PD1) for use in the PLD AND array and Output MicroCells, this clock signal may be disabled during Power Down mode to further reduce power consumption. This feature is enabled by the MCU and Run-Time using the PMMR0 register as shown in Table 28. Note that even when the clock signal CLKIN is blocked by this feature, the clock signal is still active at the APD down-counter.

SRAM Standby Mode

The PSD SRAM has a dedicated VSTBY pin (Port C PC2) that can be connected to an external battery. When system V_{CC} falls below the battery voltage at the VSTBY pin, the PSD will automatically connect VSTBY as the power source for the PSD SRAM. The SRAM standby current (I_{STBY}) is typically 0.5 µA and the minimum data retention voltage is 2.0 volts. Note: Pin PC2 should be grounded if not used as VSTBY.

Table 27. Summary of PSD813FN/FH Timing and Standby Current During Power Down and Sleep Mode

Mode	PLD Propagation Delay	PLD Recovery Time to Normal Operation	Access Time	Access Recovery Time to Normal Access
Power Down	Normal tpd (Note 1)	0	No Access	tLVDV
Sleep	t_{PD4} (Note 2)	t_{PD5} (Note 3)	No Access	tLVDV1

NOTES: 1. Power Down does not affect the operation of the PLD.
2. In Sleep Mode any input to the PLD will have a propagation delay of t_{PD4}.
3. PLD recovery time to normal operation after existing Sleep Mode. An input to the PLD during the transition will have a propagation delay of t_{PD5}.

Power Management Unit (cont.)

Figure 20. APD Logic Block

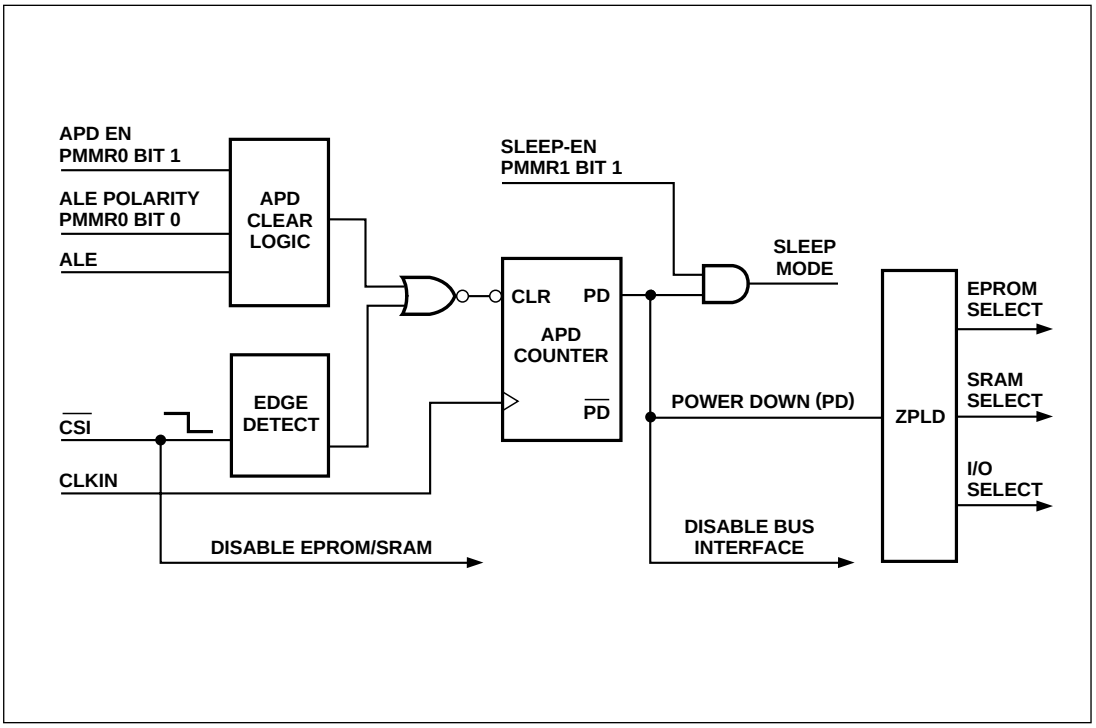
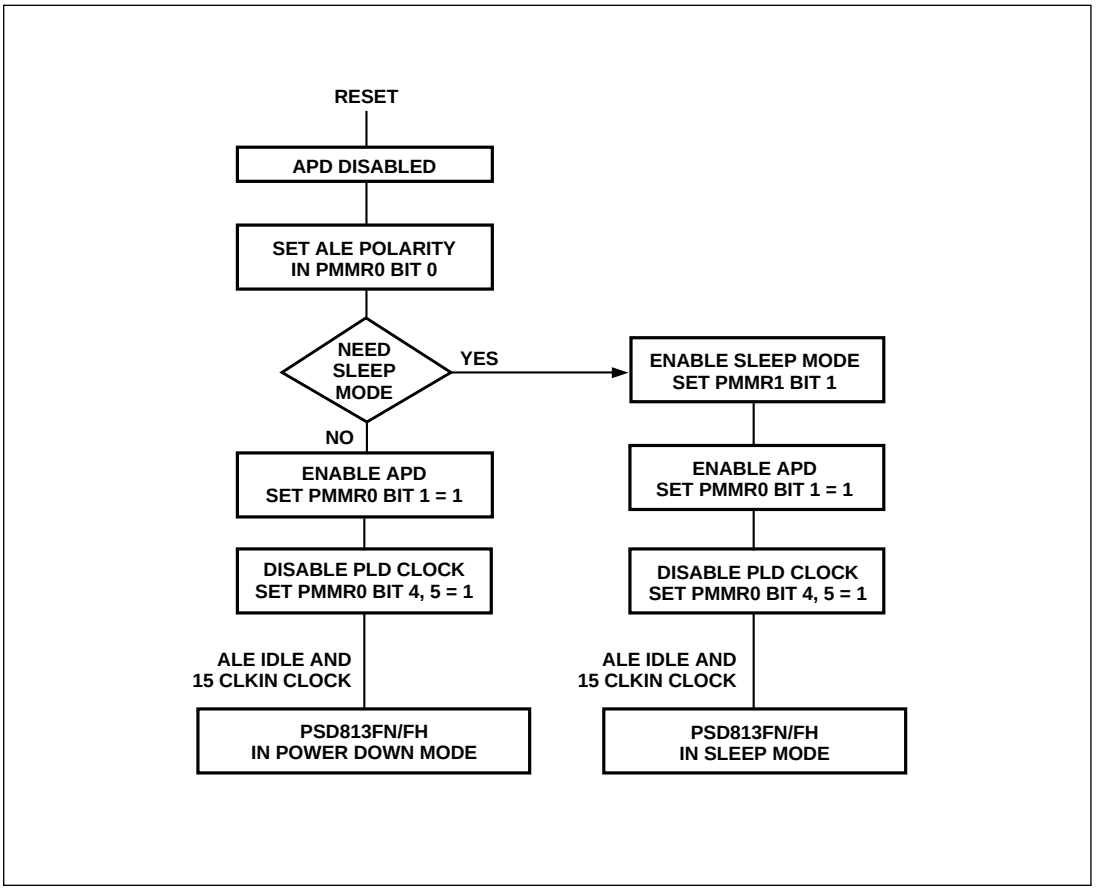


Figure 21. Enable Power Down Flow Chart



Power Management Unit (cont.)

Table 28. Power Management Mode Registers (PMMR0, PMMR1)**

PMMR0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	PLD Mcell clk	PLD Array clk	*	CMiser	APD Enable	ALE PD Polarity
		1 = off	1 = off		1 = on	1 = on	1 = high

*Bits 3, 6 and 7 are not used, and should set to 0.

**Both the PMMR0 and PMMR1 register bits are clear to zero following power up. Subsequent reset pulses will not clear the registers.

Bit 0 0 = ALE power down polarity low
1 = ALE power down polarity high

Bit 1 0 = Automatic Power Down (APD) is disabled
1 = Automatic Power Down (APD) is enabled

Bit 2 0 = EPROM/SRAM CMiser is off
1 = EPROM/SRAM CMiser is on

Bit 4 0 = CLKIN input to the PLD AND array is connected
1 = CLKIN input to PLD AND array is disconnected

Bit 5 0 = CLKIN input to the PLD Micro⇔Cells is connected
1 = CLKIN input to PLD Micro⇔Cells is disconnected

PMMR1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
*	*	*	*	*	*	Sleep Mode Enable	*
						1 = on	

*Unused bits should be set to 0.

Bit 1 0 = Sleep Mode is Disabled
1 = Sleep Mode is Enabled

Table 29. APD Counter Operation

APD Enable Bit	ALE PD Polarity	ALE Level	APD Counter
0	X	X	Not Counting
1	X	Pulsing	Not Counting
1	1	1	Counting (Generates PDN after 15 Clocks)
1	0	0	Counting (Generates PDN after 15 Clocks)

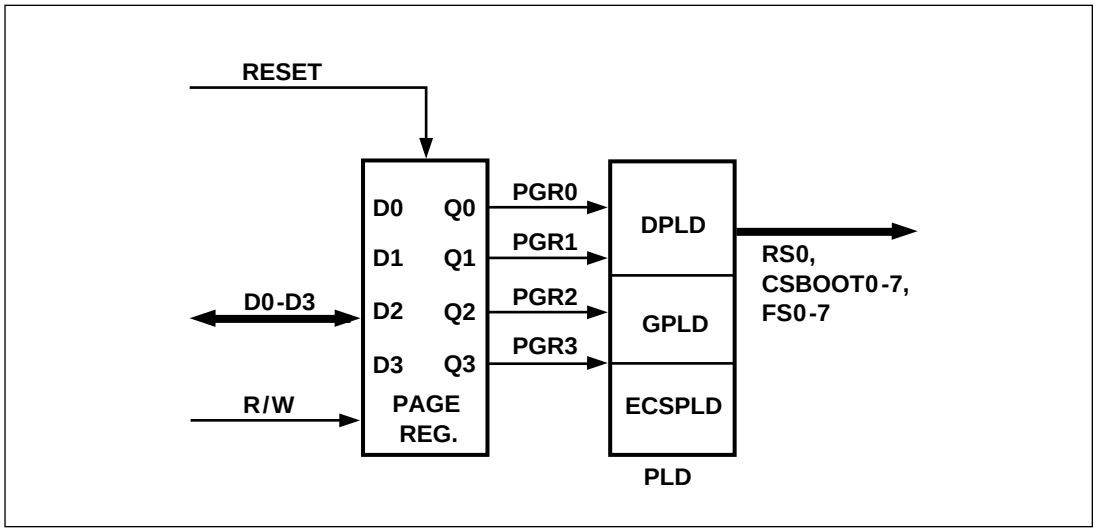
Other Features

Page Register

The four-bit Page Register increases the addressing capability of the microcontroller by a factor of 16. The contents of the Register can also be read by the microcontroller. The outputs of the Page Register (PGR0-PGR3) are inputs to the PLD and can be included in the Flash, Boot EPROM, or SRAM chip select equations.

Figure 24 shows the Page Register. The four Flip-Flops in the Register are connected to the internal data bus D0 – D3. The microcontroller can write to or read from the Page Register. The Register can operate as an independent register and used in general purpose logic if page expansion is not needed.

Figure 22. Page Register



Reset Input

The PSD813FN/FH has an active low reset input which loads internal configurations and clear some of the registers. Figure 33 shows the reset timing requirement. The active low range has a minimum t_{NLNH} duration. After the rising edge of reset, the PSD813FN/FH remains in the reset state during t_{OPR} range. The device must be reset at power-up prior to use. IMPORTANT: The PSD must be out of the reset condition prior to or concurrent with the MCU coming out of reset.

While the reset input is active, the PLD is active and the outputs are determined by the PSDabel equations. The chip status during reset and power down is shown in Table 30.

Other Features (cont.)

Table 30. Chip Status During Reset and Power Down Mode

Port Configuration	Reset	Power Down Mode
MCU I/O	Input	Unchanged
PLD Output	Active	Depends on inputs to the PLD
Address Out	Tri-stated	Not defined
Data Port	Tri-stated	Tri-stated
Peripheral I/O	Tri-stated	Tri-stated

Register	Reset	Power Down Mode
PMMR0 & 1	Cleared (power up reset) Unchanged (warm reset)	Unchanged
Micro⇔Cells Flip-Flop	Unchanged*	Unchanged*
All other registers	Cleared to “0”	Unchanged

*The Micro⇔Cell Flip-Flop can be cleared or set by the reset input or the PDN (Power Down) signal, depending on the .re and .pr equations that are defined in the PSDabel file.

Security Protection

The PSD813FN/FH has a programmable security bit which acts as a duplication barrier. When the bit is set, the contents of the Flash and Boot EPROM, non-volatile configuration bits, and the PLDs cannot be read by device programmers.

The security bit is set through the PSDsoft Software and is embedded in the compiled output file. The security bit is UV erasable and a secured windowed part can be erased and re-programmed.

Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature	CLDCC	– 65	+ 150	°C
		PLDCC	– 65	+ 125	°C
	Operating Temperature	Commercial	0	+ 70	°C
		Industrial	– 40	+ 85	°C
		Military	– 55	+ 125	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Programming Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection		>2000		V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	V_{CC} Tolerance
			-15
Commercial	0° C to +70°C	+ 5 V	± 10%

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V

AC/DC Parameters

The following tables describe the AD/DC parameters of the PSD813FN/FH:

- ❑ DC Electrical Specification
- ❑ AC Timing Specification
  - PLD Timing
    - Combinatorial Timing
    - Synchronous Clock Mode
    - Asynchronous Clock Mode
    - Input Micro⇔Cell Timing
  - Microcontroller Timing
    - Read Timing
    - Write Timing
    - Peripheral Mode Timing
    - Power Down and Reset Timing

Following are some issues concerning the parameters presented:

- ❑ In the DC specification the Supply Current is given for different modes of operation. Before calculating the total power consumption, determine the percentage of time that the PSD813FN/FH is in each mode. Also the supply power is considerably different if CMiser is "ON".
- ❑ The AC power component gives the PLD, EPROM, and SRAM mA/MHz specification.
- ❑ In the MCU timing specification add the required time delay when CMiser is "ON".

DC Characteristics (5 V ± 10% Versions)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		All Speeds	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		4.5 V < V_{CC} < 5.5 V	2		V_{CC} +.5	V
V_{IL}	Low Level Input Voltage		4.5 V < V_{CC} < 5.5 V	–0.5		0.8	V
V_{IH1}	Reset High Level Input Voltage		(Note 1)	.8 V_{CC}		V_{CC} +.5	V
V_{IL1}	Reset Low Level Input Voltage		(Note 1)	–.5		.2 V_{CC} –.1	V
V_{HYS}	Reset Pin Hysteresis			0.3			V
V_{OL}	Output Low Voltage		I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
			I_{OL} = 8 mA, V_{CC} = 4.5 V		0.15	0.45	V
V_{OH}	Output High Voltage Except VBATon, CEout		I_{OH} = –20 µA, V_{CC} = 4.5 V	4.4	4.49		V
			I_{OH} = –2 mA, V_{CC} = 4.5 V	2.4	3.9		V
V_{SBY}	SRAM Standby Voltage			2.0		V_{CC}	V
I_{SBY}	SRAM Standby Current		V_{CC} = 0 V		0.5	1	µA
I_{IDLE}	Idle Current (V_{STBY} Pin)		V_{CC} > V_{SBY}	–0.1		0.1	µA
V_{DF}	SRAM Data Retention Voltage		Only on V_{STBY}	2			V
I_{SB}	Standby Supply Current	Power Down Mode	$\overline{CSI}$ >V_{CC} –.3 V (Note 2)		50	100	µA
		Sleep Mode	$\overline{CSI}$ >V_{CC} –.3 V (Note 3)		25	50	µA
I_{LI}	Input Leakage Current		V_{SS} < V_{IN} > V_{CC}	–1	±.1	1	µA
I_{LO}	Output Leakage Current		.45 < V_{IN} > V_{CC}	–10	±5	10	µA
I_{CC} (DC) (Note 4)	Operating Supply Current	PLD Only	f = 0 MHz		400	700	µA/PT
		EPROM Adder	CMiser = ON and Not Selected		0	0	mA
			CMiser = ON and EPROM Selected (x8 Data Bus)		10	15	mA
			CMiser = OFF		15	20	mA
		Flash DC Adder	During Flash Read, f = 0 MHz		10	18	mA
			During Flash Erase/Write, f = 0 MHz		25	50	mA
		SRAM Adder	SRAM Not Selected		0	0	mA
			CMiser = ON, SRAM Selected (x8 Data Bus)		25	40	mA
			CMiser = OFF		15	20	mA
I_{CC} (AC)	PLD				2	3	mA/MHz
	EPROM or SRAM				2		mA/MHz
	Flash AC Adder				2		mA/MHz

NOTES: 1. Reset input has hysteresis. V_{IL1} is valid at or below .2V_{CC} –.1. V_{IH1} is valid at or above .8V_{CC}.
2. $\overline{CSI}$ deselected or internal PD is active.
3. Sleep mode bit is set and internal PD is active.
4. I_{OUT} = 0 mA.

PSD813FN/FH AC/DC Parameters – GPLD and ECSPLD Timing (5 V ± 10% Versions)

GPLD and ECSPLD Combinatorial Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-15		PT Aloc	Slew Rate	Unit
			Min	Max			
t_{PD1}	ECSPLD Input Pin to ECSPLD Combinatorial Output	(Notes 1 & 2)		24		Add 3	ns
t_{PD2}	GPLD Input Pin/Feedback to GPLD Combinatorial Output Port C	(Note 2a)		32	Add 2		ns
t_{PD3}	GPLD Input Pin/Feedback to GPLD Combinatorial Output Port A or B	(Note 2a)		34			ns
t_{EA}	GPLD Input to ECSPLD Output Enable	(Notes 2 & 2a)		29		Add 3	ns
	GPLD Input to GPLD Output Enable	(Notes 2a & 2b)		32			ns
t_{ER}	GPLD Input to ECSPLD Output Disable	(Notes 2 & 2a)		29		Add 3	ns
	GPLD Input to GPLD Output Disable	(Notes 2a & 2b)		32			ns
t_{ARP}	GPLD Register Clear or Preset Delay	(Notes 2a & 2b)		33			ns
t_{ARPW}	GPLD Register Clear or Preset Pulse Width	(Notes 2a & 2b)	29				ns
t_{ARD}	GPLD Array Delay	Any Micro⇔Cell		22	Add 2		ns

NOTES: 1. ECSPLD Input pins are A(0:15), PGR(0:3), CNTL(0:2), PDN.
2. ECSPLD Outputs are PA(0:3), PB(0:3), PD(0:2).
2a. GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN. Add 25ns for propagation delay from RSTin pin.
2b. GPLD Outputs are PA(4:7), PB(4:7), PC(0:7).

PSD813FN/FH AC/DC Parameters – GPLD and ECSPLD Timing (5 V ± 10% Versions)

GPLD Micro⇔Cell Synchronous Clock Mode Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-15		PT Aloc	Slew Rate	Unit
			Min	Max			
f_{MAX}	Maximum Frequency External Feedback	$1/(t_S + t_{CO})$		25.00			MHz
	Maximum Frequency Internal Feedback (f_{CNT})	$1/(t_S + t_{CO}–10)$		31.25			MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH} + t_{CL})$		35.71			MHz
t_S	Input Setup Time	(Note 2a)	20		Add 2		ns
t_H	Input Hold Time	(Note 2a)	0				ns
t_{CH}	Clock High Time	Clock Input	15				ns
t_{CL}	Clock Low Time	Clock Input	15				ns
t_{CO}	Clock to Output Delay	Clock Input		22			ns
t_{ARD}	GPLD Array Delay	Any Micro⇔Cell		22	Add 2		ns
t_{MIN}	Minimum Clock Period	$t_{CH} + t_{CL}$	29				ns

GPLD Micro⇔Cell Asynchronous Clock Mode Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-15		PT Aloc	Slew Rate	Unit
			Min	Max			
f_{MAXA}	Maximum Frequency External Feedback	$1/(t_{SA} + t_{COA})$		21.74			MHz
	Maximum Frequency Internal Feedback (f_{CNTA})	$1/(t_{SA} + t_{COA}–10)$		27.78			MHz
	Maximum Frequency Pipelined Data	$1/(t_{CH} + t_{CL})$		35.71			MHz
t_{SA}	Input Setup Time	(Note 2a)	12		Add 2		ns
t_{HA}	Input Hold Time	(Note 2a)	12				ns
t_{CHA}	Clock Input High Time	(Note 2a)	15				ns
t_{CLA}	Clock Input Low Time	(Note 2a)	15				ns
t_{COA}	Clock to Output Delay	(Note 2a)		37			ns
t_{ARD}	GPLD Array Delay	Any Micro⇔Cell		22	Add 2		ns
t_{MINA}	Minimum Clock Period	$1/f_{CNTA}$	43				ns

NOTE: 2a. GPLD Inputs are A(0:15), PGR(0:3), CNTL(0:2), PA(0:7), PB(0:7), PC(0:7), PD(0:2), ALE, PDN. Add 25ns for propagation delay from RSTin pin.

PSD813FN/FH AC/DC Parameters – GPLD and ECSPLD Timing (5 V ± 10% Versions)

Input Micro⇔Cell Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-15		PT Aloc	Unit
			Min	Max		
t_{IS}	Input Setup Time	(Note 2c)	0			ns
t_{IH}	Input Hold Time	(Note 2c)	26			ns
t_{INH}	NIB Input High Time	(Note 2c)	18			ns
t_{INL}	NIB Input Low Time	(Note 2c)	18			ns
t_{INO}	NIB Input to Combinatorial Output Delay	(Note 2c)		59	Add 2	ns

NOTES: 2c. Inputs from Port A, B and C relative to register/latch clock from the PLD. ALE latch timings refer to t_{AVLX} and t_{LXAX}.

Microcontroller Interface – AC/DC Parameters

(5V ± 10% Versions)

Explanation of AC Symbols for PLD Timing.

Example: t_{AVLX} – Time from Address Valid to ALE Invalid.

Signal Letters

A – Address Input
C – CEout Output
D – Input Data
E – E Input
G – Internal WDOG_ON signal
I – Interrupt Input
L – ALE Input
N – Reset Input or Output
P – Port Signal Output
Q – Output Data
R – $\overline{WR}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DS}$, IORD, $\overline{PSEN}$ Inputs
S – Chip Select Input
T – R/$\overline{W}$ Input
W – Internal PDN Signal
B – Vstby Output
M – Output Micro⇔Cell

Signal Behavior

t – Time
L – Logic Level Low or ALE
H – Logic Level High
V – Valid
X – No Longer a Valid Logic Level
Z – Float
PW – Pulse Width

Microcontroller Interface – AC/DC Parameters

Read Timing

Symbol	Parameter	Conditions	-15		CMiser ON	Unit
			Min	Max		
t_{LVLX}	ALE or AS Pulse Width		28		0	ns
t_{AVLX}	Address Setup Time	(Note 4)	10		0	ns
t_{LXAX}	Address Hold Time	(Note 4)	11		0	ns
t_{AVQV}	Address Valid to Data Valid	(Note 4)		150	Add 10	ns
t_{SLQV}	$\overline{CS}$ Valid to Data Valid			150	Add 10	ns
t_{RLQV}	$\overline{RD}$ to Data Valid 8/16-Bit Bus	(Note 3)		40	0	ns
	$\overline{RD}$ to Data Valid 8-Bit Bus, 8031 Separate Mode	(Note 3a)		45	0	ns
t_{RHQX}	$\overline{RD}$ Data Hold Time	(Note 3)	0		0	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	(Note 3)	38		0	ns
t_{RHQZ}	$\overline{RD}$ to Data High-Z	(Note 3)		33	0	ns
t_{EHEL}	E Pulse Width		38		0	ns
t_{THEH}	R/$\overline{W}$ Setup Time to Enable		18		0	ns
t_{ELTL}	R/$\overline{W}$ Hold Time After Enable		0		0	ns
t_{AVPV}	Address Input Valid to Address Output Delay	(Note 5)		48	0	ns

NOTES: 3. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, PSEN (in 8031 combined mode) signals.
3a. $\overline{RD}$ and $\overline{PSEN}$ have the same timing for 8031 separate mode.
4. Any input used to select an internal PSD813FN/FH function.
5. In multiplexed mode latched address generated from ADIO delay to address output on any Port.

Microcontroller Interface – AC/DC Parameters

(5 V ± 10% Versions)

Write/Erase/Program Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-15		EPROM_CMiser ON	Unit
			Min	Max		
t_{LVLX}	ALE or AS Pulse Width		28			ns
t_{AVLX}	Address Setup Time	(Note 6)	10			ns
t_{LXAX}	Address Hold Time	(Note 6)	11			ns
t_{AVWL}	Address Valid to Leading Edge of $\overline{WR}$	(Notes 6 and 8)	30			ns
t_{SLWL}	$\overline{CS}$ Valid to Leading Edge of $\overline{WR}$	(Note 8)	35			ns
t_{DVWH}	$\overline{WR}$ Data Setup Time	(Note 8)	22			ns
t_{WHDX}	$\overline{WR}$ Data Hold Time	(Note 8)	5			ns
t_{WLWH}	$\overline{WR}$ Pulse Width	(Note 8)	28			ns
t_{WHAX}	Trailing Edge of $\overline{WR}$ to Address Invalid	(Note 8)	0			ns
t_{WHPV}	Trailing Edge of $\overline{WR}$ to Port Output Valid	(Note 8)		38		ns
t_{AVPV}	Address Input Valid to Address Output Delay	In 8-Bit Data Bus Mode (Note 7)		48		ns
t_{WHWH1}	Byte Programming Operation	Also includes preprogramming time	14			µs
t_{WHWH2}	Sector Erase Operation	Not 100% tested	2.2			sec
t_{VCS}	V_{CC} Set up Time		50			µs

NOTE: 6. Any input used to select an internal PSD813FN/FH function.
7. In multiplexed mode latched address generated from ADIO delay to address output on any Port.
8. $\overline{WR}$ timing has the same timing as E and $\overline{DS}$ signals.

Microcontroller Interface – AC/DC Parameters

Port A Peripheral Data Mode Read Timing

Symbol	Parameter	Conditions	-15		Unit
			Min	Max	
$t_{AVQV (PA)}$	Address Valid to Data Valid	(Note 9)		62	ns
$t_{SLQV (PA)}$	$\overline{CS}$ Valid to Data Valid			62	ns
$t_{RLQV (PA)}$	$\overline{RD}$ to Data Valid	(Notes 3, 10)		40	ns
	$\overline{RD}$ to Data Valid 8031 Mode			45	ns
$t_{DVQV (PA)}$	Data In to Data Out Valid			26	ns
$t_{QXRH (PA)}$	$\overline{RD}$ Data Hold Time	(Note 3)	0		ns
$t_{RLRH (PA)}$	$\overline{RD}$ Pulse Width	(Note 3)	38		ns
$t_{RHQZ (PA)}$	$\overline{RD}$ to Data High-Z	(Note 3)		33	ns

Port A Peripheral Data Mode Write Timing

Symbol	Parameter	Conditions	-15		Unit
			Min	Max	
$t_{WLQV (PA)}$	$\overline{WR}$ to Data Propagation Delay	(Note 8)		35	ns
$t_{DVQV (PA)}$	Data to Port A Data Propagation Delay	(Note 11)		26	ns
$t_{WHQZ (PA)}$	$\overline{WR}$ Invalid to Port A Tri-state	(Note 8)		33	ns

NOTES: 9. Any input used to select Port A Data Peripheral Mode.
10. Data is already stable on Port A.
11. Data stable on ADIO pins to data on Port A.

Microcontroller Interface – AC/DC Parameters

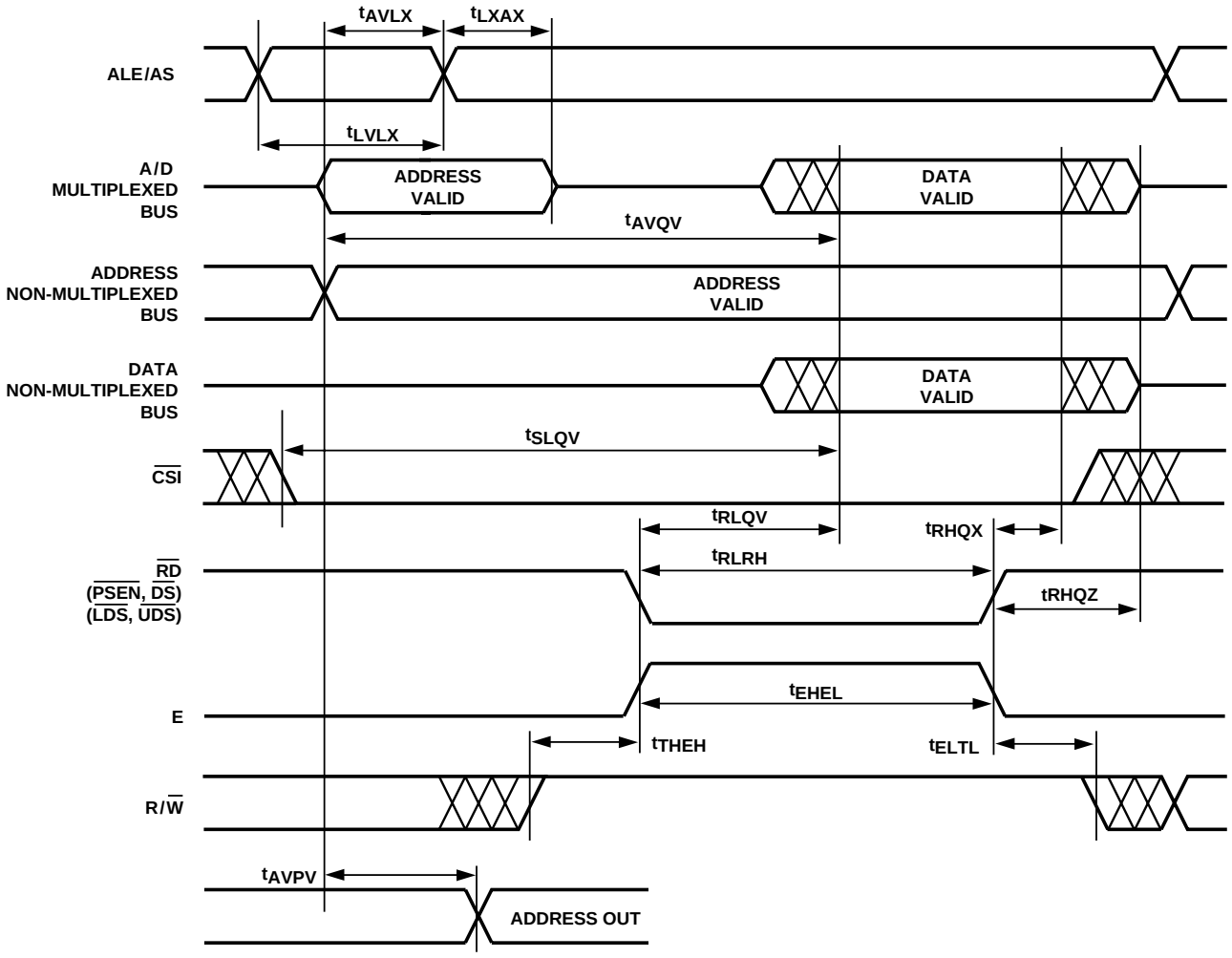
Power Down Timing

Symbol	Parameter	Conditions	-15		Unit
			Min	Max	
t_{LVDV}	ALE Access Time from Power Down			150	ns
t_{LVDV1}	ALE or $\overline{CSI}$ Access Time from Sleep			200	ns
t_{PD4}	GPLD and ECSPLD Propagation Delay in Sleep Mode			600	ns
t_{PD5}	GPLD and ECSPLD Recovery Time After Sleep Mode			250	ns
t_{CLWH}	Maximum Delay from APD Enable to Internal PDN Valid Signal	Using CLKIN Input	15* t_{MIN} (µs)		µs

Reset Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{NLNH}	RESET Active Low Time		150			ns
t_{OPR}	RESET High to Operational Device				120	ns

Figure 23. Read Timing



*t_{AVLX} and t_{LXAX} are not required for 80C251 in Page Mode or 80C51XA in Burst Mode.

Figure 24. Write Timing

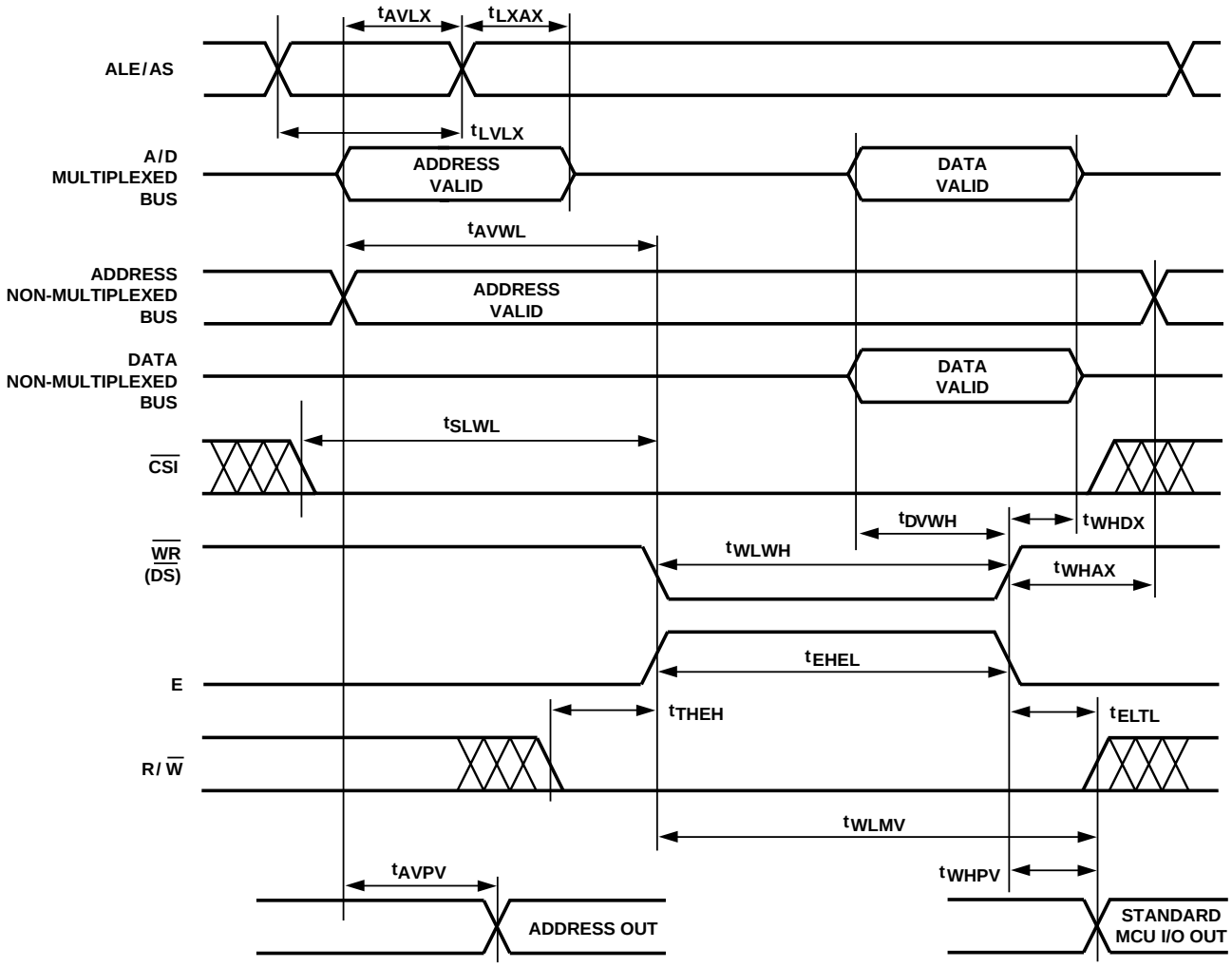


Figure 25. Peripheral I/O Read Timing

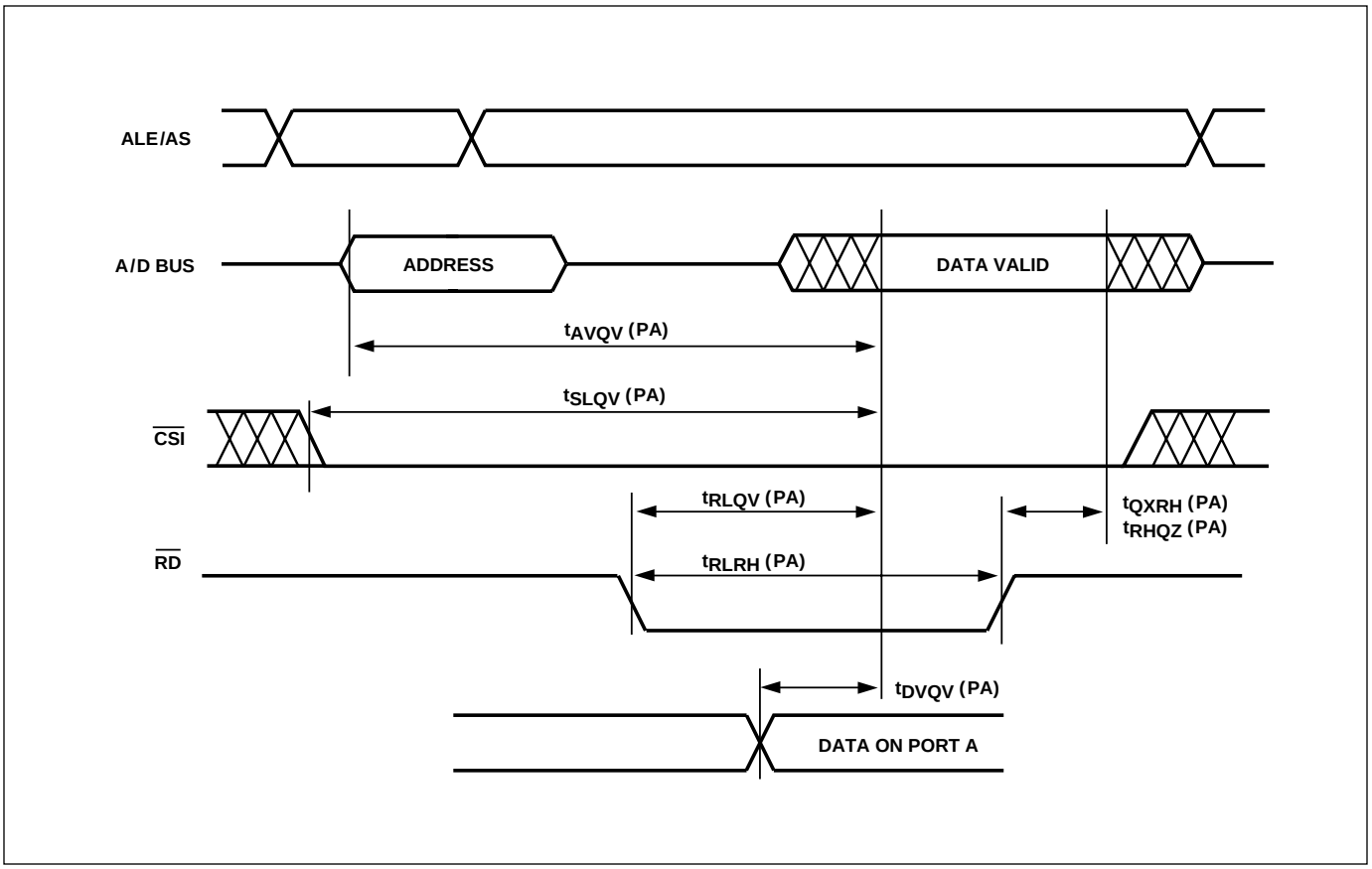


Figure 26. Peripheral I/O Write Timing

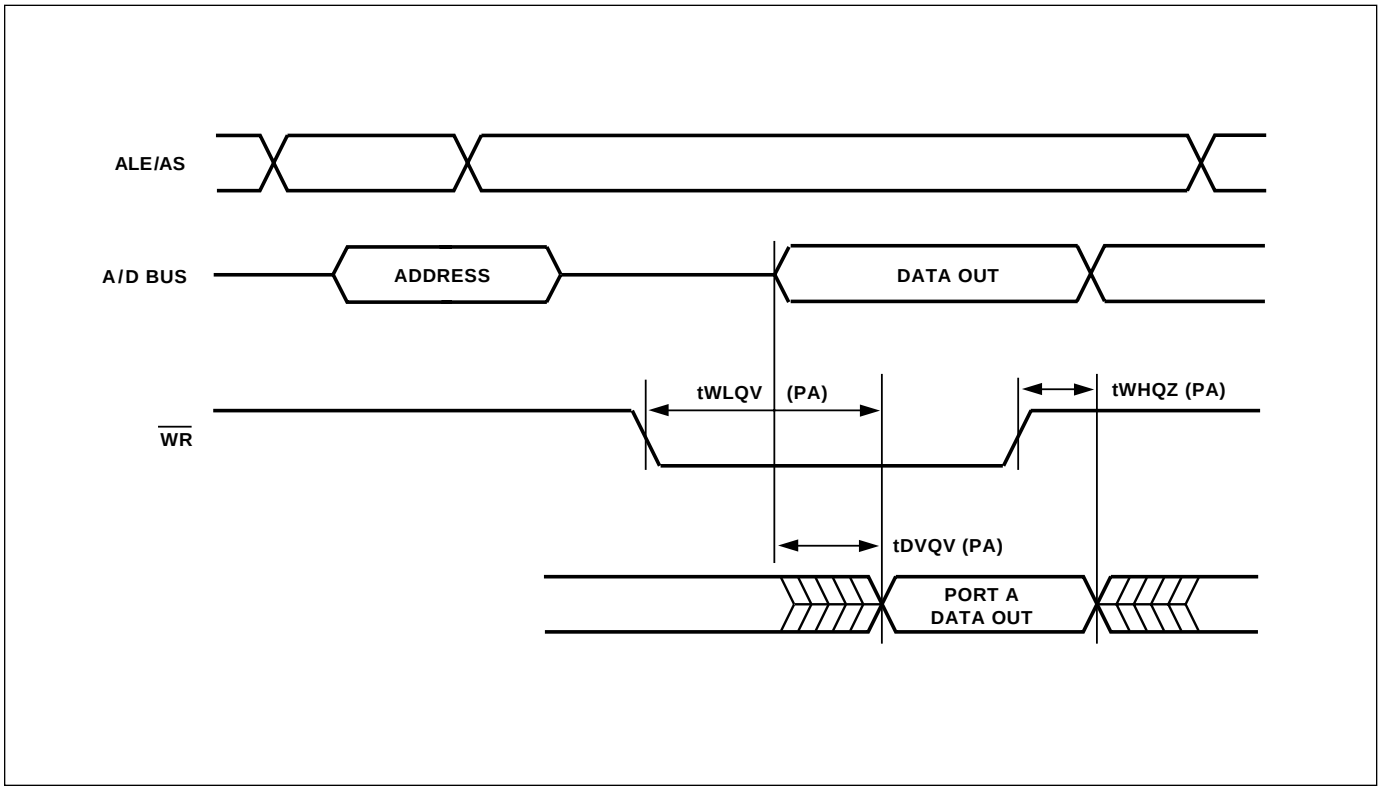


Figure 27. Combinatorial Timing – PLD

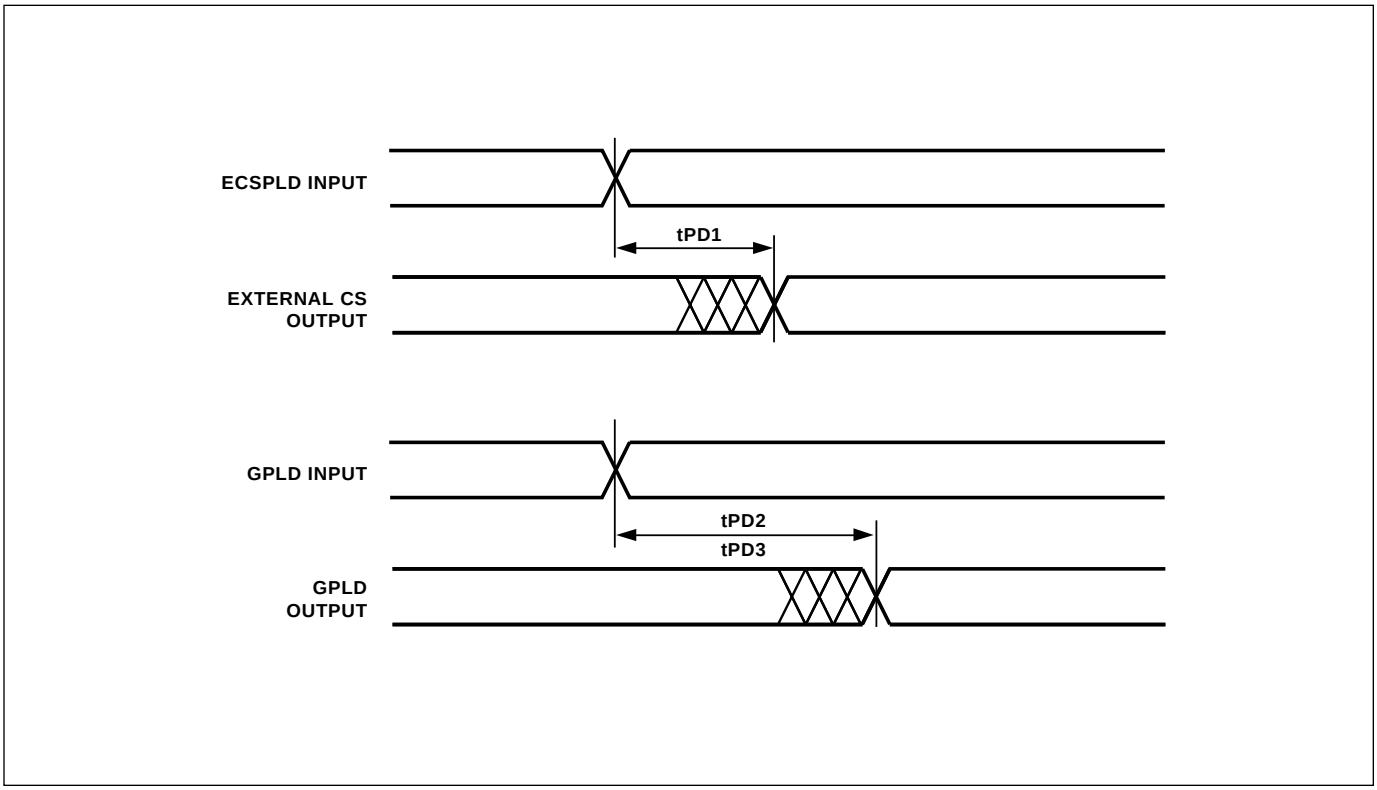


Figure 28. Synchronous Clock Mode Timing – PLD

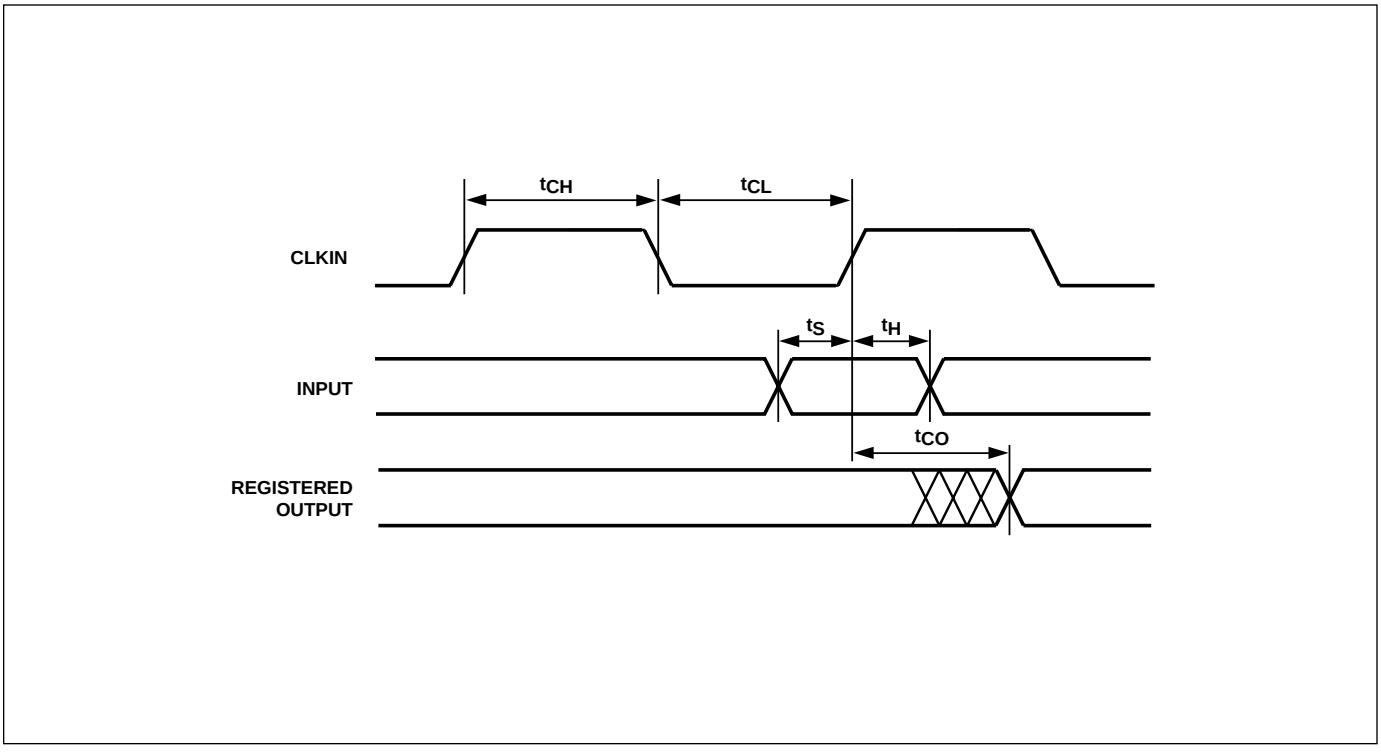


Figure 29. Asynchronous Clock Mode Timing (Product-Term Clock)

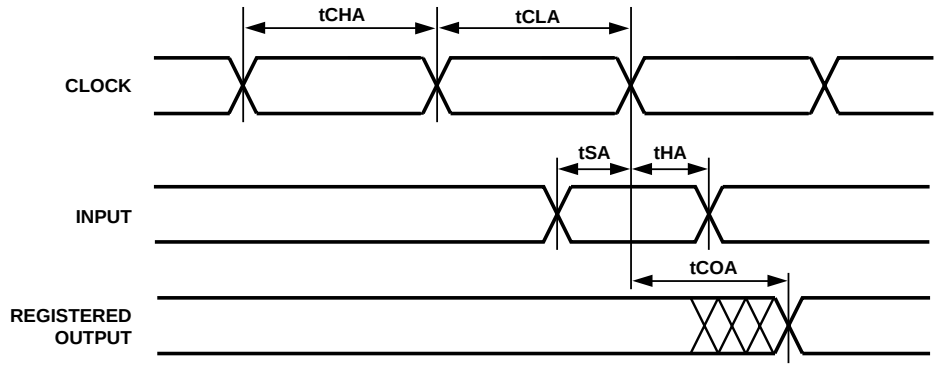


Figure 30. Input Micro⇔Cell Timing (Product-Term Clock)

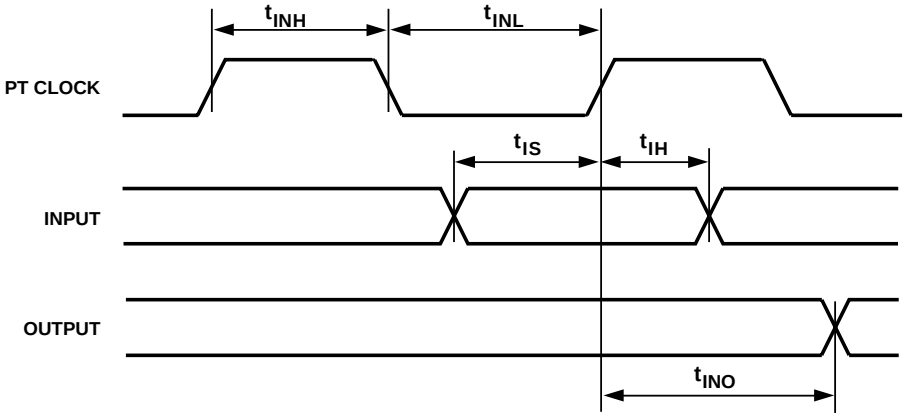


Figure 31. Input to Output Disable/Enable

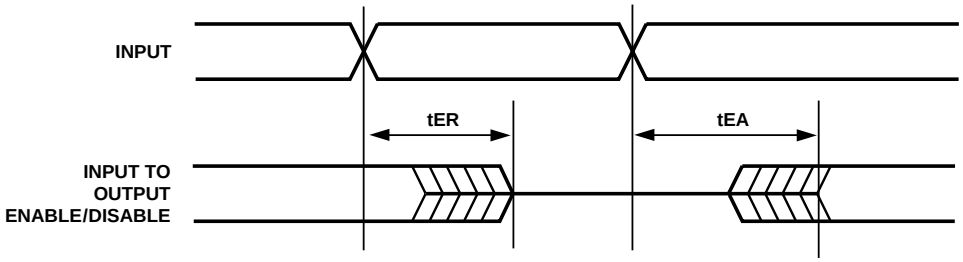


Figure 32. Asynchronous Reset/Preset

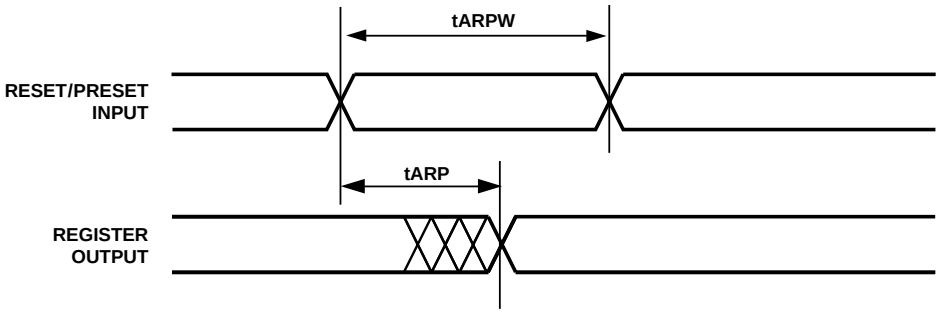


Figure 33. Reset Timing

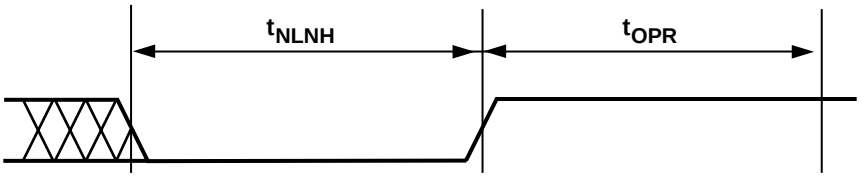
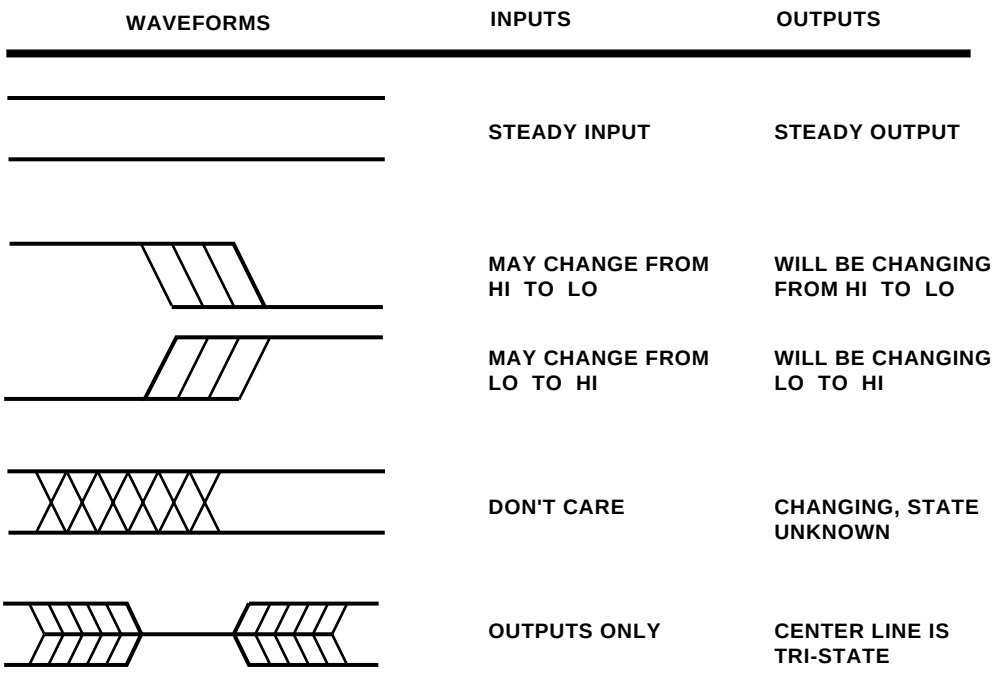


Figure 34. Key to Switching Waveforms



Pin Capacitance

T_A = 25 °C, f = 1 MHz

Symbol	Parameter[1]	Conditions	Typical[2]	Max	Unit
C_{IN}	Capacitance (for input pins only)	V_{IN} = 0 V	4	6	pF
C_{OUT}	Capacitance (for input/output pins)	V_{OUT} = 0 V	8	12	pF
C_{VPP}	Capacitance (for WR/V_{PP} or R/W/V_{PP})	V_{PP} = 0 V	18	25	pF

NOTES: 1. These parameters are only sampled and are not 100% tested.
2. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 35. AC Testing Input/Output Waveform

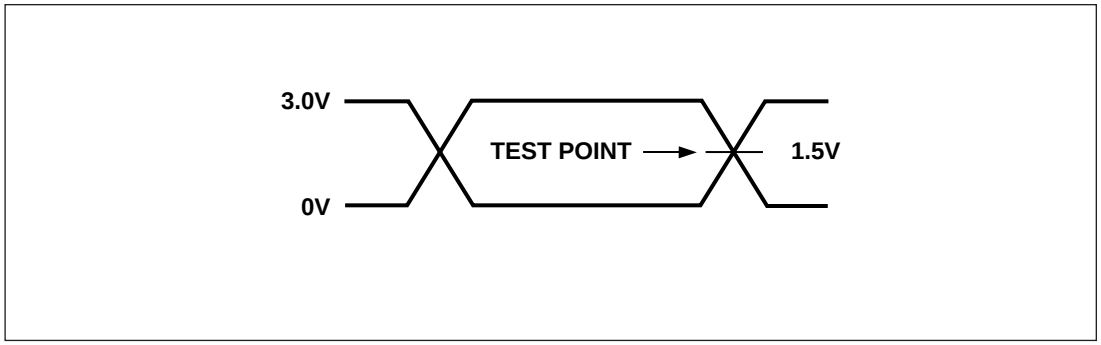
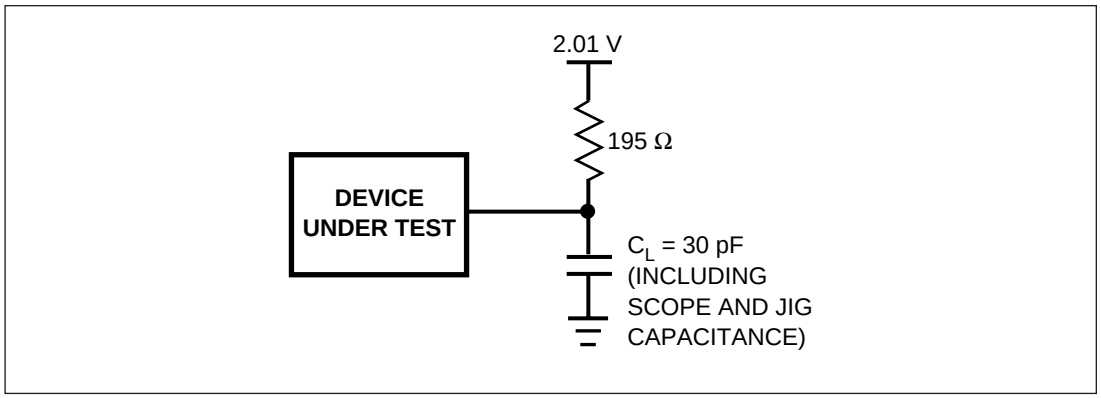


Figure 36. AC Testing Load Circuit



PSD813FN/FH Pin Assignments

Pin No.	Pin Assignments	Pin No.	Pin Assignments
52-Pin PLDCC	52-Pin PLDCC	52-Pin PLDCC	52-Pin PLDCC
1	GND	27	PA2
2	PB5	28	PA1
3	PB4	29	PA0
4	PB3	30	AD0
5	PB2	31	AD1
6	PB1	32	AD2
7	PB0	33	AD3
8	PD2	34	AD4
9	PD1	35	AD5
10	PD0	36	AD6
11	PC7 (CSF)	37	AD7
12	PC6 (A18F)	38	V_{CC}
13	PC5 (A17F)	39	A8
14	PC4 (A16F)	40	A9
15	V_{CC}	41	A10
16	GND	42	A11
17	PC3 (A14F)	43	A12
18	PC2 (Vstby)	44	A13
19	PC1 (RDF)	45	A14
20	PC0 (WRF)	46	A15
21	PA7	47	CNTL0
22	PA6	48	RST
23	PA5	49	CNTL2
24	PA4	50	CNTL1
25	PA3	51	PB7
26	GND	52	PB6

PSD813FN/FH Package Information

Figure 37. Drawing J7 – 52-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)

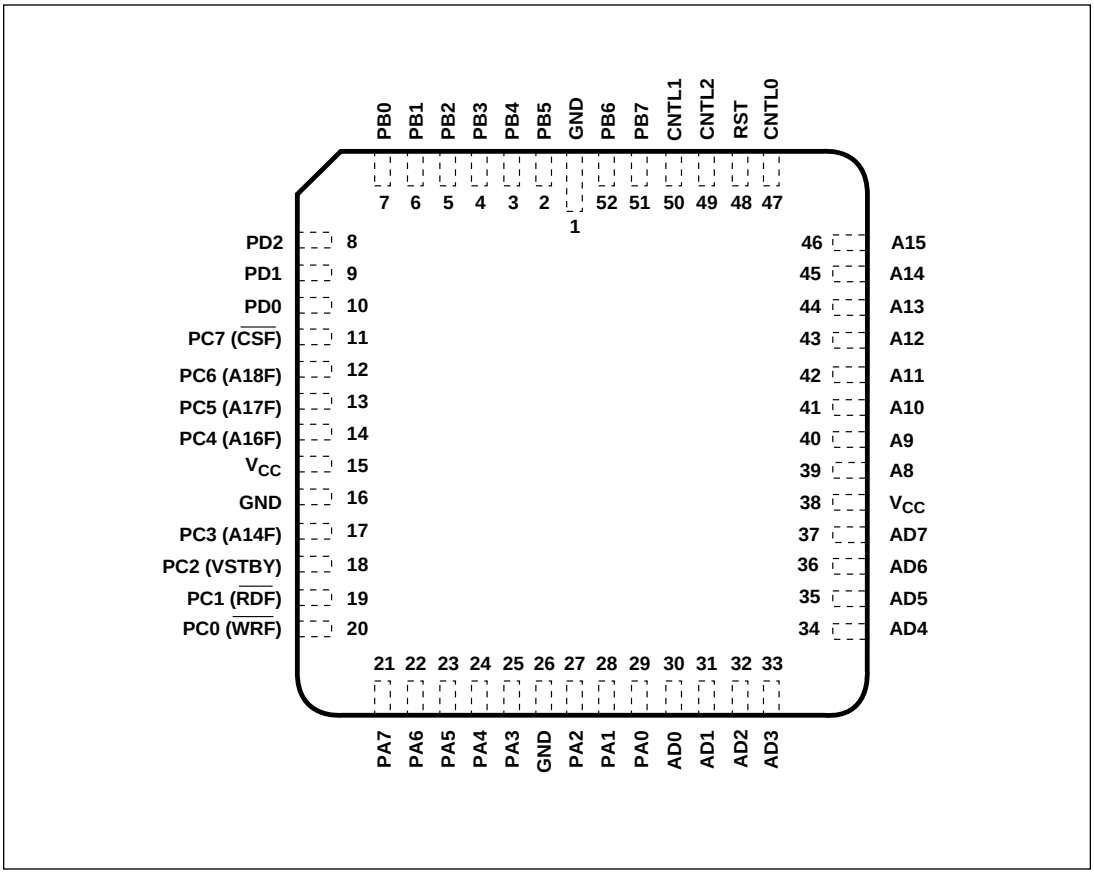
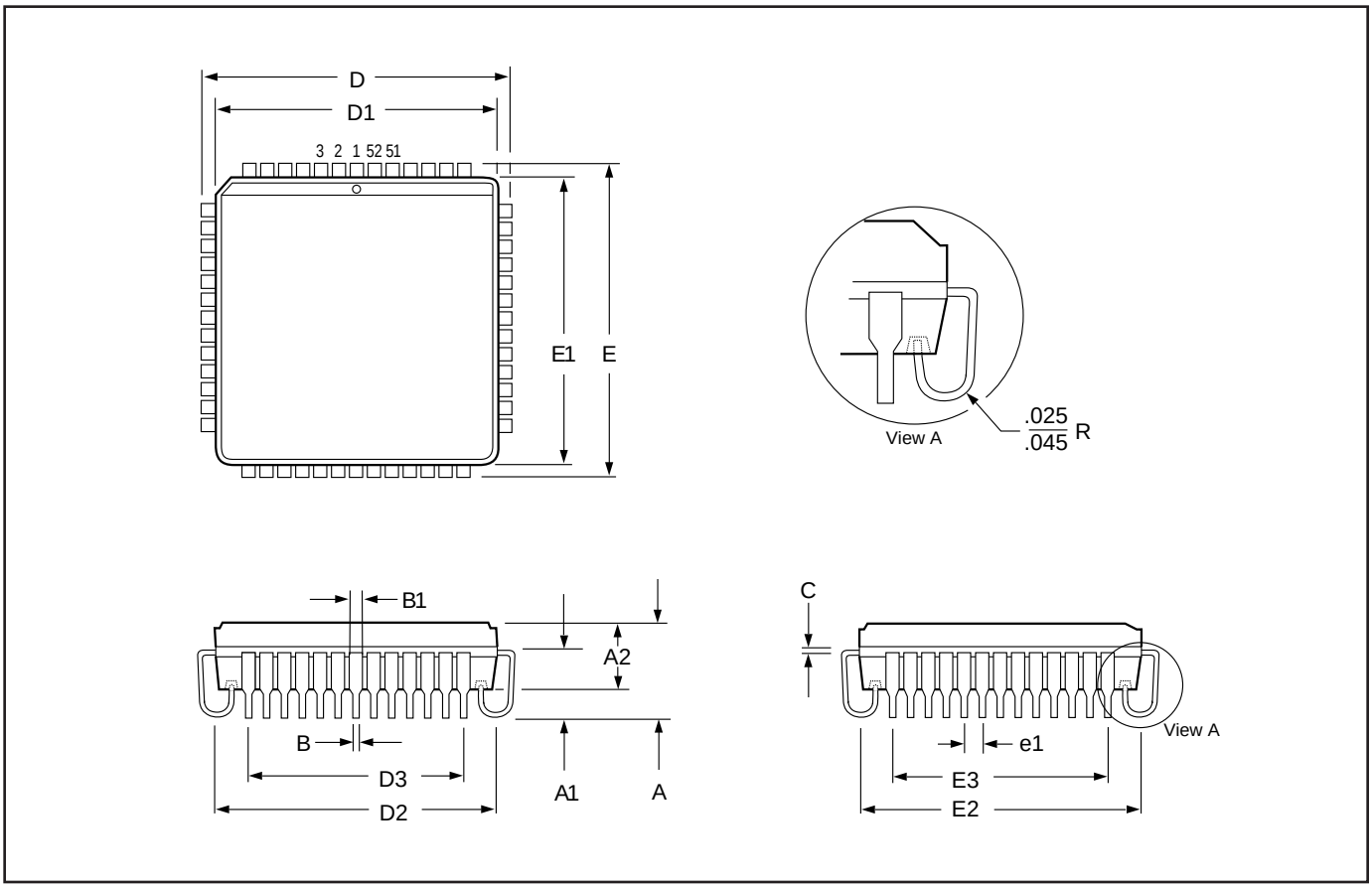


Figure 37A.
Drawing J7 – 52-Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



Family: Plastic Leaded Chip Carrier

	Millimeters			Inches		
Symbol	**Min**	**Max**	**Notes**	**Min**	**Max**	**Notes**
A	4.19	4.57		0.165	0.180	
A1	2.54	2.79		0.100	0.110	
A2	3.66	3.86		0.144	0.152	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.246	0.261		0.0097	0.0103	
D	19.94	20.19		0.785	0.795	
D1	19.05	19.15		0.750	0.754	
D2	17.53	18.54		0.690	0.730	
D3	15.24		Reference	0.600		Reference
E	19.94	20.19		0.785	0.795	
E1	19.05	19.15		0.750	0.754	
E2	17.53	18.54		0.690	0.730	
E3	15.24		Reference	0.600		Reference
e1	1.27		Reference	0.050		Reference
N	52			52		

020197R1

Appendix A – Flash Memory

Description

The PSD813FN/FH has a non-volatile Flash memory that may be erased electrically at the sector level, and programmed Byte-by-Byte.

Organization

The Flash Memory organization is 512K x 8 bits (only 128K x 8 is used) with Address lines A0 – A18 and Data Inputs/Outputs D0 – D7. Memory control is provided by Chip Enable (CSF), Output Enable (RDF) and Write Enable (WRF) Inputs.

Erase and Program are performed using embedded algorithms through the internal Program/Erase Controller (P/E.C.).

Data Output bits D7 and D6 provide polling or toggle signals during Automatic Program or Erase to indicate the Ready/Busy state of the internal Program/Erase Controller.

Sectors

Erasure of the memory is in sectors. There are 8 sectors of 64K bytes each in the memory address space. Erasure of each sector takes typically 1.5 seconds and each sector can be programmed and erased over 100,000 cycles. Sector erasure may be suspended, while data is read from other blocks of the memory, and then resumed.

Bus Operations

Five operations can be performed by the appropriate bus cycles: Read Array, Read Electronic Signature, Output Disable, Standby, and Write the Command of an Instruction.

Command Interface

Command Bytes can be written to a Command Interface (C.I.) latch to perform Reading (from the Array or Electronic Signature), Erasure or programming. For added data protection, command execution starts after 4 or 6 command cycles. The first, second, fourth and fifth cycles are used to input a code sequence to the Command Interface. This sequence is equal for all P/E.C. instructions. The command itself and its confirmation – if it applies – are given on the third and fourth or sixth cycles.

Instructions

Seven instructions are defined to perform Reset, Read Electronic Signature, Auto Program, Sector Auto Erase, Auto Bulk Erase, Sector Erase Suspend and Sector Erase Resume. The internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides Data Polling, Toggle, and Status data to indicate completion of Program and Erase Operations.

Instructions are composed of up to six cycles. The first two cycles input a code sequence to the Command Interface which is common to all P/E.C. instructions (see Table 4 for Command Descriptions). The third cycle inputs the instruction set up command instruction to the Command Interface. Subsequent cycles output Signature or the addressed data for Read operations. For added data protection, the instructions for program and sector or bulk erase require further command inputs. For a Program instruction, the fourth command cycle inputs the address and data to be programmed. For an Erase instruction (sector or bulk), the fourth and fifth cycles input a further code sequence before the Erase confirm command on the sixth cycle. Byte programming takes typically 10µs while erase is performed in typically 1.5 seconds.

Erasure of a memory sector may be suspended, in order to read data from another sector, and then resumed. Data Polling, Toggle and Error data may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. When power is first applied or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Array.

Appendix A – Flash Memory (cont.)

Table 1. Operations

Operation	$\overline{CSF}$	$\overline{RDF}$	$\overline{WRF}$	D0 – D7
Read	V_{IL}	V_{IL}	V_{IH}	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	Hi-Z

NOTE: X = V_{IL} or V_{IH}.

Table 2. Electronic Signature

Operation	$\overline{CSF}$	$\overline{RDF}$	$\overline{WRF}$	A0	A1	A6	Addresses	D0 – D7
Manufact. Code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Don't Care	20h
Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	Don't Care	0E2h

NOTE: See RSIG instruction

Device Operation

Signal Descriptions

❑ ***A0 – A18 Address Inputs***

The Address inputs for the memory array are latched during a write operation. When A0, A1 and A6 are Low, the Electronic Signature Manufacturer code is read. When A0 is High and A1 and A6 are Low, the Device code is read. See the RSIG instruction and Table 2.

❑ ***D0 – D7 Data Input/Outputs***

The data input is a byte to be programmed or a command written to the C.I. Both are latched when Chip Enable $\overline{CSF}$ and Write Enable $\overline{WRF}$ are active. The data output is from the memory Array, the Electronic Signature, the Data Polling bit (D7), the Toggle Bit (D6), the Error bit (D5) or the Erase Timer bit (D3). Outputs are valid when Chip Enable $\overline{CSF}$ and Output Enable $\overline{RDF}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

❑ ***$\overline{CSF}$ Chip Enable***

The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{CSF}$ High deselects the memory and reduces the power consumption to the standby level. $\overline{CSF}$ can also be used to control writing to the command register and to the memory array, while $\overline{WRF}$ remains at a low level. Addresses are then latched on the falling edge of $\overline{CSF}$ while data is latched on the rising edge of $\overline{CSF}$.

❑ ***$\overline{RDF}$ Output Enable***

The Output Enable gates the outputs through the data buffers during a read operation.

❑ ***$\overline{WRF}$ Write Enable***

This input controls writing to the Command Register and Address and Data latches. Addresses are latched on the falling edge of $\overline{WRF}$, and Data Inputs are latched on the rising edge of $\overline{WRF}$.

❑ ***V_{CC} Supply Voltage***

The power supply for all operations (Read, Program and Erase).

❑ ***V_{SS} Ground***

V_{SS} is the reference for all voltage measurements.

Device Operation (cont.)

Table 3. Instructions (Note 1)

Mne.	Instr.	Cyc.		1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
RST(3,8)	Reset	1+	**Addr.**(2,0)	X	Read Memory Array until a new write cycle is initiated.					
			Data	0F0h						
RSIG(3)	Read	3+	**Addr.**(2,5)	x5555h	x2AAAh	x5555h	Read Electronic Signature until a new write cycle is initiated. See Note 4.			
			Data	0AAh	55h	90h				
PG	Program	4	**Addr.**(2,5)	x5555h	x2AAAh	x5555h	Program Address	Read Data polling or toggle Bit until Program completes.		
			Data	0AAh	55h	0A0h	Program Data			
SE	Sector Erase	6	**Addr.**(2,5)	x5555h	x2AAAh	x5555h	x2AAAh	x2AAAh	Sector Address	Additional Sector(6)
			Data	0AAh	55h	80h	0AAh	55h	30h	30h
BE	Bulk Erase	6	**Addr.**(2,5)	x5555h	x2AAAh	x5555h	x5555h	x2AAAh	x5555h	Note 7
			Data	0AAh	55h	80h	0AAh	55h	10h	
ES	Erase Suspend	1	**Addr.**(2,5)	X	Read until Toggle stops, then read all the data needed from any sector(s) not being erased then Resume Erase.					
			Data	0B0h						
ER	Erase Resume	1	**Addr.**(2,5)	X	Read Data Polling or Toggle Bit until Erase completes or Erase is suspended another time.					
			Data	30h						

NOTES: 1. Command not interpreted in this table will default to read array mode.
2. X = Don't Care.
3. The first cycle of the RST, RSP or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of read cycles can occur after one command cycle.
4. Signature Address bits A0, A1, A6 at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1, A6 at V_{IL} will output Device code (0E2h).
5. Address bits A16, A17, A18 are don't care for coded address inputs.
6. Optional, additional sectors addresses must be entered within a 80µs delay after last write entry, timeout status can be verified through D3 value. When full command is entered, read Data Polling or Toggle bit until Erase is completed or suspended.
7. Read Data Polling or Toggle bit until Erase completes.
8. A wait time of 5µs is necessary after a Reset command before starting any operation.

Table 4. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Bulk Erase Confirm
30h	Sector Erase Resume/Confirm
80h	Set-up Erase
90h	Read Electronic Signature
0A0h	Program
0B0h	Erase Suspend
0F0h	Reset

Device Operation (cont.)

Table 5. Status Register

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits D5 for Program or Erase Success.
		'0'	Erase on Going	
		DQ	Program Complete	
		DQ	Program on Going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program on Going	Successive read output complementary data on D6 while Programming or Erase operations are going on. D6 remain at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged.
		'-0-0-0-0-0-0-0-'	Program ('0' on D6) Complete	
		'-1-1-1-1-1-1-1-'	Erase or Program ('1' on D6) Complete	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' if P/E.C. has exceeded the specified time limits.
		'0'	Program or Erase on Going	
4		'1'		
		'0'		
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES). An additional sector to be erased in parallel can be entered to the P/E.C.
		'0'	Erase Timeout Period on Going	
2	Reserved			
1	Reserved			
0	Reserved			

NOTE: Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations.

Appendix A – Flash Memory (cont.)

Device Operation (cont.)

Memory Sectors

The sectors of the Flash Memory are shown in Figure 1. The memory array is divided into 8 sectors of 64K bytes. Each sector can be erased separately or any combination of sectors can be erased simultaneously. The Sector Erase operation is managed automatically by the P/E.C. The operation can be suspended in order to read from any another sector, and then resumed.

Operations

Operations are defined as specific bus cycles and signals which allow Memory Read, Command Write, Output Disable, Standby, Read Status Bits, and Electronic Signature Read. They are shown in Tables 1 and 2.

- **Read**
  Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{CSF}$ and Output Enable $\overline{RDF}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. The data read depends on the previous command written to the memory (see instructions RST and RSIG, and Status Bits).

- **Write**
  Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{CSF}$ is Low and Write Enable $\overline{WRF}$ is Low with Output Enable $\overline{RDF}$ High. Addresses are latched on the falling edge of $\overline{WRF}$ or $\overline{CSF}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{WRF}$ or $\overline{CSF}$ whichever occurs first.

- **Output Disable**
  The data outputs are high impedance when the Output Enable $\overline{RDF}$ is High with Write Enable $\overline{WRF}$ High.

- **Standby**
  The memory is in standby when Chip Enable $\overline{CSF}$ is High and Program/Erase Controller P/E.C. is Idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{RDF}$ or Write Enable $\overline{WRF}$ inputs.

- **Automatic Standby**
  After 150 ns of inactivity and when CMOS levels are driving the addresses, the chip automatically enters a pseudo standby mode where power consumption is reduced to the CMOS standby value, while outputs are still driving the bus.

Appendix A – Flash Memory (cont.)

Figure 1. Memory Map and Sector Address Table

A18	A17	A16		TOP ADDRESS	BOTTOM ADDRESS
1	1	1	64K Bytes Sector	7FFFFh	70000h
1	1	0	64K Bytes Sector	6FFFFh	60000h
1	0	1	64K Bytes Sector	5FFFFh	50000h
1	0	0	–	4FFFFh	40000h
0	1	1	–	3FFFFh	30000h
0	1	0	–	2FFFFh	20000h
0	0	1	64K Bytes Sector	1FFFFh	10000h
0	0	0	64K Bytes Sector	0FFFFh	00000h

Instructions and Commands

The Command Interface (C.I.) latches commands written to the memory. Instructions are made up from one or more commands to perform Reset, Read Electronic Signature, Sector Erase, Bulk Erase, Program, Sector Erase Suspend and Erase Resume. Commands are made of address and data sequences. Addresses are latched on the falling edge of WRF or CSF and data is latched on the rising of WRF or CSF. The instructions require from 1 to 6 cycles, the first or first three of which are always write operations used to initiate the command. They are followed by either further write cycles to confirm the first command or execute the command immediately. Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to assure maximum data security. Commands are initialized by two preceding coded cycles which unlock the Command Interface. In addition, for Erase, command confirmation is again preceded by the two coded cycles.

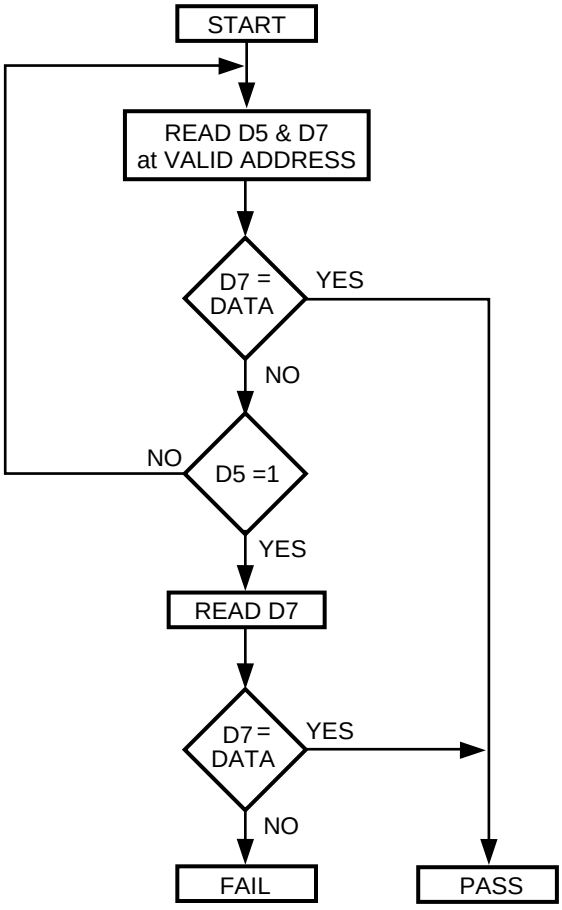
P/E.C. status is indicated during command execution by Data Polling on D7, detection of Toggle on D6, or Error on D5 and Erase Timer D3 bits. Any read attempt during Program or Erase command execution will automatically output those four bits. The P/E.C. automatically sets bits D3, D5, D6 and D7. Other bits (D0, D1, D2 and D4) are reserved for future use and should be masked.

- **Data Polling Bit DQ7**

  When Programming operations are in progress, this bit outputs the complement of the bit being programmed on D7. During Erase operation, it outputs a '0'. After completion of the operation, D7 will output the bit last programmed or a '1' after erasing. Data Polling is valid only effective during P/E.C. operation, that is after the fourth WRF pulse for programming or after the sixth WRF pulse for Erase. It must be performed at the address being programmed or at an address within the sector being erased. If the byte to be programmed belongs to a protected sector the command is ignored. If all the sectors selected for erasure are protected, D7 will set to '0' for about 100 µs, and then return to previous addressed memory data. See Figure 2 for the Data Polling flowchart.

Appendix A – Flash Memory (cont.)

Figure 2. Data Polling Flowchart



Instructions and Commands (cont.)

❑ **Toggle Bit D6**

When Programming operations are in progress, successive attempts to read D6 will output complementary data. D6 will toggle following toggling of either RDF or CSF when RDF is low. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit is valid only effective during P/E.C. operations, that is after the fourth WRF pulse for programming or after the sixth WRF pulse for Erase. If the byte to be programmed belongs to a protected sector the command will be ignored. If the sectors selected for erasure are protected, D6 will toggle for about 100 µs and then return back to Read. See Figure 3 for Toggle Bit flowchart and Figure 4 for Toggle Bit waveforms.

Appendix A – Flash Memory (cont.)

Figure 3. Data Toggle Flowchart

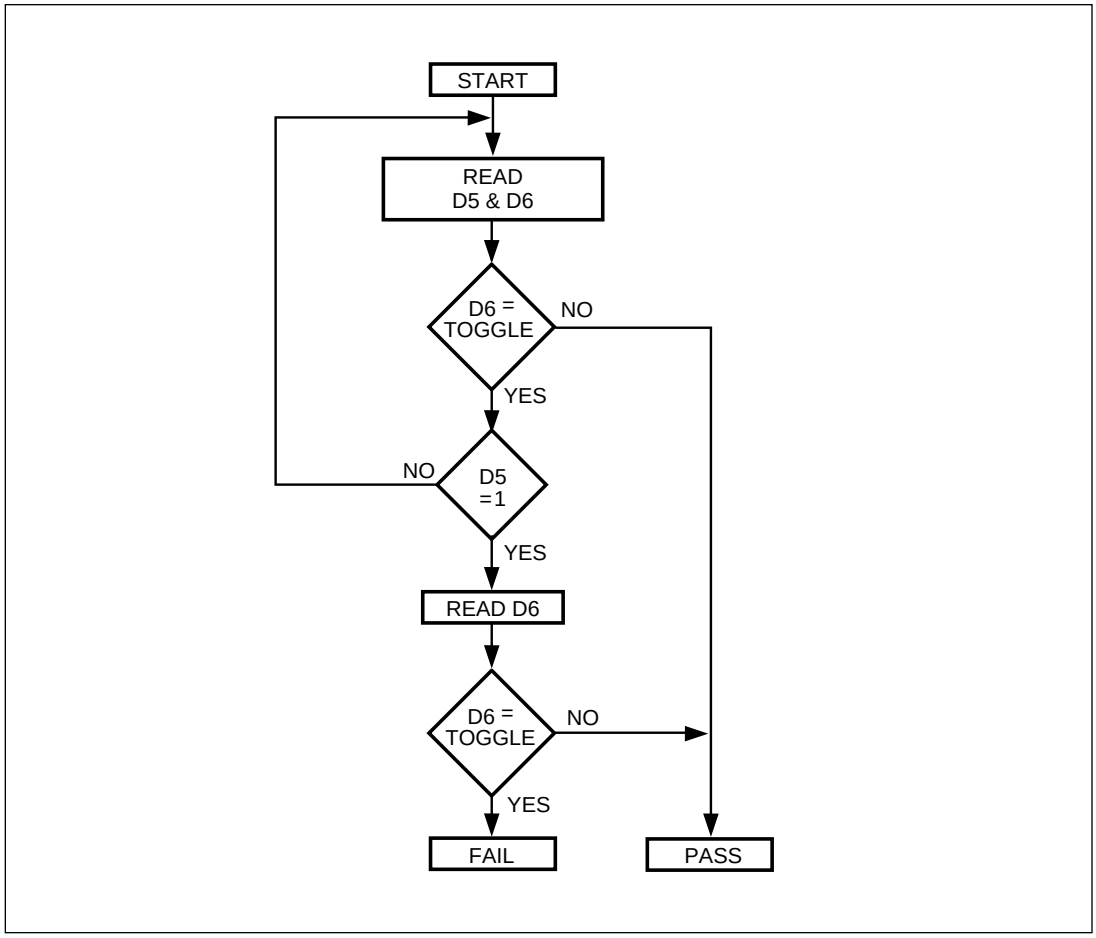
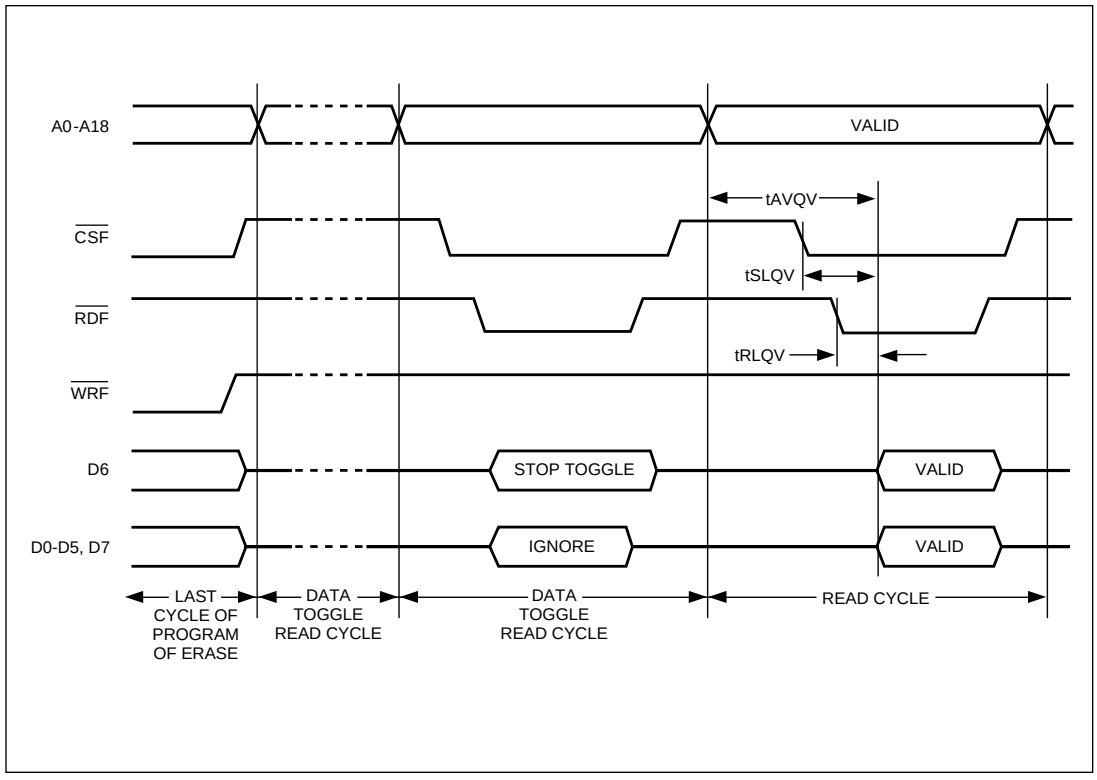


Figure 4. Data Toggle D6 AC Waveforms



Appendix A – Flash Memory (cont.)

Device Operation (cont.)

Instructions and Commands (cont.)

❑ **Error Bit D5**

This bit is set to '1' by the P/E.C. when there is a failure of byte programming, sector erase, or bulk erase that results in invalid data being programmed in the memory sector. In case of error in sector erase or byte program, the sector in which the error occurred or to which the programmed byte belongs, must be discarded. Other sectors may still be used. Error bit resets after Reset (RST) instruction. In case of success, the error bit will set to '0' during Program or Erase and to valid data after write operation is completed.

❑ **Erase Time Bit D3**

This bit is set to '0' by the P/E.C. when the last sector Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the wait period is finished, after 80 to 120 µs, D3 returns back to '1'.

❑ **Coded Cycles**

The two coded cycles unlock the Command Interface. They are followed by a command input or a command confirmation. The coded cycles consist of writing the data 0AAh at address 5555h during the first cycle and data 55h at address 2AAAh during the second cycle. Addresses are latched on the falling edge of $\overline{WRF}$ or $\overline{CSF}$ while data is latched on the rising edge of $\overline{WRF}$ or $\overline{CSF}$. The coded cycles happen on first and second cycles of the command write or on the fourth and fifth cycles.

❑ **Reset (RST) Instruction**

The Reset instruction consists of one write operation giving the command 0F0h. It can be optionally preceded by the two coded cycles. After wait state of 5 µs, subsequent read operations will read the memory array addressed and output the read byte.

❑ **Read Electronic Signature (RSIG) Instruction**

This instruction uses the two coded cycles followed by one write cycle giving the command 90h to address 5555h for command setup. A subsequent read will output the manufacturer code or the device code depending on the levels of A0, A1, A6, A16, A17 and A18. The manufacturer code, 20h, is output when the addresses lines A0, A1 and A6 are Low, the device code, 0E2h is output when A0 is High with A1 and A6 Low. See Table 2.

❑ **Bulk Erase (BE) Instruction**

This instruction uses six write cycles. The Erase Set-up command 80h is written to address 5555h on third cycle after the two coded cycles. The Bulk Erase Confirm command 10h is written at address 5555h on sixth cycle after another two coded cycles. If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing to 0FFh. Read operations after the sixth rising edge of $\overline{WRF}$ or $\overline{CSF}$ output the status register bits. During the execution of the erase by the P/E.C. the memory accepts only the Reset (RST) command. Read of Data Polling bit D7 return '0', then '1' on completion. The Toggle Bit D6 toggles during erase operation and stops when erase is completed. After completion the Status Register bit D5 returns a '1' if there has been an Erase Failure because the erasure has not been verified even after the maximum number of erase cycles have been executed.

Appendix A – Flash Memory (cont.)

Device Operation (cont.)

Instructions and Commands (cont.)

❑ ***Sector Erase (SE) Instruction***

This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written to address 5555h on third cycle after the two coded cycles. The Sector Erase Confirm command 30h is written on sixth cycle after another two coded cycles. During the input of the second command an address within the sector to be erased is given and latched into the memory. Additional Sector Erase confirm commands and sector addresses can be written subsequently to erase other sectors in parallel, without further coded cycles. The erase will start after an Erase timeout period of about 100 µs. Thus, additional Sector Erase commands must be given within this delay. The input of a new Sector Erase command will restart the timeout period. The status of the internal timer can be monitored through the level of D3, if D3 is '0' the Sector Erase Command has been given and the timeout is running, if D3 is '1', the timeout has expired and the P/E.C. is erasing the sector(s). Before and during Erase timeout, any command different from 30h will abort the instruction and reset the device to read array mode. It is not necessary to program the sector with 00h as the P/E.C. will do this automatically before to erasing to 0FFh. Read operations after the sixth rising edge of $\overline{WRF}$ or $\overline{CSF}$ output the status register status bits.

During the execution of the erase by the P/E.C., the memory accepts only the ES (Erase Suspend) and RST (Reset) instructions. Data Polling bit D7 returns a '0' while the erasure is in progress and a '1' when it has completed. The Toggle Bit D6 toggles during the erase operation. It stops when erase is completed. After completion the Status Register bit D5 returns '1' if there has been an Erase Failure because erasure has not completed even after the maximum number of erase cycles have been executed. In this case, it will be necessary to input a Reset (RST) to the command interface in order to reset the P/E.C.

❑ ***Program (PG) Instruction***

This instruction uses four write cycles. The Program command A0h is written on the third cycle after two coded cycles. A fourth write operation latches the Address on the falling edge of $\overline{WRF}$ or $\overline{CSF}$ and the Data to be written on its rising edge and starts the P/E.C. During the execution of the program by the P/E.C. by the P/E.C., the memory will not accept any instruction. Read operations output the status bits after the programming has started. Memory programming is made only by writing '0' in place of '1' in a Byte.

❑ ***Erase Suspend (ES) Instruction***

The Sector Erase operation may be suspended by this instruction which consists of writing the command 0B0h without any specific address code. No coded cycles are required. It allows reading of data from another sector while erase is in progress. Erase suspend is accepted only during the Sector Erase instruction execution and defaults to read array mode. Writing this command during Erase timeout will, in addition to suspending the erase, terminate the timeout. The Toggle Bit D6 stops toggling when the P/E.C. is suspended. Toggle Bit status must be monitored at an address out of the sector being erased.

The Toggle Bit will stop toggling between 0.1 µs and 15 µs after the Erase Suspend (ES) command has been written. The Flash Memory will then automatically set to Read Memory Array mode. When erase is suspended, Read from sectors being erased will output invalid data, Read from sector not being erased is valid. During the suspension the memory will respond only to Erase Resume (ER) and Reset (RST) instructions. The RST command will definitively abort erasure and result in invalid data in the sectors being erased.

Appendix A – Flash Memory (cont.)

Device Operation (cont.)

Instructions and Commands (cont.)

❑ ***Erase Resume (ER) Instruction***

If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any coded cycles.

❑ ***Programming***

The memory can be programmed byte-byte. The program sequence is started by the two coded cycles, followed by writing the Program command (0A0h) to the Command Interface. This is followed by writing the address and data byte to the memory. The Program/Erase Controller automatically starts and performs the programming after the fourth write operation. During programming the memory status is checked by reading the status bits D5, D6 and D7 which show the status of the P/E.C. D6 and D7 determine if programming is on going or has completed and D5 allows a check to be made for any possible error.

Power Up

The memory Command Interface is reset on power up to Read Array. Either $\overline{CSF}$ or $\overline{WRF}$ must be tied to V_{IH} during Power-up to allow maximum security and the possibility to write a command on the first rising edge of $\overline{CSF}$ or $\overline{WRF}$. Any write cycle initiation is blocked when V_{CC} is below V_{LKO}.

Supply Rails

Normal precautions must be taken for supply voltage decoupling. Each device in a system should have the V_{CC} rail decoupled with a 0.1 µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry V_{CC} program and erase currents as required.

Table 6. Program, Erase Times and Program, Erase Endurance Cycles

(T_A = 0 to 70°C; V_{CC} = 5 V ± 10% or 5 V ± 5%)

Parameter	Min	Typ	Max	Unit
Chip Program (Byte)		6		sec
Bulk Erase (Preprogrammed)		2.5	30	sec
Bulk Erase		8.5		sec
Sector Erase (Preprogrammed)		1	30	sec
Sector Erase		1.5		sec
Byte Program	10		1200	µs
Program/Erase Cycles (per Sector)	100,000			cycles

Product Revisions

Product Revisions	Revision Reason	Data Sheet Changes
Original PSD813FN/FH (10/97)	Initial release	–