STA002

STARMAN™ CHANNEL DECODER

FRONT_END INTERFACE:
- IF input carrier frequency: f = 1.84 MHz
- Single internal 6 bit A/D converter
- QPSK demodulation
- Input symbol frequency: Fs = 1.84 Msymbols/s
- Digital Nyquist root filter:
  - roll-off value of 0.4
- Digital carrier loop:
  - on-chip quadrature demodulator and tracking loop
  - lock detector
  - C/N indicator
- Digital timing recovery:
  - internal timing error evaluation, filter and correction
- Digital AGC:
  - internal signal power estimation and filter
 - output control signal for AGC (1 bit PWM)

FORWARD ERROR CORRECTION:
- Inner decoder:
  - Viterbi soft decoder for convolutional codes, constraint length M=7, Rate 1/2
- Deinterleaver block
- Outer decoder:
  - Reed-Solomon decoder for 32 parity bytes; correction of up to 16 byte errors
  - Block lengths: 255
  - Energy dispersal descrambler

BACK_END INTERFACE:
- Broadcast Channel selection
- Audio Service Component selection to MPEG decoder
- Service Component selection

CONTROL:
- I²C serial Bus control interface

TQFP44
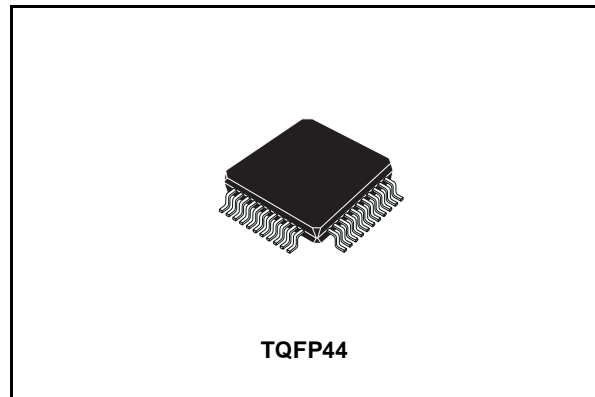
DECRYPTION:
- WES scheme supported

DESCRIPTION
Designed for World Space satellites digital audio receivers, the STA002 Digital Receiver Front-end integrates all the blocks needed to demodulate incoming digital satellite audio signals from the tuner: analog to digital converter, QPSK demodulator, signal power estimator, automatic gain control, Viterbi decoder, deinterleaver, Reed-Solomon decoder and energy dispersal descrabler. Its advanced error correction functions guarantees a low error rate even with small low gain receiver antennas.

Additional functions include the selection of broadcast channel, service components and audio components for source decoding:

- The MPEG Audio bitstream is provided at the serial audio output port.
- The Broadcast Channel is provided to the serial data output port.
- The Service Component is provided at the SC output interface.

World Space encryption scheme is supported for pay programs and paging.

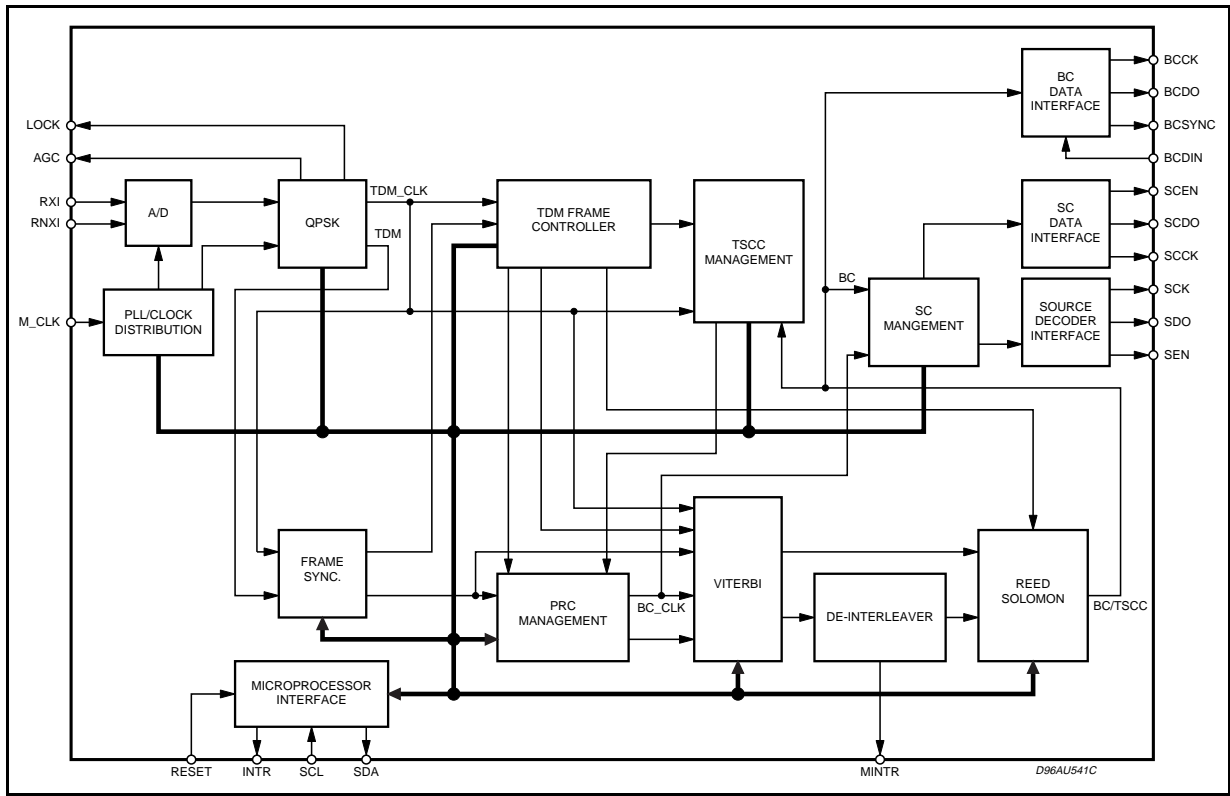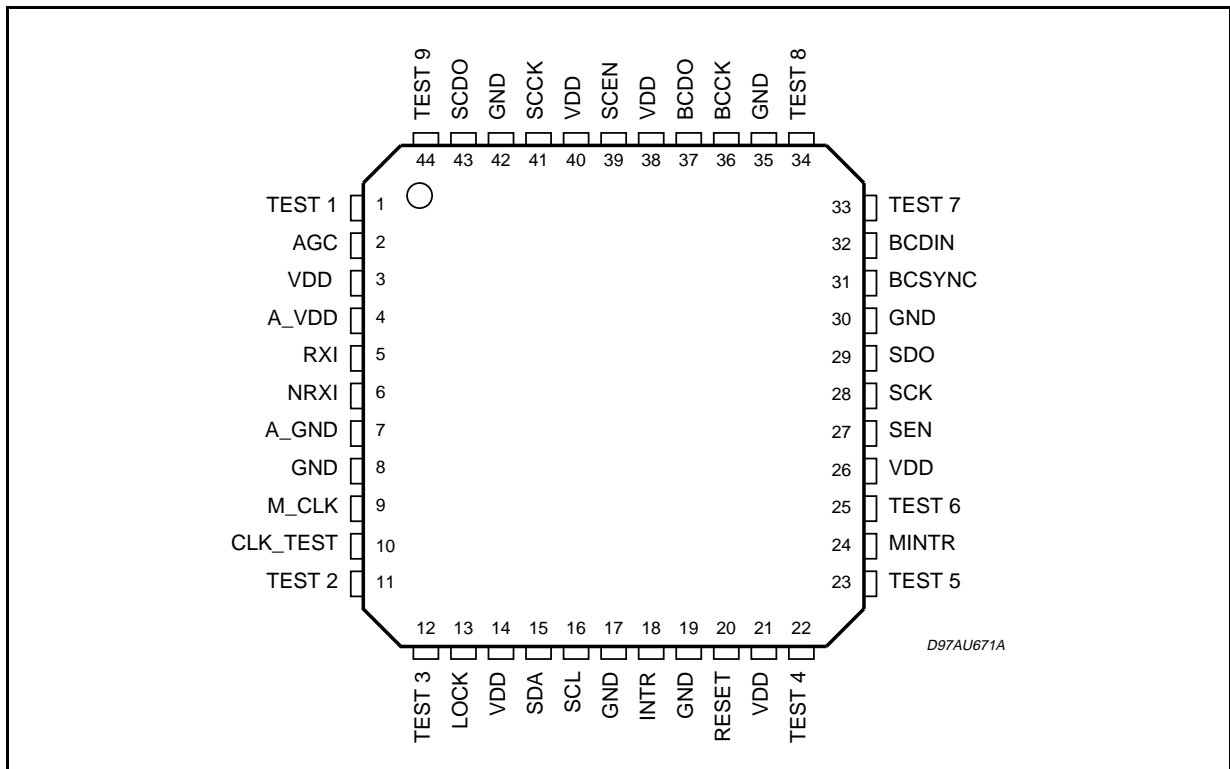**Fig. 1: Channel Decoder Block Diagram**

Fig. 2: Pin Connection

PIN DESCRIPTION

Type	Pin Name	Type	Function	PAD Description
1, 11, 12	TEST (1:3)	I	Test Pin	CMOS Input Pad Buffer with Pull-Down
22	23, 25, 33, 34, 44	TEST (4:9) I		Test Pin
2	AGC	O	AGC Output	CMOS 2mA Output Driver
3, 14, 21, 26, 38, 40	VDD		Positive Supply Voltage	
4	A_VDD		Analog Positive Supply Voltage	
5	RXI	I	IF Signal Input	Analog Pad Buffer
6	NRXI	I	IF Signal Input	Analog Pad Buffer
7	A_GND		Analog Ground	
9	M_CLK	I	Master Clock	Analog Pad Buffer with Comparator
10	CLK_TEST		Not Connected	CMOS Input Pad Buffer
13	LOCK	O	Carrrier Lock Indicator	CMOS 2mA Output Driver
15	SDA	I/O	Data + ACK	CMOS Schmitt Trigger Bdir Pad Bufer
16	SCL	I	Serial Clock	CMOS Input Pad Schmitt Triggered
8, 17, 19, 30, 35, 42	GND		Negative Supply Voltage	
18	INTR	O	Interrupt	CMOS 2mA Output Driver
20	RESET	I	Master Reset	CMOS Input Pad Buffer with Pull-Up
24	MINTR	O	MPEG Interrupt	CMOS 2mA Output Driver
27	SEN	O	MPEG Enable	CMOS 2mA Output Driver
28	SCK	O	MPEG Clock	CMOS 2mA Output Driver
29	SDO	O	MPEG Bit Output	CMOS 2mA Output Driver
31	BCSYNC	O	Broadcast Channel Sync	CMOS 2mA Output Driver
32	BCDIN	I	Broadcast Channel Data Input	CMOS Input Pad Buffer
36	BCCK	O	Broadcast Channel Clock	CMOS 2mA Output Driver
37	BCDO	O	Broadcast Channel Data Output	CMOS 2mA Output Driver
39	SCEN	O	Service Component Enable	CMOS 2mA Output Driver
41	SCCK	O	Service Component Clock	CMOS 2mA Output Driver
43	SCDO	O	Service Component Data Output	CMOS 2mA Output Driver

Note: pin 1, 11, 12 and 22 must be connected to ground in functional mode.

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-amb}$	Thermal resistance Junction to Ambient	85	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply	-0.3 to 4	V
V_i	Voltage on Input pins	-0.3 to V_{DD} +0.3	V
V_O	Voltage on output pins	-0.3 to V_{DD} +0.3	V
T_{stg}	Storage Temperature	-40 to +150	°C
T_{oper}	Operative ambient temp	-20 to +85	°C

ELECTRICAL CHARACTERISTICS: V_{DD} = 3.3V $\pm$0.3V; T_{amb} = 0 to 70°C; Rg = 50Ω unless otherwise specified

DC OPERATING CONDITIONS

Symbol	Parameter	Value
V_{DD}	Power Supply Voltage	2.7 to 3.6V
T_j	Operating Junction Temperature	-20 to 125°C

GENERAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{IL}	Low Level Input Current Without pull-up device	V_i = 0V	-10		10	μA	1
I_{IH}	High Level Input Current Without pull-up device	V_i = V_{DD}	-10		10	μA	1
V_{esd}	Electrostatic Protection	Leakage < 1μA	2000			V	2

Note 1: The leakage currents are generally very small, < 1nA. The value given here is a maximum that can occur after an electrostatic stress on the pin.
Note 2: Human Body Model.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
V_{IL}	Low Level Input Voltage				0.2*V_{DD}	V	
V_{IH}	High Level Input Voltage		0.8*V_{DD}			V	
V_{ol}	Low Level Output Voltage	I_{ol} = Xma			0.4V	V	1, 2
V_{oh}	High Level Output Voltage		0.85*V_{DD}			V	1, 2

Note 1: Takes into account 200mV voltage drop in both supply lines.
Note 2: X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

PULL_UP & PULL_DOWN CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
I_{pu}	Pull-up current	V_i = 0V	-25	-66	-125	μA	1
I_{pu}	Pull-up current	V_i = V_{DD}	25	66	125	μA	1
R_{pu}	Equivalent Pull-up Resistance	V_i = 0V		50		kΩ	
R_{pu}	Equivalent Pull-down Resistance	V_i = V_{DD}		50		kΩ	

Note 1: Min. condition: V_{DD} = 2.7V, 125°C Min process
Max. condition: V_{DD} = 3.6V, -20°C Max.

M_ CLK Electrical Characteristics (Pin number 9)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{il}	Low Level Input Voltage			V_{DD} -1.7	V
V_{ih}	High Level Input Voltage	V_{DD} -0.9			V
V_{ref}	Input Reference Voltage		V_{DD} -1.3		V

POWER DISSIPATION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Note
PD	Power Dissipation @ V_{DD} = 3V	M_CLK = 39,0269MHz			80	mW	

Fig. 3: Test Circuit
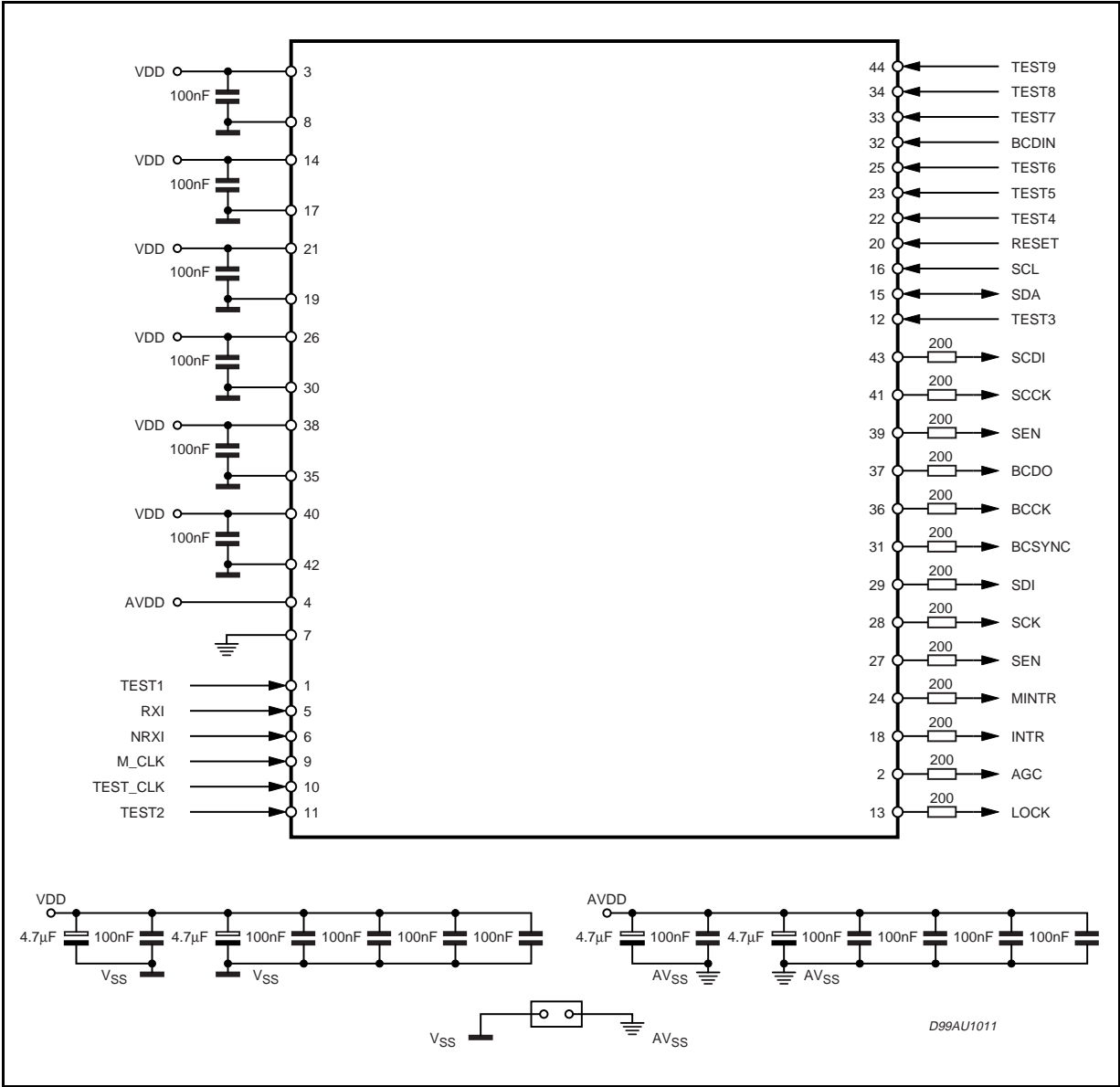
Figure 4. Test Load Circuit
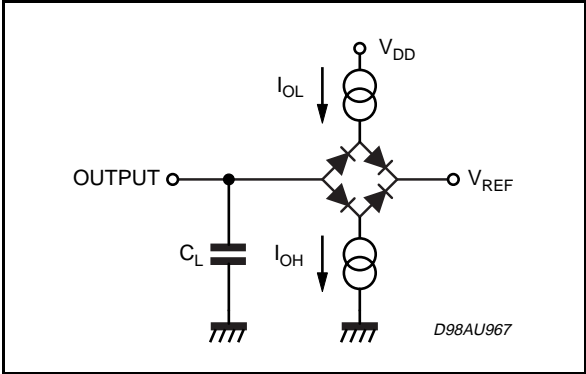
Test Load

Output	I_{OL}	I_{OH}	C_L	V_{REF}
SDA	5mA		100pF	3.6V
Other Outputs	100μA	100μA	100pF	1.5V

FUNCTIONAL DESCRIPTION

The STA002 integrates all the functions needed to demodulate the signal coming from the RF FE; with reference to the block diagram (Fig 1), STA002 includes the following functions:

Microprocessor interface

Data transmission from microcontroller to the device takes place through the 2 wires (SDA and SCL) I2C bus interface. STA002 acts always as a slave in all its communications.

Interface to the Front-end

This block receives from the RF front-end the QPSK modulated signal, centered at 1.84 MHz (2nd IF frequency). This signal is over sampled using the Master Clock and converted to digital on 6 bits in 2's complement format. The same frequency is also used to provide the clock signal for the QPSK demodulator block.

QPSK

This block is composed by:

- AGC1
- quadrature demodulator
- carrier recovery
- timing recovery
- frequency sweep generator
- AGC2
- lock indicator
- carrier to noise estimator

To assure flexibility and to cover different working conditions most of the parameters of each function can be programmed through the I2C interface.

TDM Demultiplexer

The TDM frame is divided into 3 fields.

The first is the Master Frame Preamble (MFP) which contains the synchronisation word. The second, the Time Slot Control Channel (TSCC), contains information about the organization of the Prime Rate Channel data which follows. The third, is the data field; it contains 96 Prime Rate Channels of 16 Kbit/s each; up to 8 Prime Rate Channels are grouped into one Broadcast Channel.

The TDM demultiplexer executes the extraction and decoding of one Broadcast Channel from the TDM stream, according to the instructions coming from the microcontroller. The decoding flow is the following:

- TDM synchronization

The master frame synchronization block receives the demodulated symbol stream from the QPSK demodulator and performs the alignment detecting the Master Frame Preamble.

The known syncronization word is also used to correct the phase ambiguity intrinsic in QPSK demodulation.

- TSCC extraction

The information of the Prime Rate Channels to Broadcast Channels allocation are contained in the TSCC field which is synchronised with the MFP.

In this stage all the information related to the TSCC are extracted and made available for the microcontroller via the I2C interface.

- PRC extraction and BC recovery

This block, after the Broadcast Channel (BC) selection, performs the extraction and synchronisation of the Prime Rate Channels (PRC) belonging to the selected BC.

The extracted PRCs are aligned and grouped into one BC data stream.

- FEC decoder

The extracted BC is decoded using a concatenated Forward Error Correction approach.

The FEC circuitry utilizes three error correction stages: a rate 1/2 Viterbi decoder, a 255x4 bytes convolutional deinterleaver and a 255/223 Reed Solomon decoder.

The RS input blocks are 255 bytes long with 32 parity bytes.

Up to 16 errored bytes can be fixed in each RS block.

BC demultiplexer

Every BC contains up to 8 Service Components; the Service Control Header (SCH) field contains all the information related to the organization of the Service Components. This stage provides the extraction of the SCH from the BC.

The SCH is available through I2C bus to the microcontroller for the selection of the desired Audio Service Component, which is then supplied directly to the MPEG Source decoder via the audio Service Component Interface.

DEVICE OPERATION

1. I²C BUS SPECIFICATION

The STA002 supports the I2C protocol. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the others as the slave. The master will always initiate the transfer and will provide the serial clock

for synchronisation. The STA002 is always a slave device in all its communications.

1. 1 COMMUNICATION PROTOCOL

1.1.0 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transitions while the clock is high are used to identify START or STOP condition.

1.1.1 Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

1.1.2 Stop condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communications between STA002 and the bus master.

1.1.3 Acknowledge bit

An acknowledge bit is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data.

During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of 8 bits of data.

Some registers do not give acknowledge when the data is not available.

1.1.4 Data input

During the data input the STA002 samples the SDA signal on the rising edge of the clock SCL. For correct device operation the SDA signal has to be stable during the rising edge of the clock and the data can change only when the SCL line is low.

1.2 DEVICE ADDRESSING

To start communication between the master and the STA002, the master must initiate with a start condition. Following this the master sends onto the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifier, corresponding to the I2C bus definition. For the STA002 these are fixed as 1101010.

The 8th bit (LSB) is the read or write operation bit

(RW; set to 1 in read mode and to 0 in write mode). After a START condition the STA002 identifies on the bus the device address and if matching it will acknowledges the identification on SDA bus during the 9th bit time.

The following 2 bytes after the device identification byte are the internal space address.

1.3 WRITE OPERATION (see fig. 5)

Following a START condition the master sends a device select code with the RW bit set to 0.

The STA002 gives the acknowledge and waits for the 2 bytes of internal address. The least significant 10 bits of the 2 bytes address provides access to any of the internal registers. The most significant bit means incremental mode (1 = autoincremental, 0 = no) and the other bits are set to zero.

After the reception of each of the internal bytes address the STA002 again responds with an acknowledge.

1.3.1 Byte write

In the byte write mode the master sends one data byte and this is acknowledged by STA002. The master then terminates the transfer by generating a STOP condition.

1.3.2 Multibyte write

The multibyte write mode can start from any internal address. The master sends the data and each one is acknowledged by the STA002. The transfer is terminated by the master generating a STOP condition.

1.4 READ OPERATION (see Fig. 6)

1.4.1 Current byte address read

The STA002 has an internal byte address counter. Each time a byte is written or read, this counter, according to the autoincremental bit setting, is incremented or not.

For the current byte address read mode, following a START condition the master sends the device address with the RW bit set to 1. The STA002 acknowledges this and outputs the byte addressed by the internal byte address counter.

The counter is then incremented or not depending on the autoincremental bit. The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

1.4.2 Random byte address read

A dummy write is performed to load the byte address into the internal address register.
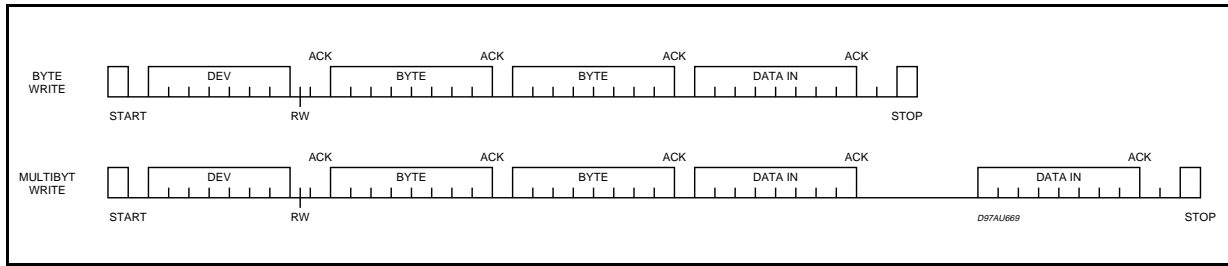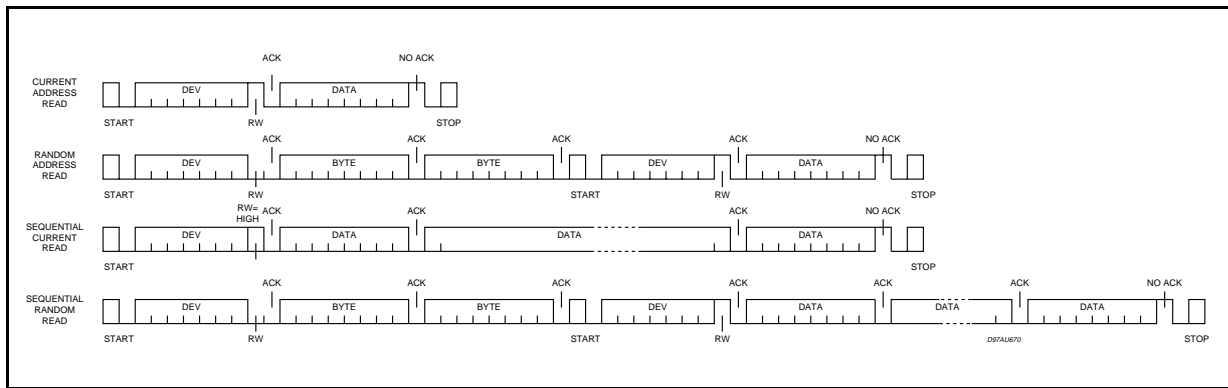
Fig. 5: Write Mode Sequence

Fig. 6: Read Mode Sequence

This is followed by another START condition from the master and the device address repeated with the RW bit set to 1. The STA002 acknowledges this and outputs the byte addressed by the internal byte address counter.

The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

1.4.3 Sequential address read

This mode can be initiated with either a current address read or a random address read. However in this case the master does acknowledge the data byte output and the STA002 continues to output the next byte in sequence.

To terminate the stream of bytes the master does not acknowledge the last received byte, but terminates the transfer with a STOP condition.

The output data stream is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output.

1.5 REGISTER MAP (8 BIT REGISTER)

1.5.1 Register address List (by function)

FUNCTION	START ADDRESS		END ADDRESS	
	HEX_COD	BIN	HEX_COD	BIN
SCH	000H	0000000000	03FH	0000111111
RFU	040H	0000111111	07FH	0001111111
QPSK	080H	0010000000	09FH	0010011111
RFU	0A0H	0010100000	0FFH	0011111111
SCH_MEM	100H	0100000000	1EBH	0111101011
RFU	1ECH	0111101100	1FFH	0111111111
TDM_MULTIPLEX	200H	1000000000	23FH	1000111111
RFU	240H	1001000000	2FFH	1011111111
TSCC_MEM	300H	1100000000	3C1H	1111000001
RFU	3C2H	1111000010	3FFH	1111111111

1.5.2 SCH Registers

HEX_COD	DEC_COD	REGISTER NAME	TYPE	RESET VALUE
000H	0	BRI_REG & NSC_REG (note 1)	R	
001H	1	EC_REG (note 1)	R	
002H	2	AFCI 1_REG (note 1)	R	
003H	3	AFCI 2_REG (note 1)	R	
004H	4	SOF_SF_REG (note 1)	R	
005H	5	ADF1_REG (7:0) (note 1)	R	
006H	6	ADF1_REG (15:8) (note 1)	R	
007H	7	ADF2_REG (7:0) (note 1)	R	
008H	8	ADF2_REG (15:8) (note 1)	R	
009H	9	ADF2_REG (23:16) (note 1)	R	
00AH	10	ADF2_REG (31:24) (note 1)	R	
00BH	11	ADF2_REG (39:32) (note 1)	R	
00CH	12	ADF2_REG (47:40) (note 1)	R	
00DH	13	ADF2_REG (55:48) (note 1)	R	
00EH	14	ADF2_REG (63:56) (note 1)	R	
00FH	15	SEL_SC_REG	R/W	98H
010H	16	IW_REG (7:0) (note 2)	W	41H
011H	17	IW_REG (15:8) (note 2)	W	42H
012H	18	IW_REG (23:16) (note 2)	W	43H
013H	19	IW_REG (31:24) (note 2)	W	44H
014H	20	IW_REG(39:32) (note 2)	W	45H
015H	21	IW_REG (47:40) (note 2)	W	46H
016H	22	IW_REG (55:48) (note 2)	W	47H
017H	23	IW_REG (63:56) (note 2)	W	48H
018H	24	EM_REG	R/W	00H
019H	25	PIWE_REG (7:0) (note 2)	R/W	00H
01AH	26	PIWE_REG (15:8) (note 2)	R/W	00H
01BH	27	BCIN_DELAY_REG	R/W	00H
01CH	28	BC_ALARM_REG	R/W	20H
01DH	29	TEST_PURPOSE	R/W	
01EH	30	RFU		
01FH	31	RFU		
020H	32	TEST PURPOSE	R/W	
021H	33	TEST PURPOSE	R/W	
022H	34	TEST PURPOSE	R/W	
023H	35	TEST PURPOSE	R/W	
024H	36	TEST PURPOSE	R/W	
025H	37	TEST PURPOSE	R/W	
026H	38	TEST PURPOSE	R/W	
027H	39	TEST PURPOSE	R/W	
028H	40	TEST PURPOSE	R/W	
029H	41	TEST PURPOSE	R/W	

Note 1: no acknowledge when data is not available
Note 2: when updated all bytes must be written

1.5.2 SCH Registers

HEX_COD	DEC_COD	REGISTER NAME	TYPE	RESET VALUE
02AH	42	TEST PURPOSE	R/W	
02BH	43	TEST PURPOSE	R/W	
02CH	44	TEST PURPOSE	R/W	
02DH	45	TEST PURPOSE	R/W	
02EH	46	TEST PURPOSE	R/W	
02FH	47	TEST PURPOSE	R/W	
030H	48	TEST PURPOSE	R/W	
031H	49	TEST PURPOSE	R/W	
032H	50	TEST PURPOSE	R/W	
033H	51	TEST PURPOSE	R/W	
034H	52	TEST PURPOSE	R/W	
035H	53	TEST PURPOSE	R/W	
036H	54	TEST PURPOSE	R/W	
037H	55	TEST PURPOSE	R/W	
038H	56	PIW_RAM (7:0) (note1)	W	00H
039H	57	PIW_RAM (15:8) (note1)	W	00H
03AH	58	PIW_RAM (23:16) (note1)	W	00H
03BH	59	PIW_RAM (31:24) (note1)	W	00H
03CH	60	PIW_RAM (39:32) (note1)	W	00H
03DH	61	PIW_RAM (47:40) (note1)	W	00H
03EH	62	PIW_RAM (55:48) (note1)	W	00H
03FH	63	PIW_RAM (63:56) (note1)	W	00H

Note 1: when updated all bytes must be written

1.5.3 QPSK Registers

HEX_COD	DEC_COD	REGISTER NAME	TYPE	RESET VALUE
080H	128	QPSK_CONTROL1	R/W	10H
081H	129	QPSK_CONTROL2	R/W	90H
082H	130	AGC1 _REF1 (note 1)	R/W	06H
083H	131	AGC1 _REF2 (note 1)	R/W	01H
084H	132	AGC1_BETA	R/W	00H
085H	133	AGC1_INTG	R/W	7FH
086H	134	AGC2 _REF	R/W	16H
087H	135	AGC2 _BETA	R/W	00H
088H	136	AGC2_INTG	R/W	23H
089H	137	CN_CNT	R/W	FFH
08AH	138	SYMFREQ1 (note 1)	R/W	D3H
08BH	139	SYMFREQ2 (note 1)	R/W	11H
08CH	140	SYMFREQ3 (note 1)	R/W	0CH
08DH	141	TIMFLTPAR	R/W	48H
08EH	142	TIMINTG	R/W	00H
08FH	143	CARFLTPAR	R/W	57H
090H	144	IFFREQ1 (note 1)	R/W	37H
091H	145	IFFREQ2 (note 1)	R/W	1DH
092H	146	IFFREQ3 (note 1)	R/W	C1H
093H	147	IFFREQ4 (note 1)	R/W	00H
094H	148	CARINTG	R/W	00H
095H	149	RAMPCTRL	R/W	01H
096H	150	CARFREQ1	R	
097H	151	CARFREQ2	R	
098H	152	CARFREQ3	R	
099H	153	FLAG	R	
09AH	154	RFU		
09BH	155	RFU		
09CH	156	RFU		
09DH	157	RFU		
09EH	158	RFU		
09FH	159	RFU		

Note 1: when updated all bytes must be written

1.5.4 SCH_MEM Registers

HEX_COD	DEC_COD	REGISTER NAME	TYPE	RESET VALUE
100H	256	SC1_LENGHT & SC1_TYPE	R	
101H	257	SC1_EC & SC1_PT	R	
102H	258	SC1_PT	R	
103H	259	LANGUAGE 1	R	
104H	260	SC2_LENGHT & SC2_TYPE	R	
105H	261	SC2_EC & SC2_PT	R	
106H	262	SC2_PT	R	
107H	263	LANGUAGE 2	R	
108H	264	SC3_LENGHT & SC3_TYPE	R	
109H	265	SC3_EC & SC3_PT	R	
10AH	266	SC3_PT	R	
10BH	267	LANGUAGE 3	R	
10CH	268	SC4_LENGHT & SC4_TYPE	R	
10DH	269	SC4_EC & SC4_PT	R	
10EH	270	SC4_PT	R	
10FH	271	LANGUAGE 4	R	
110H	272	SC5_LENGHT & SC5_TYPE	R	
111H	273	SC5_EC & SC5_PT	R	
112H	274	SC5_PT	R	
113H	275	LANGUAGE 5	R	
114H	276	SC6_LENGHT & SC6_TYPE	R	
115H	277	SC6_EC & SC6_PT	R	
116H	278	SC6_PT	R	
117H	279	LANGUAGE 6	R	
118H	280	SC7_LENGHT & SC7_TYPE	R	
119H	281	SC7_EC & SC7_PT	R	
11AH	282	SC7_PT	R	
11BH	283	LANGUAGE 7	R	
11CH	284	SC8_LENGHT & SC8_TYPE	R	
11DH	285	SC8_EC & SC8_PT	R	
11EH	286	SC8_PT	R	
11FH	287	LANGUAGE8	R	
120H	288	DYNAMIC LABEL	R	
121H	289	DYNAMIC LABEL	R	
122H	290	DYNAMIC LABEL	R	
123H	291	DYNAMIC LABEL	R	
124H	292	DYNAMIC LABEL	R	
1E7H	487	DYNAMIC LABEL	R	
1E8H	488	DYNAMIC LABEL	R	
1E9H	489	DYNAMIC LABEL	R	
1EAH	490	DYNAMIC LABEL	R	
1EBH	491	DYNAMIC LABEL	R	

Note: no acknowledge when data is not available for all the SCH_MEM registers

1.5.5 TDM_MULTIPLEX Registers

HEX_COD	DEC_COD	REGISTER NAME	TYPE	RESET VALUE
200H	512	TDM_TRSH 1	R/W	4BH
201H	513	TDM_TRSH 2	R/W	43H
202H	514	PRC_TRSH 1	R/W	2AH
203H	515	PRC_TRSH 2	R/W	23H
204H	516	VITERBI_ERROR_CONTROL	R/W	00H
205H	517	SP_TRSH 2	R/W	13H
206H	518	PRC_MAXDELAY	R/W	06H
207H	519	TDM_ALARM	R/W	00H
208H	520	PRC_ALARM	R/W	00H
209H	521	BC_SEL 1 (note)	R/W	01H
20AH	522	BC_SEL2 (note)	R/W	00H
20BH	523	CONTROL	R/W	00H
20CH	524	INT_MASK	R/W	00H
20DH	525	ERROR_ REG	R/W	00H
20EH	526	STATUS REG	R	
20FH	527	PRC_ACTIVE_REG	R	
210H	528	PRC_ LOCK_REG	R	
211H	529	PRC_DELAY_REG	R	
212H	530	RS_ERROR_CONTROL	R/W	00H
213H	531	VIT_ERROR1	R/W	
214H	532	VIT_ERROR2	R/W	
215H	533	RS_BYTE_ERROR1	R/W	
216H	534	RS_BYTE_ERROR2	R/W	
217H	535	RS_BLOCK_ERROR	R/W	
218H	536	TEST_PURPOSE	R/W	
219H	537	TEST_PURPOSE	R/W	
21AH	538	TEST_PURPOSE	R/W	
21BH	539	TEST_PURPOSE	R/W	
21CH	540	TEST_PURPOSE	R/W	
21DH	541	TEST_PURPOSE	R/W	
21EH	542	PLL_INT_REG	R/W	00H
21FH	543	TEST_PURPOSE	R/W	
220H	544	RESERVED	R/W	07H
221H	545	RESERVED	R/W	1CH
222H	546	RESERVED	R/W	4AH
223H	547	RESERVED	R/W	03H
224H	548	RESERVED	R/W	18H
225H	548	RESERVED	R/W	25H
226H	550	RESERVED	R/W	2EH
227H	551	RESERVED	R/W	3EH
228H	552	RESERVED	R/W	18H
229H	553	RESERVED	R/W	0DH
22AH	554	RESERVED	R/W	18H
22BH	555	RESERVED	R/W	12H
22CH	556	RESERVED	R/W	0AH
22DH	557	RESERVED	R/W	0CH

Note: when updated all bytes must be written

1.5.5 TDM_MULTIPLEX Registers (continued)

HEX_COD	DEC_COD	REGISTER NAME	TYPE	RESET VALUE
22EH	558	RESERVED	R	0EH
22FH	559	RESERVED	R	12H
230H	560	RESERVED	R	32H
231H	561	RESERVED	R	0CH
232H	562	RESERVED	R	1CH
233H	563	RESERVED	R	2FH
234H	564	RESERVED	R	0AH
235H	565	RESERVED	R	0BH
236H	566	RESERVED	R	2AH
237H	567	RESERVED	R	09H
23CH	568	TEST_PURPOSE	R	09H
23DH	569	TEST_PURPOSE	R	09H
237EH	570	TEST_PURPOSE	R	09H

1.5.6 TSCC_MEM Registers

HEX_COD	DEC_COD	REGISTER NAME	TYPE	RESET VALUE
300H	768	TSCW 1 (7:0)	R	
301H	769	TSCW 1 (15:8)	R	
302H	770	TSCW 2 (7:0)	R	
303H	771	TSCW 2 (15:8)	R	
304H	772	TSCW 3 (7:0)	R	
305H	773	TSCW 3 (15:8)	R	
306H	774	TSCW 4 (7:0)	R	
307H	775	TSCW 4 (15:8)	R	
3BCH	956	TSCW 95 (7:0)	R	
3BDH	957	TSCW 95 (15:8)	R	
3BEH	958	TSCW 96 (7:0)	R	
3BFH	959	TSCW 96 (15:8)	R	
3C0H	960	TSCW ID (7:0)	R	
3C1H	961	TSCW ID (15:8)	R	

2. IF INTERFACE

The Master Clock (M_CLK) is the source of all the STA002 internal timings.

M_CLK is internally divided to drive the A/D converter and to provide the clock signal for the QPSK block.

The IF input signal, centered at 1.84MHz, is oversampled at a frequency F_{ck} of M_CLK/4 or M_CLK/2 according to STA002 presettings.

2.1 PLL

This fully integrated PLL includes the phase/frequency detector, the charge pump, the filter and the VCO.

The PLL output frequency F_{ck} can be selected via I²C interface according to the PLL_INT_REG.

Reg. name: PLL_INT_REG

Internal address: 21E H

Reset Value : 00H

Type: R/W

MSB							LSB
X	X	b5	b4	b3	b2	b1	b0

Description: PLL and INTR pin control register

b1	b0	PLL output clock (ADC input)
0	0	M_CLK (pin 9)
0	1	2XM_CLK (pin9)
1	0	Test purpose
1	1	Test purpose

b5	b4	INTR pin control
0	0	Normal function (from ERROR_REG)
0	1	BC_LOCK signal on INTR pin
1	0	MFP_LOCK signal on INTR pin
1	1	PRCP_ALL_LOCK on INTR pin

b3, b2: Test purpose

2.2 A/D CONVERTER

This block performs the analog to digital conversion of the incoming IF input signal.

The ADC has a resolution of 6 bit and is based on the so called Half Flash architecture to reduce both area and power consumption.

The sampling rate depends on the M_CLK (Master Clock) frequency and on the PLL presetting.

3. QPSK DEMODULATOR

3.1 QUADRATURE DEMODULATOR

The final base-band demodulation is performed in this block.

The samples of the IF input signal are multiplied by the sine and cosine functions to get the two in-phase (I) and quadrature (Q) components of the QPSK signal. The phase ambiguity inherent in QPSK is solved in the frame synchronisation part.

A programmable bit allows to multiply by -1 the quadrature component in order to accomodate QPSK modulation with another convention of rotation sense (this is equivalent to a permutation of I and Q components).

The sine and cosine functions are generated by an NCO using a phase accumulator and a look-up table.

3.2. INTERPOLATOR NYQUIST FILTER

The I and Q components are filtered by a digital Nyquist root filter with the following features:

Separate I and Q stream, Fck/Fsym samples per symbols;

Raised root cosine shape with roll-off factor of 40%;

Separate I and Q output stream, 1 sample per symbol.

This filter performs both the Nyquist filter function (matched with the one in the transmission side) and the interpolation function to compute the optimum output sample.

3.3. TIMING RECOVERY

The timing loop is completely implemented digitally and comprises the timing detector working at symbol rate, a loop filter, the timing NCO and the Nyquist/interpolator filters.

The loop is controlled by two parameters, alpha_tmg and beta_tmg contained in the TIMFLTPAR register.

3.3.1 Timing loop registers

Timing loop filter parameter register (TIMFLTPAR)

Internal address: 8D H

Reset Value: 48H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
alpha_tmg				beta_tmg			

Timing frequency registers (TIMINTG)

Internal address: 8E H

Reset Value: 0AH

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
signed number							

The value of this register, when the system is locked, is an image of the frequency offset.

Timing NCO frequency setting (SYMFREQ)

Internal address: 8C H 8B H 8A H

Reset Value   : 0CH 11H D3H

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

SYMFREQ3

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

SYMFREQ2

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

SYMFREQ1

This register is divided into three bytes. The LSB byte is named SYMFREQ1, the MSB is named SYMFREQ3.

The 22 bits value to be written into this register is given by:

$$SYMFREQ = INT\left(\frac{F_{sym}}{F_{ck}} 2^{22}\right)$$

for example if

M_CLK = 39,02687179MHz, Fck = M_CLK/4

SYMFREQ = 790995 = (C11D3)HEX

which is the Reset Value.

3.3.2 Loop equations

This timing loop is a second order one. The natural frequency and the damping factor may be calculated by the following formulas:

$$f_n = \frac{\sqrt{K_o\,K_D\,\beta \cdot m}}{2\pi}$$

where β is programmed by the timing register beta_tmg:

$$b = 2^{beta\_tmg-14} \cdot F_{sym} \quad (F_{sym} = 1.84MHz)$$

where m is the reference value of the AGC2 loop (see AGC2_REF register), K_D is the timing detector gain and Ko is the constant of the timing NCO:

$$K_o = \frac{2\pi}{2^{22}} F_{ck}$$

The damping factor is:

$$\xi = \frac{\alpha}{2}\,\sqrt{\frac{K_o\,K_D \cdot m}{\beta}}$$

where α is programmed by the timing register alpha_tmg:

$$\alpha = 2^{alpha\_tmg}$$

beta_tmg can only take value from 0 to 15; if beta_tmg is 0 the loop reduces to a first order one.
Alpha_tmg can take any value from 0 to 7. If both alpha_tmg and beta_tmg are 0 then the timing loop is open.
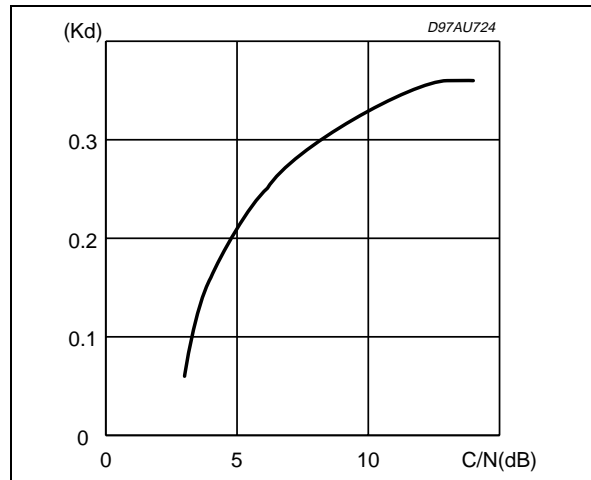
The timing phase detector gain K_D depends on the signal to noise ratio and is given in the following figure:

(see par. 3.8 for the C/N definition)

$K_D = 0.356$ for a noise free input signal.

The natural frequency and the damping factor can be rewritten as:

Phase Detector Gain

$$f_n = 2.064\,\sqrt{F_{CK}}\,\sqrt{m \cdot K_D \cdot 2^{beta\_tmg}}$$

$$\xi = 0.0577\,\sqrt{F_{CK}}\,\sqrt{\frac{m \cdot K_D}{2^{beta\_tmg}}} \cdot 2^{alpha\_tmg}$$

Table 1 gives the natural frequency and the damping factor for the nominal amplitude m = 22, $K_D = 0.356$ and M_CLK = 39.02687179MHz.

In high noise conditions the value of K_D may be reduced up to 25% of its nominal (noise free) value; it is recommended to start with a damping factor, calculated without noise, greater than the usual value of 0.7.

3.4. CARRIER RECOVERY

Also the carrier recovery is completely implemented digitally and comprises a phase and frequency detector, a loop filter, a NCO and a sine/cosine look-up table.

The carrier NCO is the local oscillator for the input quadrature demodulator.

3.4.1 Carrier loop registers

Carrier loop filter parameter register (CARFLTPAR)

Internal address: 8F H

Reset Value: 57H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
alpha_car				**beta_car**			

TABLE 1. Timing loop parameters (m= 22; K_D = 0.356; M_CLK = 39.02687179MHz)

beta_tmg		0	1	2	3	4	5	6	7	8	9	10
fn(Hz)		NA	25	36	51	72	102	144	204	288	408	577
alpha_tmg		Damping factor										
	0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
	1	NA	0.71	0.50	0.36	0.25	0.18	0.13	0.09	0.06	0.04	0.03
	2	NA	1.42	1.01	0.71	0.50	0.36	0.25	0.18	0.13	0.09	0.06
	3	NA	2.85	2.01	1.42	1.01	0.71	0.50	0.36	0.25	0.18	0.13
	4	NA	5.70	4.03	2.85	2.01	1.42	1.01	0.71	0.50	0.36	0.25
	5	NA	11.4	8.06	5.70	4.03	2.85	2.01	1.42	1.01	0.71	0.50
	6	NA	22.8	16.1	11.4	8.06	5.70	4.03	2.85	2.01	1.42	1.01
	7	NA	45.6	32.2	22.8	16.1	11.4	8.06	5.70	4.02	2.85	2.01

Carrier frequency registers (CARINTG)
Internal address: 94 H
Reset Value: 00H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

signed number

This register is formed by the 8 integrator MSBs of the carrier loop filter.
The value of this register, when the system is locked, is an image of the frequency offset.
It may be read or written at any time by the micro.
When written the integrator LSBs are reset.

Carrier NCO frequency setting register (IFFREQ)
Internal address: 93 H   92 H   91 H   90 H

Reset Value   : 00H C1H   1DH   37H

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

IFFREQ4

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

IFFREQ3

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

IFFREQ2

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

IFFREQ1

This register is divided into four bytes.
The LSB byte is named IFFREQ1, the MSB is named IFFREQ4.

The 26 bits value to be written into this register is given by:

$$IFFREQ = INT\left(\frac{IF}{F_{ck}} 2^{26}\right)$$

For example if M_CLK = 39.02687179MHz,
Fck = M_CLK/4

$$IFFREQ = 12655927 = (C11D37)_{HEX}$$

which is the Reset Value.

Actual Carrier Frequency Register (CARFREQ)
Internal address: 96 H, 97 H, 98 H

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

CAR FREQ 3

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

CAR FREQ 2

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

CAR FREQ 1

This register contains the actual carrier frequency value when the system is locked.
It is divided into 3 registers: CARFREQ3, down to 1 (CARFREQ3 is the MSB).
This register may be read at any time and it is useful to store the value of the recovered carrier.
If the system unlocks (due, to a lack of signal etc.) the carrier NCO could be initialized with this value to speed-up the tracking process.

3.4.2 Loop parameters

Like the timing loop the carrier loop is a second

TABLE 2. Carrier loop parameters (m = 22; K_D = 1.26; M_CLK = 39.02687179MHz)

beta_car	0	1	2	3	4	5	6	7	8	9	10
fn(KHz)	NA	0.38	0.54	0.77	1.09	1.54	2.17	3.07	4.35	6.15	8.69
alpha_car						Damping factor					
0	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
1	NA	0.67	0.47	0.34	0.24	0.17	0.12	0.08	0.06	0.04	0.03
2	NA	1.34	0.95	0.67	0.47	0.34	0.24	0.17	0.12	0.08	0.06
3	NA	2.69	1.90	1.34	0.95	0.67	0.47	0.34	0.24	0.17	0.12
4	NA	5.37	3.80	2.69	1.90	1.34	0.95	0.67	0.47	0.34	0.24
5	NA	10.7	7.60	5.37	3.80	2.69	1.90	1.34	0.95	0.67	0.47

order system controlled by two parameters, alpha-car and beta-car, contained in the CARFLTPAR register.

The natural frequency and the damping factor are given in the following formulas:

$$f_n = \sqrt{\frac{m\,K_o\,K_D\,\beta}{2\pi}}$$

where β is programmed by the carrier register beta_car:

$$\beta = 2^{beta\_car-4} \cdot Fsym \quad (Fsym = 1.84MHz)$$

m is the reference value of the AGC2 loop (see AGC2_REF register), K_D is the phase detector gain and Ko is the constant of the carrier NCO:

$$K_O = \frac{2\pi}{2^{26}}\,F_{CK}$$

The damping factor is

$$\xi = \frac{\alpha}{2}\,\sqrt{\frac{mK_o\,K_D}{\beta}}$$

where α is programmed by the carrier register alpha_car:

$$\alpha = 2^{alpha\_car+6}$$

beta_car can only take value from 0 to 15; if beta_car is 0 the loop becames a first order one.

alpha_car can take any value from 0 to 9. If both alpha_car and beta_car are 0 then the loop is open.

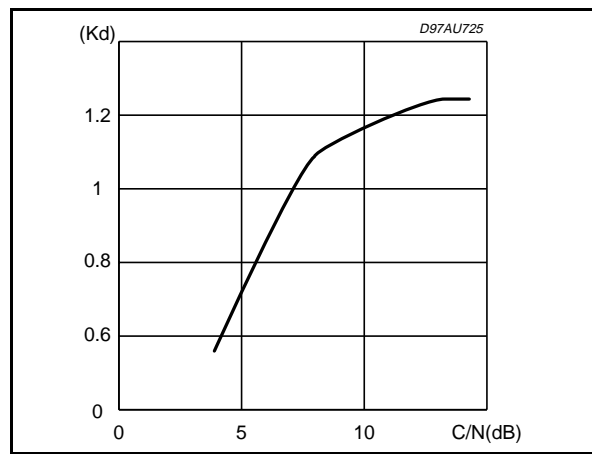K_D depends on the signal to noise ratio and is given in the figure in next column.

(see par. 3.8 for C/N definition)

K_D = 1.26 for a noise free input signal.

The natural frequency and the damping factor can be rewritten as:

$$f_n = 16.515\,\sqrt{F_{CK}}\,\sqrt{m \cdot K_D \cdot 2^{beta\_car}}$$

Phase Detector Gain

$$\xi = 0.0289\,\sqrt{F_{CK}}\,2^{alpha\_car}\,\sqrt{\frac{m \cdot K_D}{2^{beta\_car}}}$$

Table 2 gives the natural frequency and the damping factor for the nominal amplitude m = 22, K_D = 1.26 and M_CLK = 39.02687179MHz.

In presence of noise the value of K_D may be reduced of up to 60%; it is recommended to start with a damping factor, without noise, greater than the usual value of 0.7.

3.4.3 Phase and frequency detector parameter

The carrier phase error is calculated by the following formula : $\varepsilon = I\,sgn(Q) - Q\,sgn(I)$.

This value is computed (at symbol rate) if the actual I and Q components are greater than a programmed threshold otherwise the previous value is mantained. In this way the detector outputs a DC value proportional to the frequency offset between the incoming signal and the local oscillator.

The threshold value may be programmed by the PFDTHR parameter inside the QPSK_CONTROL2 register:

QPSK_CONTROL2 Register

Internal address: 81 H

Reset Value: 90H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
PFDTHR				CNTHR		SN	

The threshold value depends on the signal level at the Nyquist filter output. A good value for this parameter is given by: PFDTHR = 0.4 AGC2REF where AGC2REF is the reference value for the AGC2 loop.

3.4.4 Internal ramp parameter

In presence of a frequency offset greater than the pull-in range of the carrier loop or in presence of low signal to noise ratio the tracking performance of the loop itself may became rather slow. To help the loop in tracking this frequency offset an internal ramp can be activated by I²C bus.

This ramp can be switched on or off by setting the SWON parameter 1 or 0 respectively. When SWON=0 the output value of the ramp is null.

The sweep rate can be calculated by the following formula:

$$\frac{dF}{dt} = \frac{2^{swstep}}{stepper + 1} \frac{F_{ck}^2}{2^{26}}$$

where swstep can only take 0 and 1 values and stepper can be programmed in a range from 0 to 15.

MSB							LSB
X	X	b5	b4	b3	b2	b1	b0

b5 : SWON; 1 = 2 ramp on; 0 = 2 ramp off

b4 : SWSTEP

b3 - b0 : STEPPER

Ramp control register (RAMPCTRL)

Internal address: 95 H

Reset Value: 01H

3.5. AGC1

3.5.1 AGC1 control

To avoid a degradation of the signal to noise ratio a constant IF level is necessary at the channel decoder input.

The AGC1 outputs a signal to control the Variable Gain Amplifier in the RF Front-End in order to mantain a fixed level at the ADC input.

The input signal power (computed after the A/D conversion) is compared to a programmable

threshold; the difference is scaled by the AGC1BETA coefficient then integrated.

The result is converted into a pulse width modulation signal to drive the AGC output pin; it may be filtered by a simple RC filter to control the gain command of a variable gain amplifier before the A to D conversion.

The 8 integrator MSB's (AGC1_ INTG register) may be read or written at any time by the micro; when written, the LSB's are reset.

The integrator value is the level of the AGC output, after low pass filtering; it gives an image of the input signal power. The sign of the loop can be controlled by the AGC1CHS control bit in the QPSK_CONTROL1 register in order to adapt the loop to a positive or negative slope of the variable gain amplifier.

3.5.2 Registers

AGC1 reference level register (AGC1_REF)

Internal address: 83 H 82H

Reset Value   : 01H 06H

MSB							LSB
X	X	X	X	X	X	b9	b8

AGC1_REF2

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

AGC1_REF1

This register is divided into two bytes. The LSB byte is named AGC1_REF1, the MSB is named AGC1_REF2.

The reset value of this register (262) maintains the peak signal input level equal to the half range of the ADC.

AGC1 integrator gain register (AGC1_BETA)

Internal address: 84 H

Reset Value: 00H

MSB							LSB
X	X	X	X	X	b2	b1	b0

AGC1_BETA

The AGC1 loop gain β_{AGC1} is given by:

$$b_{AGC1} = 2^{AGC1\_BETA}$$

The parameter AGC1_BETA can only take values from 0 to 5. When AGC1_BETA is set to "111" the loop gain is null. This condition is useful to open the AGC1 loop.

AGC1 integrator value register (AGC1_INTG)

Internal address: 85 H

Reset Value: 00H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

signed number

To open the AGC1 loop this register must be re-set and the AGC1_BETA parameter must be "111".

3.6. AGC2

3.6.1 AGC2 control

The AGC2 loop is used at the output of the Nyquist / interpolator filter for power optimization in the signal bandwith.

The modulus of the complex signal at the output of the Nyquist filter is compared to a programmable threshold and then scaled by the AGC2_BETA coefficient and integrated.

The integrated error drives two multiplier at the output of both the Nyquist filters in order to maintain constant the level signal at the demodulator output.

3.6.2 Register

AGC2 reference level register (AGC2_REF)

Internal address: 86 H

Reset Value : 16 H

MSB							LSB
X	X	b5	b4	b3	b2	b1	b0

AGC2_REF

The value written in this register corresponds to the modulud of the output complex signal (I,Q).

AGC2 integrator gain register (AGC2_BETA)

Internal address: 87 H

Reset Value: 00H

MSB							LSB
X	X	X	X	X	b2	b1	b0

AGC2_BETA

The AGC2 loop gain β_{AGC2} can be controlled by this register:

$$\beta_{AGC2} = 2^{AGC2\_BETA}$$

The parameter AGC2_BETA can take values from 0 to 6. When AGC2_BETA is set to "111" the loop gain is null and the AGC2 amplifier gain keeps the last value.

AGC2 integrator value register (AGC2_INTG)

Internal address: 88 H

Reset Value: 00H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

signed number

To open the AGC2 loop this register must be re-set and the AGC2_BETA parameter must be "111".

The AGC2 reference level value impacts the value of the following functions:

- Carrier to Noise indicator;
- The carrier loop;
- The timing loop

3.7. LOCK INDICATOR

This 1 bit carrier lock flag may be read at any time.

This flag is available at the chip output and can be also read by the micro in the FLAG register
A low logic level at the Lock Indicator means that a QPSK signal is found.The lock indicator flag controls , internally, the ramp block. The sweep function is disable whenever a lock condition is detected.

3.8. CARRIER TO NOISE INDICATOR

A register is used to estimate the carrier to noise level C/N in a range from 4 to 17dB.

Remark: in the WorldStar system the correspondence between C/N, Eb/No (Energy per net-bit to noise ratio) and Eb/No|$_{QPSK}$ (Energy per channel-bit to noise ratio) are the following:

$$C/N = Eb/No|_{QPSK} + 3dB = Eb/No - 0.6dB$$

The C/N indicator may be used to optimize the antenna pointing or to give an idea of the RF sigal quality. This is based on the measure of the scattering of the QPSK constellation: a 10 bit counter is incremented when the scattering is exceeding a certain value. After a programmable time interval the 8MSB of the counter are loaded in the corresponding I^{2}C-bus register.
The register value strongly depends on the AGC2_REF parameter.

3.8.1 C/N Register (CNCNT)

This register contains a value proportional to the signal to noise ratio at the Nyquist filter output (Eb/No|$_{QPSK}$).

![ST logo]

TABLE 3. Correspondence between C/N and the CNCNT register contents.

C/N(dB)	Eb/No|QPSK	CNTHR = 8			CNTHR = 12			CNTHR = 16		
m = AGC2_ REF		16	22	26	16	22	26	16	22	26
3	0	161	121	101	NA	177	151	NA	NA	193
4	1	155	112	93	NA	173	145	NA	NA	192
5	2	148	102	84	NA	168	138	NA	NA	190
6	3	140	91	73	NA	161	130	NA	NA	186
7	4	132	79	61	NA	155	120	NA	NA	184
8	5	122	68	50	NA	148	110	NA	NA	180
9	6	113	55	38	NA	141	100	NA	NA	177
10	7	105	46	28	NA	134	89	NA	NA	174
11	8	92	33	20	NA	125	79	NA	NA	170
12	9	84	26	13	NA	118	67	NA	NA	165
13	10	71	20	8	NA	112	57	NA	NA	161
14	11	65	14	6	NA	103	51	NA	NA	158
15	12	58	9	3.2	NA	93	40	NA	NA	154
16	13	49	5	1.6	NA	84	32	NA	NA	149
17	14	42	3.4	0.9	NA	77	27	NA	NA	144
18	15	34	2.4	0.5	NA	70	23	NA	NA	141
19	16	32	1.5	0.25	NA	66	19	NA	NA	137
20	17	30	0.9	0.07	NA	61	13	NA	NA	131

The value are the average of 1000 readings of the CNCNT register.

The relation between C/N and the required value (CNCNT) is given in the table 3 for three AGC2 reference levels. A value of 255 means overflow.

3.8.2 Control Register

There are two parameters to control the C/N estimator circuit CNTHR and SN located in the QPSK _CONTROL 2 register.
The CNTHR parameter (2 bits) sets the threshold value under which the circuit is activated.
The SN parameter (2bits) sets the measure time internal.
Both there two parameters are given in the following tables:

CNTHR	THRESHOLD
00	8
01	12
10	16
11	NA

SN	TIME INTERVAL IN SYMBOLS
00	1024
01	4096
10	16384
11	65536

A suitable value of the threshold and time interval must be chosen to have a good level of confidence of the C/N estimate.
To increase the measure accuracy is advisable to average several values.
Before starting the measure the CNCNT register must be reset and can be read after the selected time internal.
A flag bit (CNFLAG) is set to 1 to indicate that a value is available in the CNCNT register.

3.9 CONTROL REGISTERS

QPSK_CONTROL1 register

Internal address: 80 H

Reset Value: 10H

MSB							**LSB**
X	b6	b5	b4	b3	X	X	X

b6 : AGC1CHS

b5 : CAR CHS

b4 :TIMCHS

b3 : QCHP

AGC1CHS changes the polarity of the AGC signal at output pin.

CARCHS and TIMCHS change the sign of the carrier tracking loop and symbol tracking loop respectively.

QCHS inverts the sign of the Q component.

QPSK_CONTROL2 register

Internal address: 81 H

Reset Value: 90H

MSB							**LSB**
b7	b6	b5	b4	b3	b2	b1	b0
PFDTHR				CNTHR		SN	

This register controls the Phase and frequency detector threshold (see par. 3.4.3) and the C/N indicator (see 3.8.2)

FLAG REGISTER

internal address: 99 H

LOCK	CNFLAG						

reserved

This is a read only register when the LOCK bit is 0 then the carrier is locked. When the CNFLAG bit is 1 then the C/N estimation is available.

4. TDM DEMULTIPLEXING

4.1 TDM_MULTIPLEX REGISTERS.

Reg name: TDM_TRSH1

Internal address: 200 H

Type: R/W

Reset Value: 4BH

MSB							**LSB**
X	b6	b5	b4	b3	b2	b1	b0

Description: Master frame preamble recognition - Synchronization threshold level.

Definition of the minimum number of TDM preamble bits to be recognized before enabling the frame synchronization.

Reg name: TDM_TRSH2

Internal address: 201 H

Type: R/W

Reset Value: 43H

MSB							**LSB**
X	b6	b5	b4	b3	b2	b1	b0

Description: Master frame preamble recognition - Warning flag threshold level.

Definition of the minimum number of TDM preamble bits to be recognized before setting an alarm condition.

Reg name: TDM_ALARM

Internal address: 207 H

Type: R/W

Reset Value: 00H

MSB							**LSB**
b7	b6	b5	b4	b3	b2	b1	b0

Description: TDM finite state machine control register (see Table 4).

Reg name: PRC_TRSH1

Internal address: 202 H

Type: R/W

Reset Value: 2AH

MSB							**LSB**
X	X	b5	b4	b3	b2	b1	b0

Description: Prime rate channel preamble recognition - Synchronization threshold level.

Definition of the minimum number of PRC preamble bits to be recognized before enabling PRC synchronization.

Table 4: TDM FSM active states

b7	b6	b5	b4	b3	b2	b1	b0	TDM FSM active states
X	X	X	X	X	0	0	0	mfp_detection, mfp_presync, mfp_sync,alarm 1 (1 cycle)
X	X	X	X	X	0	0	1	mfp_detection, mfp_presync, mfp_sync,alarm 1 (2 cycle)
X	X	X	X	X	0	0	0	mfp_detection, mfp_presync, mfp_sync,alarm 1 (3 cycle)
X	X	X	X	X	0	0	1	mfp_detection, mfp_presync, mfp_sync,alarm 1 (4 cycle)
0	0	0	0	0	1	X	X	mfp_detection, mfp_presync, mfp_sync, alarm 1, alarm 2 (1 cycles)
0	0	0	0	1	1	X	X	mfp_detection, mfp_presync, mfp_sync, alarm 1, alarm 2 (2 cycles)
-	-	-	-	-	1	X	X	mfp_detection, mfp_presync, mfp_sync, alarm 1, alarm 2 (n cycles)
1	1	1	1	1	1	X	X	mfp_detection, mfp_presync, mfp_sync, alarm 1, alarm 2 (32 cycles)

Reg name: PRC_TRSH2

Internal address: 203 H

Type: R/W

Reset Value: 23H

MSB							LSB
X	X	b5	b4	b3	b2	b1	b0

Description: Prime rate channel preamble recognition - Warning flag threshold level.

It defines the minimum number of PRC preamble bits to be recognized before setting an alarm condition.

Reg name: PRC_ALARM

Internal address: 208 H

Type: R/W

Reset Value: 00H

MSB							LSB
b7	b6	b5	b4	X	X	b1	b0

Description: PRC finite state machine control register (see table 5).

Reg name: PRC_ACTIVE_REG

Internal address: 20F H

Type: R

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description: It gives the list of active PRC within one selected BC.

b0 to b7 indicates PRC0 to PRC7 respectively.

Reg name: PRC_LOCK_REG

Internal address: 210 H

Type: R

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description: Lock status of each PRC

b0 to b7 indicates the lock status of PRC0 to PRC7 respectively.

Reg name: PRC_DELAY_REG

Internal address: 211 H

Type: R

MSB							LSB
X	X	X	X	b3	b2	b1	b0

Description: PRC maximum number of delay symbols

It detects the maximum number of delay symbols among the PRC within the same BC.

Table 5: PRC_ALARM

b7	b6	b5	b4	b1	b0	PRC FSM active states
X	X	X	X	0	0	prcp_detection, prcp_presync, prcp_sync
X	X	X	X	0	1	prcp_detection, prcp_presync, prcp_sync, alarm 1
0	0	0	0	1	0	sp_detection, sp_presync, sp_sync, alarm2
0	0	0	1	1	0	sp_detection, sp_presync, sp_sync, alarm2 (1 cycle)
0	0	1	0	1	0	sp_detection, sp_presync, sp_sync, alarm2 (2 cycles)
0	0	1	1	1	0	sp_detection, sp_presync, sp_sync, alarm2 (3 cycles)
-	-	-	-	1	0	sp_detection, sp_presync, sp_sync, alarm2 (n cycles)
1	1	1	1	1	0	sp_detection, sp_presync, sp_sync, alarm2 (16 cycles)
0	0	0	0	1	1	sp_detection, sp_presync, sp_sync, alarm1, alarm2
0	0	0	1	1	1	sp_detection, sp_presync, sp_sync, alarm1, alarm2 (1 cycle)
0	0	1	0	1	1	sp_detection, sp_presync, sp_sync, alarm1, alarm2 (2 cycles)
0	0	1	1	1	1	sp_detection, sp_presync, sp_sync, alarm1, alarm2 (3 cycles)
-	-	-	-	1	1	sp_detection, sp_presync, sp_sync, alarm1, alarm2 (n cycles)
1	1	1	1	1	1	sp_detection, sp_presync, sp_sync, alarm1, alarm2 (16 cycles)

Reg name: PRC_MAXDELAY
Internal address: 206 H
Type: R/W
Reset Value:06H

MSB							LSB
X	X	X	X	X	b2	b1	b0

Description: Maximum accepted number of delay symbols among the prime rate channels belonging to the same broadcast channel.

Reg name: SP_TRSH2
Internal address: 205 H
Type: R/W
Reset Value: 13H

MSB							LSB
X	X	X	b4	b3	b2	b1	b0

Description: Service control header preamble recognition - Warning flag threshold level.

Definition of the minimum number of SCH preamble bits to be recognized before enabling SCH synchronization

Reg name: BC_SEL1, BC_SEL2
Internal address: 209 H , 20AH
Type: R/W
Reset Value: 01H, 00H

BC_SEL1 (LSB)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

BC_SEL2 (MSB)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

Description: Broadcast channel selection

b10 ....b0: BC number selection

b11: Test purpose

b15 ... b12 : Test purpose (must be set at 0 in functional mode)

4.2 INTERRUPT/STATUS REGISTERS

Reg name: CONTROL
Internal address: 20BH
Type: R/W
Reset Value: 00H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description: Control register
b0 : Software reset on
b1 : Software reset enable
b2 : Set TDM out of frame
b3 : ERROR_REG reset on read enable
b4 : Set PRC out of frame
b5 : Set BC out of frame
b6, b7: Test purpose

Reg name: INT_MASK
Internal address: 20CH
Type: R/W
Reset Value: 00H

MSB							LSB
X	b6	b5	b4	b3	b2	b1	b0

Description: Enable/Disable interrupt on INTR pin
b0 : SCCF interrupt mask
b1 : Max Delay Alarm mask
b2 : Illegal Address mask
b3 : TDM out of frame mask
b4 : RS block error mask
b5 : SCH interrupt mask
b6 : Test purpose

Reg name: ERROR_REG
Internal address: 20DH
Type: R/W
Reset Value: 00H

MSB							LSB
X	b6	b5	b4	b3	b2	b1	b0

Description: Interrupt register
b0 : SCCF interrupt on
b1 : Max Delay Alarm on

b2 : Illegal Address on

b3 : TDM out of frame on

b4 : RS block error on

b5 : SCH interrupt on

b6 : Test purpose

Reg name: STATUS REG

Internal address: 20EH

Type: R

Reset Value: 00H

MSB							LSB
X	X	b5	b4	b3	b2	b1	b0

Description: Status register:

b0 : TSCC available

b1 : BC lock

b2 : SCH available

b3 : PRC lock

b4 : MFP lock

b5 : SCCF available

5. VITERBI DECODER AND SYNCHRONIZATION

A Viterbi decoder has been implemented in the STA002 in order to extract the most probable transmitted sequence using a trace back procedure.

This Viterbi decoder has been realized using 64-bit trace back depth and the soft decision approach on the six-bit I and Q components coming from the QPSK demodulator.

The convolutive codes are generated by the polynomials $Gx = 171_{oct}$ and $Gy = 133_{oct}$.

The Viterbi decoder computes for each symbol the metrics of the four possible paths, proportional to the square of the Euclidian distance between the recived I and Q and the theoretical symbol value.

Four logical RAM banks (implemented with eight RAM blocks of 32x64 bits) have been used for the path memory.

The decoding latency is 256 bits.

A bit error (BER) estimator has been integrated in the Viterbi block.

Corrected data bits at Viterbi output are encoded according to the transmission convolutional code so that a "good" stream is obtained. These data are compared with the data stream coming from the QPSK demodulator after having stored it into a memory buffer to compensate the Viterbi la-tency.

The number of wrong bits is accumulated into a register according to a given time base expressed in number of bits and, assuming that the BER at the output of the Viterbi decoder is negligible with respect to the input BER, this count can be read by the system micro controller to evaluate the signal quality after QPSK demodulation.

The error rate measurement is programmable throught the VITERBI_ERROR_CONTROL register and the error rate is available in the registers:

- VIT$_{ERROR}$ 1

- VIT$_{ERROR}$ 2

Reg name: VITERBI_ERROR_CONTROL

Internal address: 204 H

Type: R/W

Reset Value: 00H

MSB							LSB
X	X	X	X	b3	b2	b1	b0

Description: Viterbi input errors measurement windows length and error mode presetting.

		Monitor windows length (bits)
b1b0 =	00	1024
	01	4096
	10	16384
	11	65536
		Error Measurement Mode
b2 =	0	Single acquisition mode
b2 =	1	Continuous acquisition mode
b3 =	0	End measurement (single /continuous acquisition)
b3 =	1	Single acquisition start

Reg name: VIT_ERR0R1, VIT_ERROR2

Internal address: 213 H , 214H

Type: R/W

VIT_ERROR 1 (ERROR COUNTER LOW)

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0

VIT_ERROR 2 (ERROR COUNTER HIGH)

MSB							LSB
A15	A14	A13	A12	A11	A10	A9	A8

Description: Viterbi error counter register

6. REED SOLOMON DECODER

The STA 002 performs a real time block decoding operation both on the Time Slot Control Channel (TSCC) field and on the Broadcast Channel (BC) stream by means of a programmable Reed-Solomon (RS) decoder.

This decoder works on blocks of 255 words of 8 bit symbols where the first 223 words represent the information and the last 32 the code redundancy.

The synchrobyte is the first byte of the block.

All the correction capability of the code is used so it is possible the correction of blocks containing up to 16 errors while blocks with greater number of errors are flagged as corrupted.

The RS decoder is programmable to support two different Galois field generator polynomials as required by WorldSpace specifications and includes an integrated BER estimator.

Monitoring the number of wrong words in each block and correlating this number with the block length, it is possible, provided that no corrupted blocks are present, to get an estimation of the signal quality at the Viterbi decoder output.

6.1 TSCC REED SOLOMON DECODER

The code generator polynomial is:

$$g(X) = \prod_{J=112}^{143} (x - \alpha^{11J})$$ over the Galois Field

generated by $X^8+X^7+X^2+X+1$.

6.2 BROADCAST CHANNEL RS DECODER AND DESCRAMBLER.

The code generator polynomial is:

$$g(x) = (x-\omega^\circ) (x-\omega^1) (...) (x-\omega^{31})$$

over the Galois Field generated by:

$$X^8+X^4+X^3+X^2+1=0$$

6.3 ENERGY DISPERSAL DESCRAMBLER

The descrambler generator polynomial is:

$$X^9+X^5+1$$

Reg name: RS_ERROR_CONTROL

Internal address: 212H

Type: R/W

Reset Value: 00H

MSB							LSB
X	X	X	X	b3	b2	b1	b0

Description: Reed Solomon input errors measurement windows length and error mode presettings

Monitor windows length (blocks)

b1b0 =	00	3
	01	64
	10	256
	11	1024

Error Measurement Mode

b2	=	0	Single acquisition mode
b2	=	1	Continuous acquisition mode
b3	=	0	End measurement (single /continuous acquisition
b3	=	1	Single acquisition start

Reg name: RS_BYTE_ERROR1,

   RS_BYTE_ERROR2

Internal address: 215 H , 216H

Type: R/W

RS_BYTE_ERR0R1 (ERROR COUNTER LOW)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

RS_BYTE_ERROR 2 (ERROR COUNTER HIGH)

MSB							LSB
X	X	b13	b12	b11	b10	b9	b8

Description: RS byte error counter register

Reg name: RS_BLOCK_ERROR

Internal address: 217H

Type: R/W

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description: RS block error counter register

7. BROADCAST CHANNEL DEMULTIPLEXER
7.1 SCH REGISTER

Reg name: BRI_REG & NSC_REG
Internal address: 000H
Type: R

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description:
b7 to b4 indicate the bit rate of the BC
(BRI field in the SCH)
0000: no valid data
0001: 16Kbps
....
1000 : 128Kbps
1001 - 1111: RFU
b3 = 0
b2 to b0 indicate the number of service components (NSC field in the SCH)
000: one Service Component
001: two Service Component
....
111: eight Service Component

Reg name: EC_REG
Internal address: 001H
Type: R

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description:
b7 to b4 = 0000
b3 to b0 indicate the encryption strategy (Encryption Control field in the SCH)
0000: no encryption
0001: static Key
0010: ESI, common key, subscription period A
0100: ESI, broadcast channel specific key for subscription period A
0101: ESI, broadcast channel specific key for subscription period B
else: RFU

Reg name: AFCI1_REG
Internal address: 002H
Type: R

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description :
b7 to b5 = 000
b4 to b0 indicate the Auxiliary field content indicator 1 (ACI1l field in the SCH)
00000: not used
00001: 16 bit encryption key selector
00010: RDS PI code
00011: Associated Broadcast Channel reference (PS flag and ASP)
else: RFU

Reg name: AFCI2_REG
Internal address: 003H
Type: R

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description:
b7 : 0
b6 to b0 indicate the Auxiliary field content indicator 2 (ACI2 field in the SCH)
00000: not used
00001:64 bit encryption key selector
00010: Service Label
else: RFU

Reg name: SOF_SF_REG
Internal address: 0041H
Type: R

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description:
b7 to b5 = 000
b4 indicate the ADF2 multiframe start flag (SF field in the SCH)
1: first segment of multiframe or no multiframe
0: intermediate segment of multiframe
b3 to b0 indicate the segment offset and lenght field (SFT field in the SCH) if SF = 1 SOLF contains the total number of multiframe segments minus 1.

0000: one segment multiframe

0001: two segment multiframe

....

1111: 16 segment multiframe

if SF = 0 SOLF contains the segment offset.

Reg name: ADF1_REG

Internal address: 006H, 005H

Type: R

ADF1 (15:8) (addr 006H)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

ADF1 (7:0) (addr 005H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description:

b15 to A0 contain the Auxiliary data field1 (ADF1 field in the SCH) with content defined by AFCI1_REG)

Reg name: ADF2_REG

Internal address: 00EH,00DH, 00CH, 00BH,
  00AH, 009H, 008H, 007H,

Type: R

ADF2(63:56) (addr 00EH)

MSB							LSB
b63	b62	b61	b60	b59	b58	b57	b56

ADF2(55:48) (addr 00DH)

MSB							LSB
b55	b54	b53	b52	b51	b50	b49	b48

ADF2(47:40) (addr 00CH)

MSB							LSB
b47	b46	b45	b44	b43	b42	b41	b40

ADF2(39:32) (addr 00BH)

MSB							LSB
b39	b38	b37	b36	b35	b34	b33	b32

ADF2(31:24) (addr 00AH)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

ADF2(23:16) (addr 009H)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

ADF2(15:8) (addr 008H)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

ADF2(7:0) (addr 007H)

MSB							LSB
A7	A6	A5	A4	A3	A3	A1	A0

Description:

b64 to b0 contain the Auxiliary data field2 (ADF2 field in the SCH) with content defined by AFCI2_REG)

Reg name: SEL_SC_REG

Internal address: 00FH

Type: R/W

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description :

b7: =1 Enable service component selection A
  = 0 Disable

b6 to b4 contain the Service Component selection A

000: SC1

001: SC2

....

111: SC8

b3: =1 Enable service component selection B
  = 0 Disable

b2 to b0 contain the Service Component selection B

000: SC1

001: SC2

....

111: SC8

Reg name: PIW_ RAM

Internal address: 03F,03E, 03D, 03C,
03B, 03A, 039, 038,

Type: W

PIW_RAM (63:56) (addr 03F)

MSB							LSB
b63	b62	b61	b60	b59	b58	b57	b56

PIW_RAM (55:48) (addr 03E)

MSB							LSB
b55	b54	b53	b52	b51	b50	b49	b48

PIW_RAM (47:40) (addr 03D)

MSB							LSB
b47	b46	b45	b44	b43	b42	b41	b40

PIW_RAM (39:32) (addr 03C)

MSB							LSB
b39	b38	b37	b36	b35	b34	b33	b32

PIW_RAM (31:24) (addr 03B)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

PIW_RAM (23:16) (addr 03A)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

PIW_RAM (15:8) (addr 039)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

PIW_RAM (7:0) (addr 038)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description:

b63 tob0 contain the prestored initialization word 0 which is the only one downloadable by the processor.

Reg name: EM_REG

Internal address: 018H

Type: R/W

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description :

Encryption mode register

b7 to b1 = not used RFU

b0 indicate the encryption mode (1)

1: normal encryption mode

0: enable blocking

(1) for more information refer to document number WST-WSG-DDS-003-500000 Chipset Encryption Implementation Specification for World space receiver

Reg name: PIWE_REG

Internal address: 01AH, 019H

Type: R/W

PIWE (15:8) (addr 01AH)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

PIWE (7:0) (addr 019H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description :

b15 to b0 contain the 16 BIT static key selector word. Each bit PIWE enables a certain static key. If bit A0 of PIWE is set, the static key 0 will be enabled for read out and so forth.

Reg name: BCIN_DELAY_REG

Internal address: 01BH

Type: R/W

Default 00H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description : BC input delay and BC input enable register

b0: enables external BC input

BC input delay (bytes)

b2b1 = 00 1
        01 2
        10 3
        11 4

b3: Test purpose (must be set at 0 in functional mode)

b7 to b4: test purpose

Reg name: BC_ALARM_REG

Internal address: 01CH

Type: R/W

Default:20H

MSB							LSB
X	X	b5	b4	b3	b2	b1	b0

Description: BC finite state machine control register (see table 6)

b5 indicates the BC synchronization mode

1: SP preamble detection

0: Synch from PRC

Reg name: IW_REG

Internal address: 017, 016, 015, 014,
                  013, 012, 011, 010,

Type: W

IW_REG (63:56) (addr 017)

MSB							LSB
b63	b62	b61	b60	b59	b58	b57	b56

IW_REG (55:48) (addr 016)

MSB							LSB
b55	b54	b53	b52	b51	b50	b49	b48

IW_REG (47:40) (addr 015)

MSB							LSB
b47	b46	b45	b44	b43	b42	b41	b40

IW_REG (39:32) (addr 014)

MSB							LSB
b39	b38	b37	b36	b35	b34	b33	b32

IW_REG (31:24) (addr 013)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

IW_REG (23:16) (addr 012)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

IW_REG (15:8) (addr 011H)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

IW_REG (7:0) (addr 010H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

Description:

b63 to b0 contain the initialization word IW.

Table 6: BC_ALARM_REG

b4	b3	b2	b1	b0	BC FSM active states
0	0	0	0	0	sp_detection, sp_presync, sp_sync
1	0	0	0	0	sp_detection, sp_presync, sp_sync, alarm_state (1 cycle)
1	0	0	0	1	sp_detection, sp_presync, sp_sync, alarm_state (2 cycles)
1	0	0	1	0	sp_detection, sp_presync, sp_sync, alarm_state (3 cycles)
1	0	0	1	1	sp_detection, sp_presync, sp_sync, alarm_state (4 cycles)
1	-	-	-	-	sp_detection, sp_presync, sp_sync, alarm_state (n cycles)
1	1	1	1	0	sp_detection, sp_presync, sp_sync, alarm_state (15 cycles)
1	1	1	1	1	sp_detection, sp_presync, sp_sync, alarm_state (16 cycles)

SCH_MEM REGISTERS

Service Component Control Field (SCCF)

Reg name: SERVICE COMPONENT 1

Internal address: 100H, 101H, 102H, 103H

Type: R

Description :

Contains information about the service component of the broadcast channel

SC1_LENGHT & SC1_TYPE (addr 100H)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

SC1_EC & SC1_PT (addr 101H)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

SC1_PT (addr 102H)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

LANGUAGE 1 (addr 103H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

b31 to b28 = SC length Bit rate of the service component divided by 8 kbps:

0000: 8 kbps

0001: 16 kbps

....

1111: 128 kbps

b27 to b24 = SC type

Type of service component:

0000: MPEG

0001: general data

0100:JPEG

0101: MPEG

0101: Low bit rate video

1111: invalid data

else: RFU

b23 = Encryption flag

0: not encrypted SC

1: encrypted SC

b22 to b8 = Program type

b7 to b0 = SC language

Reg name: SERVICE COMPONENT 2

Internal address: 104H, 105H, 106H, 107H

Type: R

Description :

Contains information about the service component of the broadcast channel

SC2 _LENGHT & SC2_TYPE(addr 104H)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

SC2 _EC & SC2_PT (addr 105H)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

SC2_PT (addr 106H)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

LANGUAGE 2 (addr 107H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

b31 to b28 = SC length Bit rate of the service component divided by 8 kbps:

0000: 8 kbps

0001: 16 kbps

....

1111: 128 kbps

b27 to b24 = SC type

Type of service component:

0000: MPEG

0001: general data

0100:JPEG

0101: Low bit rate video

1111: invalid data

else: RFU

b23 = Encryption flag

0: not encrypted SC

1: encrypted SC

b22 to b8 = Program type

b7 to b0 = SC language

Reg name: SERVICE COMPONENT 3

Internal address: 108H, 109H, 10AH, 10BH

Type: R

Description :

Contains information about the service component of the broadcast channel

SC3_LENGHT & SC3_TYPE (addr 108H)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

SC3 _EC & SC3_PT(addr 109H)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

SC3_PT (addr 10AH)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

LANGUAGE 3 (addr 10BH)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

b31 to b28 = SC length Bit rate of the service component divided by 8 kbps:

0000: 8 kbps

0001: 16 kbps

....

1111: 128 kbps

b27 to b24 = SC type

Type of service component:

0000: MPEG

0001: general data

0100:JPEG

0101: Low bit rate video

1111: invalid data

else: RFU

b23 = Encryption flag

0: not encrypted SC

1: encrypted SC

b22 to b8 = Program type

b7 to b0 = SC language

Reg name: SERVICE COMPONENT 4

Internal address: 10CH, 10DH, 10EH, 10FH

Type: R

Description :

Contains information about the service component of the broadcast channel

SC4_LENGHT & SC3_TYPE (addr 10CH)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

SC4_EC & SC3_PT (addr 10DH)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

SC4 _PT(addr 10EH)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

LANGUAGE 4 (addr 10FH)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

b31 to b28 = SC length Bit rate of the service component divided by 8 kbps:

0000: 8 kbps

0001: 16 kbps

....

1111: 128 kbps

b27 to b24 = SC type

Type of service component:

0000: MPEG

0001: general data

0100: JPEG

0101: Low bit rate video

1111: invalid data

else: RFU

b23 = Encryption flag

0: not encrypted SC

1: encrypted SC

b22 to b8 = Program type

b7 to b0 = SC language

Reg name: SERVICE COMPONENT 5

Internal address: 110H, 111H, 112H, 113H

Type: R

Description :

Contains information about the service component of the broadcast channel

SC5 _LENGHT & SC5_TYPE(addr 110H)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

SC5_EC & SC5_PT(addr 111H)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

SC5_PT (addr 112H)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

LANGUAGE 5(addr 113H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

b31 to b28 = SC length Bit rate of the service component divided by 8 kbps:

000: 8 kbps

001: 16 kbps

....

1111: 128 kbps

b27 to b24 = SC type

Type of service component:

0000: MPEG

0001: general data

0100: JPEG

0101: Low bit rate video

1111: invalid data

else: RFU

b23 = Encryption flag

0: not encrypted SC

1: encrypted SC

b22 to b8 = Program type

b7 to b0 = SC language

Reg name: SERVICE COMPONENT 6

Internal address: 114H, 115H, 116H, 117H

Type: R

Description :

Contains information about the service component of the broadcast channel

SC6 _LENGHT & SC6_TYPE(addr 114H)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

SC6 _EC & SC6_PT(addr 115H)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

SC6_PT (addr 116H)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

LANGUAGE6 (addr 117H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

b31 to b28 = SC length Bit rate of the service component divided by 8 kbps:

0000: 8 kbps

0001: 16 kbps

....

1111: 128 kbps

b27 to b24 = SC type

Type of service component:

0000: MPEG

0001: general data

0100: JPEG

0101: Low bit rate video

1111: invalid data

else: RFU

b23 = Encryption flag

0: not encrypted SC

1: encrypted SC

b22 to b8 = Program type

7 to b0 = SC language

Reg name: SERVICE COMPONENT 7

Internal address: 118H, 119H, 11AH, 11BH

Type: R

Description :

Contains information about the service component of the broadcast channel

SC7_LENGHT & SC7_TYPE (addr 118H)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

SC7 _EC & SC7_PT(addr 119H)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

SC7_PT (addr 11AH)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

LANGUAGE7 (addr 11BH)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

b31 to b28 = SC length Bit rate of the service component divided by 8 kbps:

0000: 8 kbps

0001: 16 kbps

....

1111: 128 kbps

b27 to b24 = SC type

Type of service component:

0000: MPEG

0001: general data

0100: JPEG

0101: Low bit rate video

1111: invalid data

else: RFU

b23 = Encryption flag

0: not encrypted SC

1: encrypted SC

b22 to b8 = Program type

b7 to b0 = SC language

Reg name: SERVICE COMPONENT 8

Internal address: 11CH, 11DH, 11EH, 11FH

Type: R

Description :

Contains information about the service component of the broadcast channel

SC8 _LENGHT & SC38_TYPE(addr 11CH)

MSB							LSB
b31	b30	b29	b28	b27	b26	b25	b24

SC8 _EC & SC8_PT(addr 11DH)

MSB							LSB
b23	b22	b21	b20	b19	b18	b17	b16

SC8 _PT (addr 11EH)

MSB							LSB
b15	b14	b13	b12	b11	b10	b9	b8

LANGUAGE8 (addr 11FH)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0

b31 to b28 = SC length Bit rate of the service component divided by 8 kbps:

0000: 8 kbps

0001: 16 kbps

....

1111: 128 kbps

b27 to b24 = SC type

Type of service component:

0000: MPEG

0001: general data

0100: JPEG

0101: Low bit rate video

1111: invalid data

else: RFU

b23 = Encryption flag

0: not encrypted SC

1: encrypted SC

b22 to b8 = Program type

b7 to b0 = SC language

8. GENERAL INFORMATION

8.1 DECRIPTION

The STA002 supports a crypto-scheme named WES (World Space Encrypton Scheme)

It is composed of two functional blocks:

- CSG (Crypto Sequence Generator) implemented in the STA002 decoder
- IWG (Initialization Word Generator) processed by external hardware such as a microcontroller or a smart card.

The CSG module produces the pseudo-casual sequence by an algorithm based on the galois arrithmetic.

This algorithm is derived in 2 phases:

1) Key expansion

2) Pseudo casual sequence generation

In the expansion phase activated every frame the IWG 8 bytes key is used to initialize a 16 bytes array.
The scrambling procedure, invoked every byte, implements a pseudo random algorithm.
The XOR operation between the output of the module the encrypted bytes completes the decryption procedure.
The 8 bytes keyword is loaded before the start of the new frame to the I^2C bus interface.

8.2. BROADCAST CHANNEL INTERFACE

The Broadcast Channel interface consists of 4 wires: output clock (BCCK), output BC data (BCDO), output BC frame sync. (BCSYNC) and input BC data (BCDIN).

The data trasmitted and recived via the broadcast channel interface are 8 bit bursts.

The most significant bit is transmitted first.

Fig.7 shows the broadcast channel serial data out (BCDO) burst of 8 bit (MSB first). The data bits are valid at the negative slope of the clock line (BCCK).

The BCSYNC signal indicates the first byte of the broadcast channel Service preamble (04H) allowing an easy syncronization to external modules using the BC data.
The input BC line (BCDI) must have the same format of the BC output (BCDO). The data bit must be valid on the negative edge of the output clock line (BCCK).
The maximum delay allowed from the output data and the input data is 4 bytes (4 bursts of 8 bits). The input delay is programmable via I2C bus with the BCIN_DELAY_REG register (01BH).

8.3 SERVICE COMPONENT INTERFACES

The STA002 provides two service component interfaces which support the same protocol:

- SC DATA INTERFACE (SCEN, SCDO, SCCK)

- SOURCE DECODER INTERFACE (SEN, SDO, SCK)

The service component interfaces consists of 3 wires each. Output clock (SCCK/SCK), SC data (SCDO/SDO) and SC byte sync (SCEN/SEN).

The data transmitted via the service component interface are 8 bit bursts.
The most significant bit is transmitted first.
As shown in fig.8 the service component serial data out (SCDO/SDO) combines burst of 8 bit length (MSB first). The data bit are valid at the negative edge of the clock line (SCCK/ SCK).

The slope change of the SCEN/SEN indicates the most significative bit of the 8 bit service component burst.

The SCEN/SEN signal is used if required for the data bits alignement only.

Fig. 7: Format Of The Broadcast Channel Interface (BC)
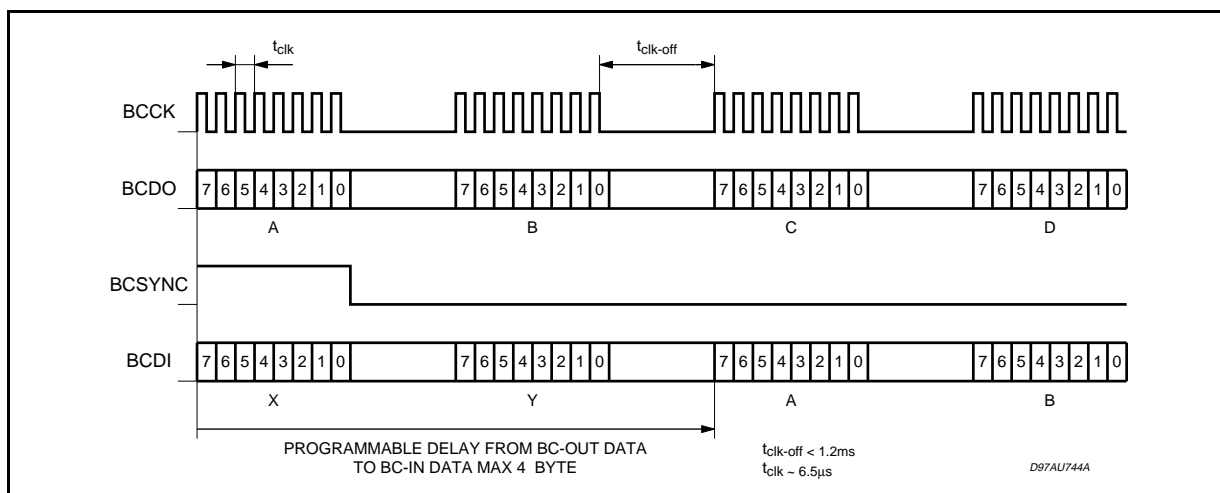
Fig. 8: Format Of The Service Component Interface
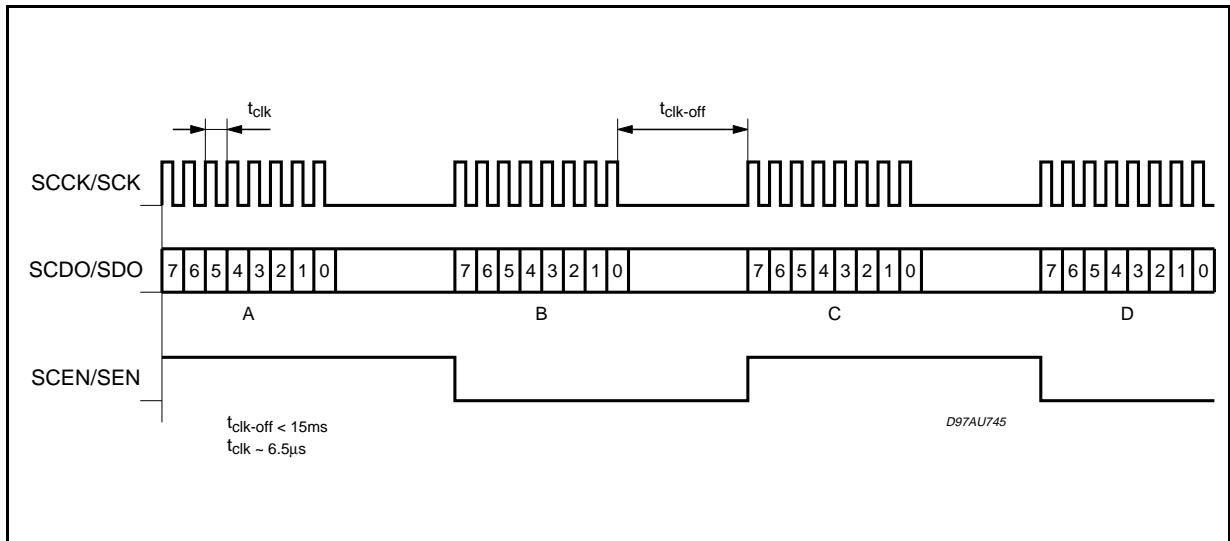
CHANNEL DECODER INTERFACES BLOCK DIAGRAM
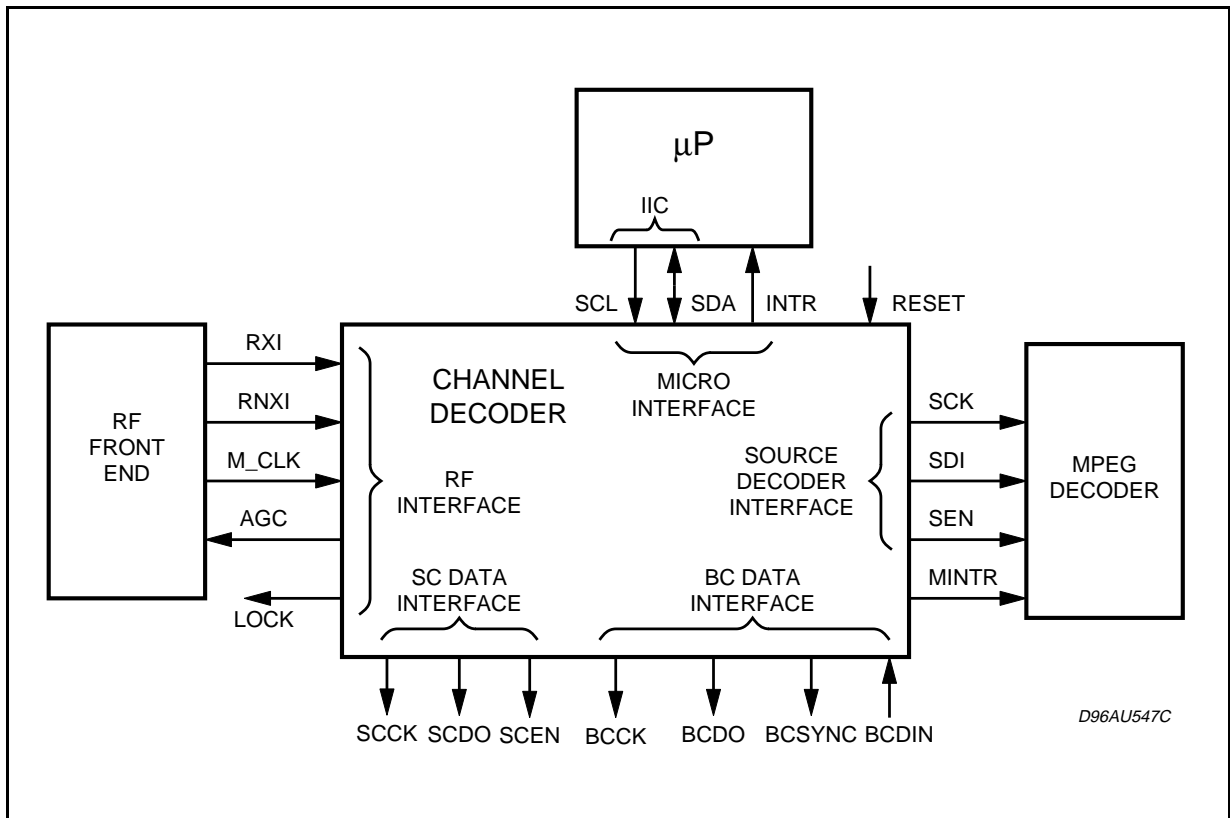
8.4 FRAME SYNCRONIZATION TIMES

FRAME SYNCRONIZATION
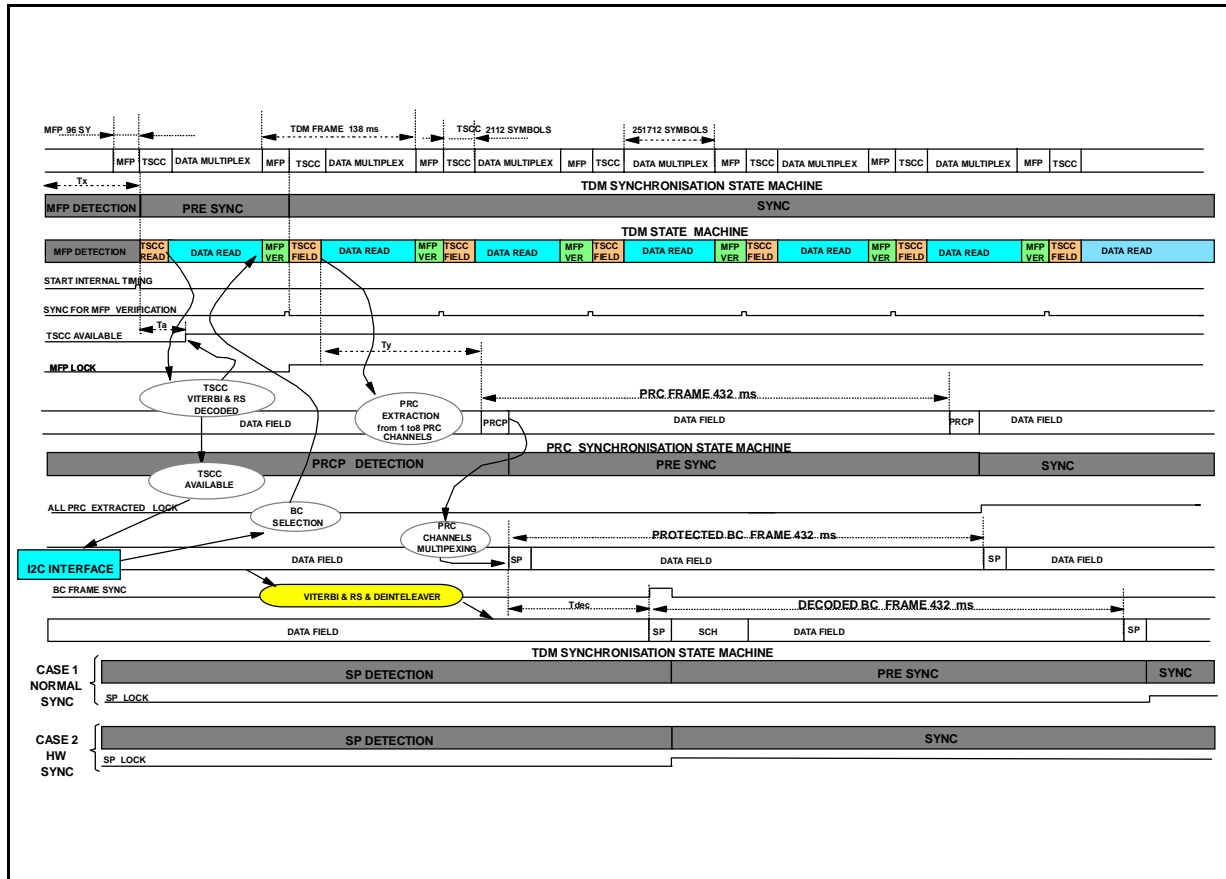
Tx = MFP detection time: 0 to 138ms

Ta = TSCC decodification time:= < 2ms

Ty = PRCP detection time: 0 to 432ms

Tdec = VITERBI decoding +
  REED SOLOMON error correction +
  deinterleaving: ~55ms x PRC number

TDM SYNCRONIZATION TIME
TDM lock = QPSK lock + Tx + 138ms

PRC SYNCRONIZATION TIME
PRC lock = QPSK lock +TDM lock + Ty + 432 ms

BC SYNCRONIZATION TIME
CASE 1 (SW sync):
the BC synchronization FSM asserts the lock sig-

nal when the SP is detected two consecutive times.

BC lock = QPSK lock + TDM lock + Ty + Tdec + 432 ms

CASE 2 (HW sync):

the BC synchronization FSM asserts the lock signal when the BC FRAME SYNC signal is asserted by the PRC alignment FSM and the SP is valid.

BC lock = QPSK lock + TDM lock + Ty + Tdec

Note :
About the BC synchronisation, the selection between SW sync and HW syn is achievable through the register BC_ALARM add 01CH bit b5.
Bit b5 = 1 indicates the SW sync Bit b5 = 0 indicates HW sync.

SCH & SCCF INTERRUPT
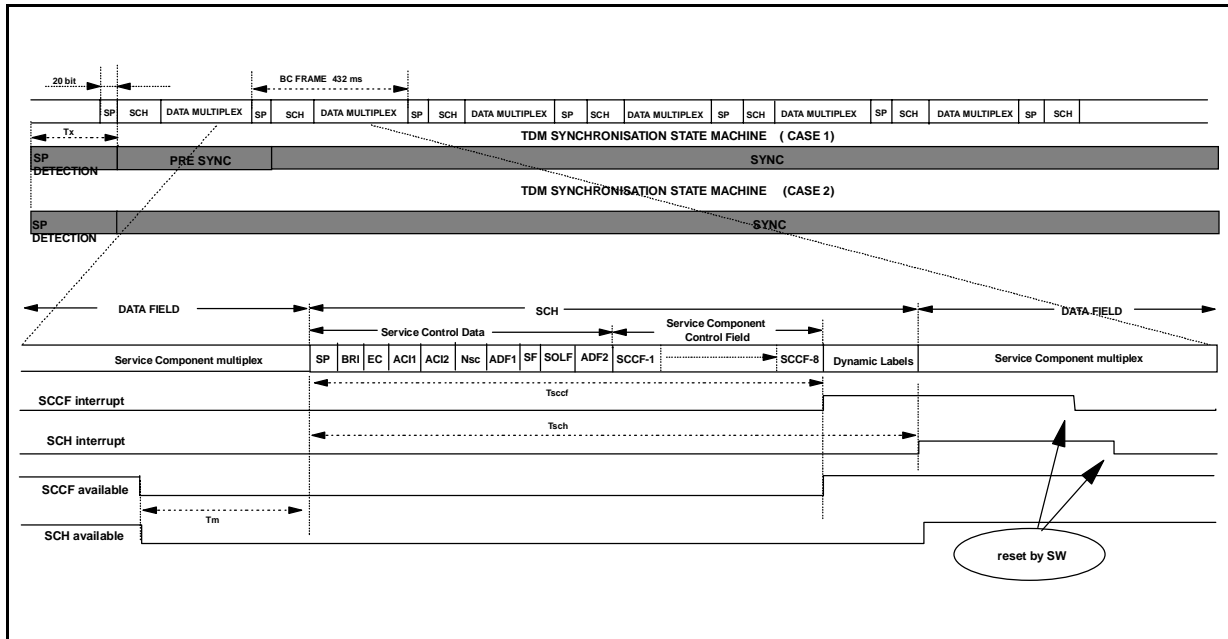
Tm = SCCF/ SCH not available setup ~ 32 ms

Tsch = SCH interrupt time ~ 1 3.5 ms

Tsccf = SCCF interrupt time ~

$$\frac{432}{7136 \cdot BRI} \cdot 128 + Nsc \cdot 32ms$$

BRI = Bit Rate Index (from 1 to 8)

Nsc = number of Service Component (from1 to 8)

8.5 LOSS OF SYNC TABLE

	MPF	PRC	BC	TSCC available	SCH available	SCCF available
TDM Out of Frame	unlocked	unlocked	unlocked	not available	*	*
PRC Out of Frame	locked	unlocked	unlocked	available	*	*
BC Out of Frame	locked	locked	unlocked	available	*	*

CONTROL REGISTER			STATUS REGISTER					
TDM OOF b2	PRC OOF b4	BC OOF b5	MFP lock b4	PRC lock b3	BC lock b1	TSCC available b0	SCH available b2	SCCF available b5
0	0	0	1	1	1	1	1	1
1	X	X	0	0	0	0	*	*
0	1	X	1	0	0	1	*	*
0	0	1	1	1	0	1	*	*

* Meaningful only if all the sync levels (MFP, PRC, BC) are locked otherwise not significant

8.6 I/O CELL DESCRIPTION

1) CMOS Output Pad Buffer, 2mA, with Slew Rate Control / Pins number 2, 13, 18, 24, 27, 28, 29, 31, 36, 37, 39, 41, 43

D98AU920
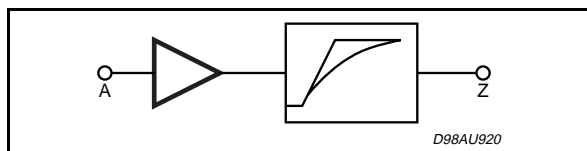
OUTPUT PIN	MAX LOAD
Z	50pF

2) CMOS Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control / Pin number 10

D98AU921
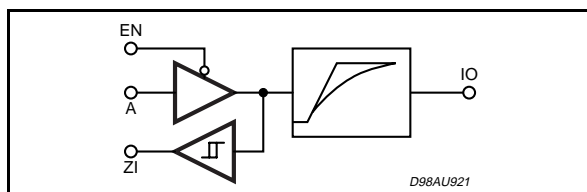
INPUT PIN	CAPACITANCE	OUTPUT PIN	MAX LOAD
IO	5pF	IO	100pF

3) CMOS Schmitt Trigger Input Pad Buffer / Pin number 16

D98AU923
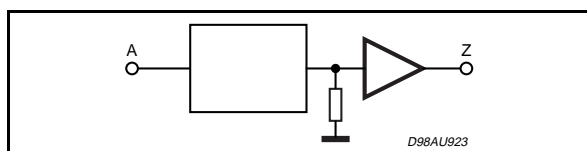
INPUT PIN	CAPACITANCE
A	3.5pF

4) CMOS Input Pad Buffer with Active Pull-Down / Pins number 11, 11, 12

D98AU923
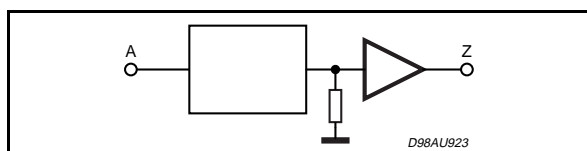
INPUT PIN	CAPACITANCE
A	3.5pF

5) CMOS Input Pad Buffer / Pins number 10, 22, 23, 25, 32, 33, 34, 44

D98AU906
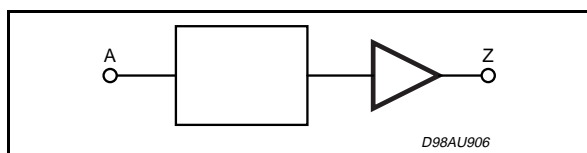
OUTPUT PIN	CAPACITANCE
A	3.5pF

6) CMOS Input Pad Buffer with Active Pull-Up / Pin number 20

D98AU907
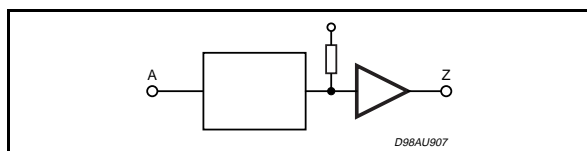
OUTPUT PIN	CAPACITANCE
A	3.5pF

I/O CELL DESCRIPTION (Continued)

7) Analog Pad Buffer / Pins number 5, 6

D98AU924
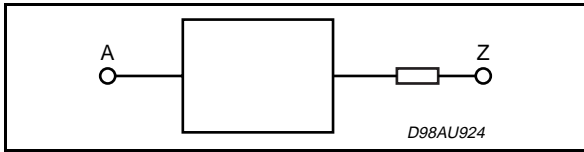
OUTPUT PIN	CAPACITANCE
A	4pF

8) M_CKL Input Stage / Pin number 9

D98AU925
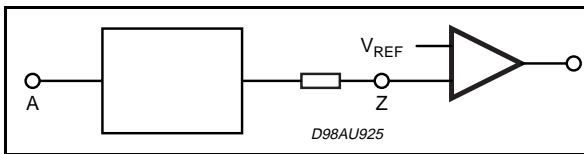
OUTPUT PIN	TOTAL CAPACITANCE
A	4pF

9) RXI/NRXI Input Stage / Pins number 5, 6

D98AU926
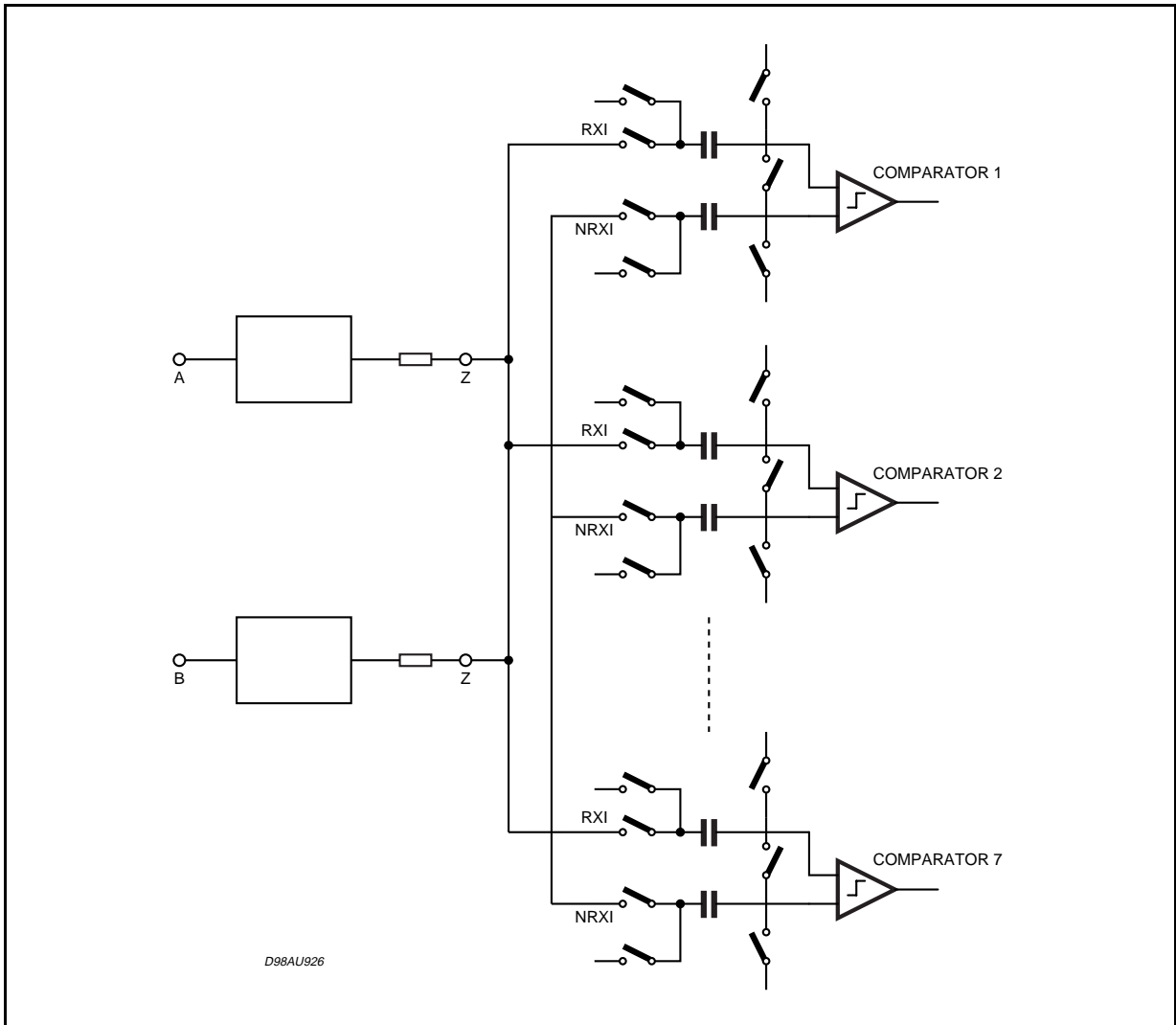
INPUT PIN	CAPACITANCE
A/AI	4pF

NRXI Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
C_m	Common Mode Voltage		V_{DD} -0.5		V	1
C_{mr}	Common Mode Voltage Range	V_{DD} -2		V_{DD} -0.3	V	2
D_{iV}	Differential Input Voltage			1V Peak to Peak	V	

Note 1: VA = VB Open circuit voltage

Note 2; VA = VB

8.7 APPLICATION NOTE (Registers preset)

According to the choosen M_CLK frequency some registers values must be changed.

Table 7 shows two different presets for M_CLK = 39.0268MHz and M_CLK = 14.72MHz

Table 7:

HEX_COD	DEC_COD	REGISTER NAME	M_CLK = 39.0268MHz PRESET	M_CLK = 14.72MHz PRESET
80H	128	QPSK_CONTROL1	38H	38H
81H	129	QPSK_CONTROL2	50H	50H
82H	130	AGC1_REF1	C8H	C8H
83H	131	AGC1_REF2	00H	00H
84H	132	AGC1_BETA	05H	05H
8AH	138	SYM_FREQ1	D3H	00H
8BH	139	SYM_FREQ2	11H	00H
8CH	140	SYM_FREQ_	0CH	10H
8DH	141	TIM_FLT_PAR	44H	44H
8FH	143	CAR_FLT_PAR	22H	22H
90H	144	IF_FREQ1	37H	00H
91H	145	IF_FREQ2	1DH	00H
92H	146	IF_FREQ3	C1H	00H
93H	147	IF_FREQ4	00H	01H
95H	149	RAMP_CTRL	20H	20H
200H	512	TDM_TRSH1	3CH	3CH
201H	513	TDM_TRSH2	3CH	3CH
202H	514	PRC_TRSH1	20H	20H
203H	515	PRC_TRSH2	20H	20H
21EH	542	PLL_INT_REG	00H	01H
220H	544	RESERVED1	06H	06H
223H	547	RESERVED4	02H	02H

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA

TQFP44 (10 x 10)

TQFP4410