



## STB50NH02L

### N-CHANNEL 24V - 0.011 $\Omega$ - 50A D<sup>2</sup>PAK STripFET™ III POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB50NH02L	24 V	< 0.0135 $\Omega$	50 A

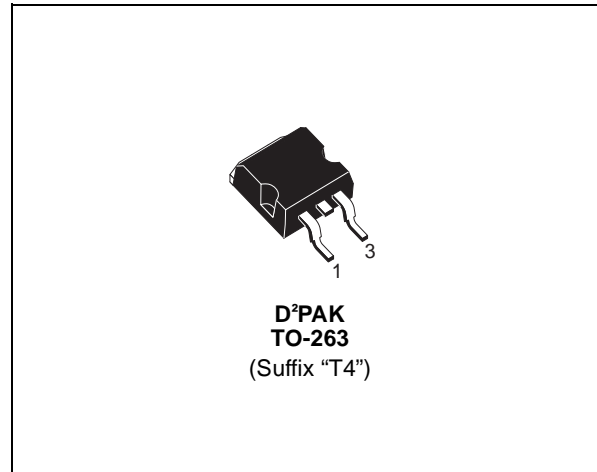
- TYPICAL R<sub>DS(on)</sub> = 0.011  $\Omega$  @ 10 V
- TYPICAL R<sub>DS(on)</sub> = 0.015  $\Omega$  @ 5 V
- R<sub>DS(ON)</sub> \* Q<sub>g</sub> INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE-MOUNTING D<sup>2</sup>PAK (TO-263)  
POWER PACKAGE IN TUBE (NO SUFFIX) OR  
IN TAPE & REEL (SUFFIX "T4")

#### DESCRIPTION

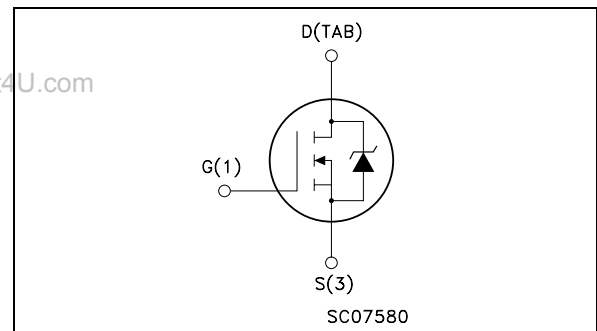
The STB50NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter applications where high efficiency is to be achieved.

#### APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS



#### INTERNAL SCHEMATIC DIAGRAM



#### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>spike(1)</sub>	Drain-source Voltage Rating	30	V
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	24	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	24	V
V <sub>GS</sub>	Gate- source Voltage	$\pm$ 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	50	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	36	A
I <sub>DM(2)</sub>	Drain Current (pulsed)	200	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	60	W
	Derating Factor	0.4	W/°C
E <sub>AS(3)</sub>	Single Pulse Avalanche Energy	200	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature		

**STB50NH02L****THERMAL DATA**

Rthj-case	Thermal Resistance Junction-case	Max	2.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose		300	°C

**ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)**

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 25 mA, V <sub>GS</sub> = 0	24			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 20 V V <sub>DS</sub> = 20 V T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			±100	nA

ON (4)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	1	1.8		V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 25 A V <sub>GS</sub> = 5 V I <sub>D</sub> = 12.5 A		0.011 0.015	0.0135 0.025	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (4)	Forward Transconductance	V <sub>DS</sub> = 10 V I <sub>D</sub> = 19 A		19		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>riss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 15V f = 1 MHz V <sub>GS</sub> = 0		1070 305 45		pF pF pF
R <sub>G</sub>	Gate Input Resistance	f=1 MHz Gate DC Bias=0 Test Signal Level =20 mV Open Drain		1		Ω

**STB50NH02L****ELECTRICAL CHARACTERISTICS (continued)****SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 10\text{ V}$ $I_D = 25\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, Figure 3)		7 62		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$0.44 \leq V_{DD} \leq 10\text{ V}$ $I_D = 50\text{ A}$ $V_{GS} = 10\text{ V}$		18 4 2.5	24	nC nC nC
$Q_{oss}^{(5)}$	Output Charge	$V_{DS} = 16\text{ V}$ $V_{GS} = 0\text{ V}$		6.5		nC

**SWITCHING OFF**

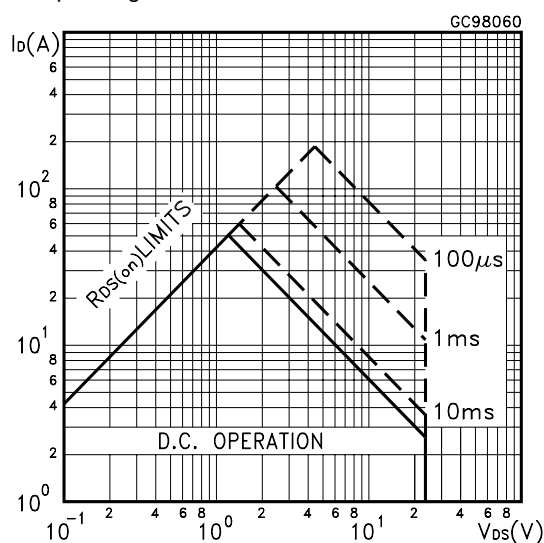
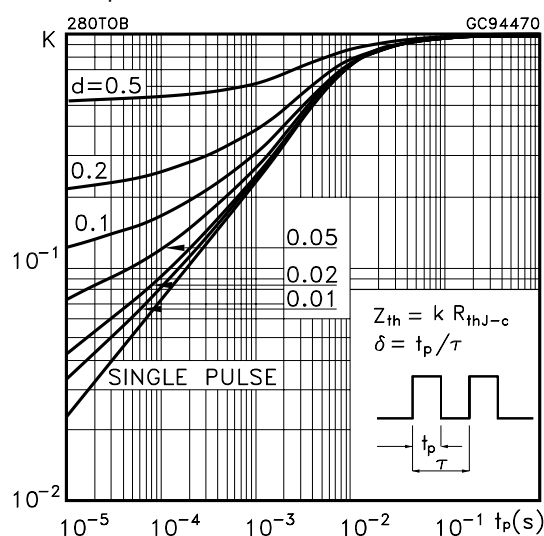
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 10\text{ V}$ $I_D = 25\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		25 12	16	ns ns

**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$	Source-drain Current Source-drain Current (pulsed)				50 200	A A
$V_{SD}^{(4)}$	Forward On Voltage	$I_{SD} = 25\text{ A}$ $V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 50\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 18\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		27 22 1.6		ns nC A

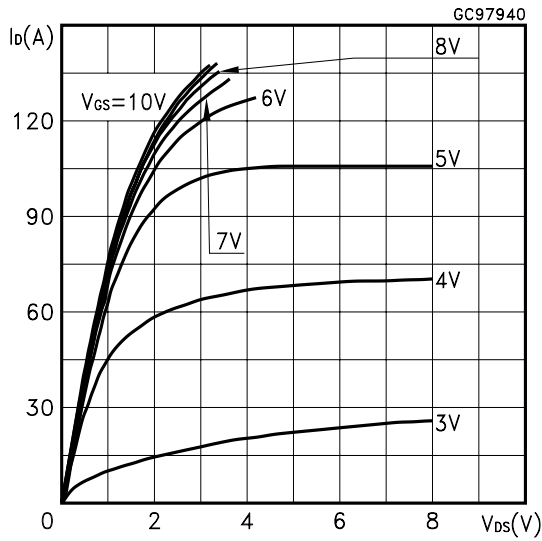
(1) Guaranteed when external  $R_g = 4.7\ \Omega$  and  $t_r < t_{rmax}$ .

(2) Pulse width limited by safe operating area

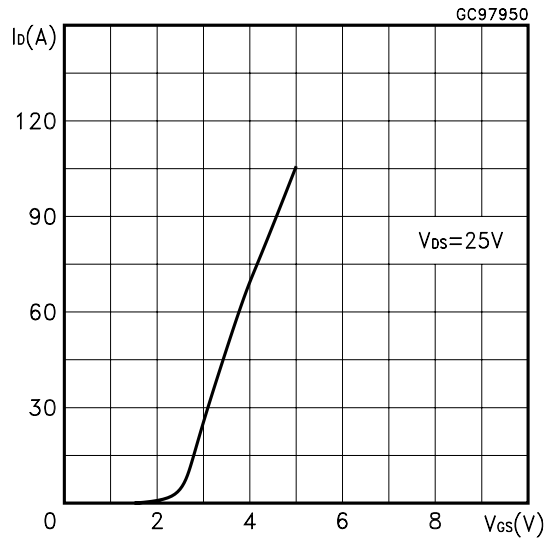
(3) Starting  $T_j = 25^\circ\text{C}$ ,  $I_D = 25\text{ A}$ ,  $V_{DD} = 18\text{ V}$ (4) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.(5)  $Q_{oss} = C_{oss} \cdot \Delta V_{in}$ ,  $C_{oss} = C_{gd} + C_{ds}$ . See Appendix A**Safe Operating Area****Thermal Impedance**

# STB50NH02L

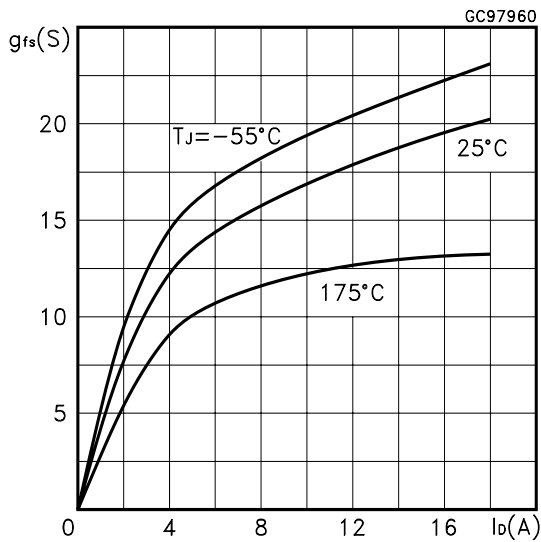
Output Characteristics



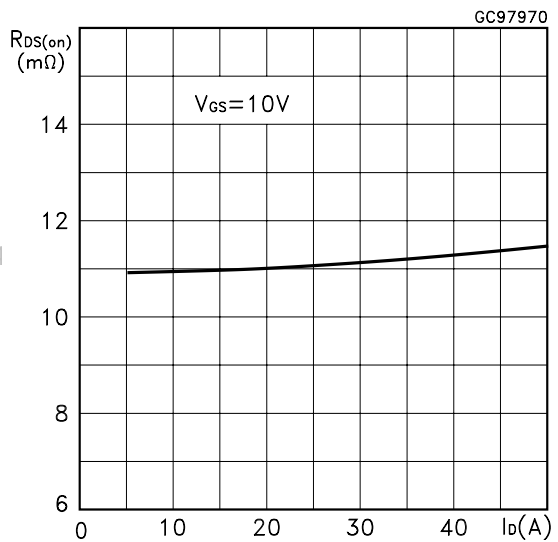
Transfer Characteristics



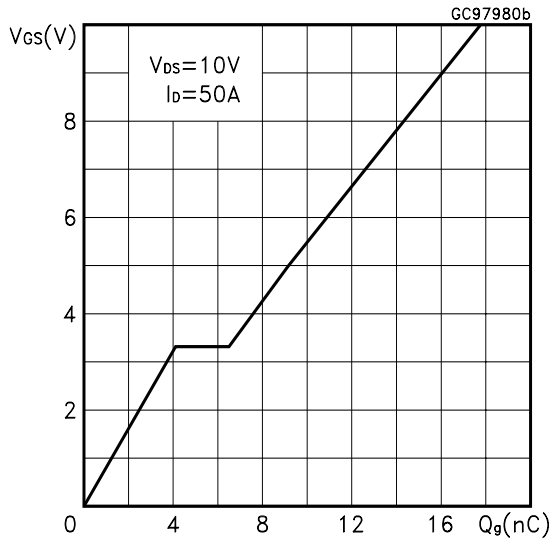
Transconductance



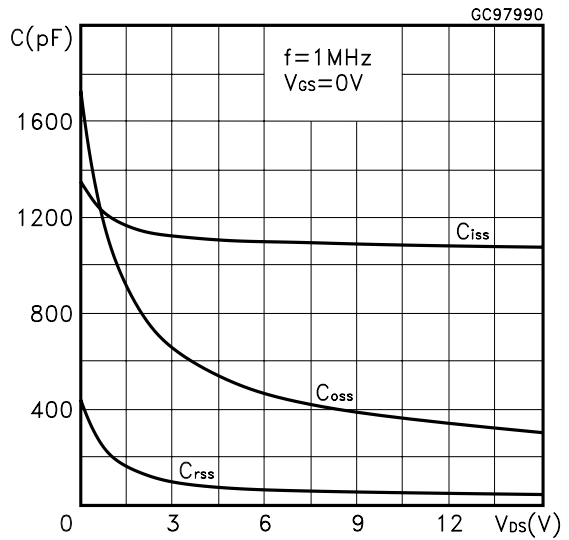
Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage

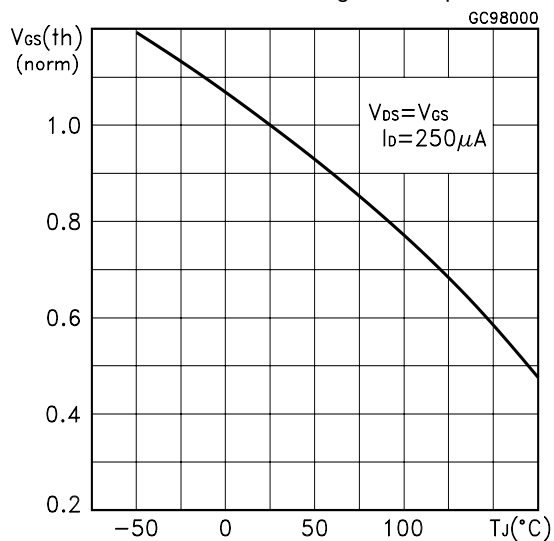


Capacitance Variations

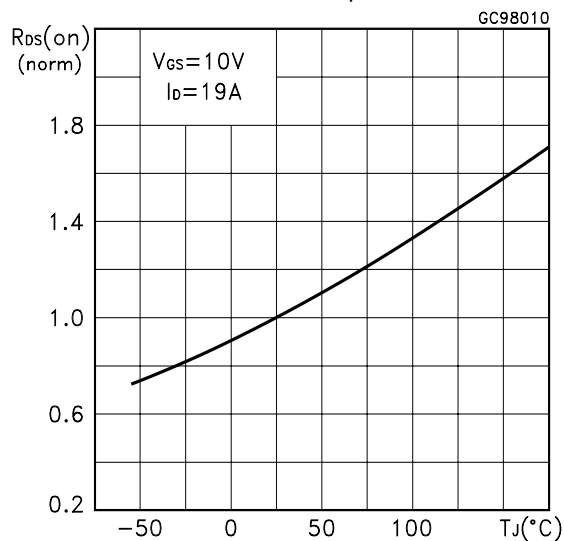


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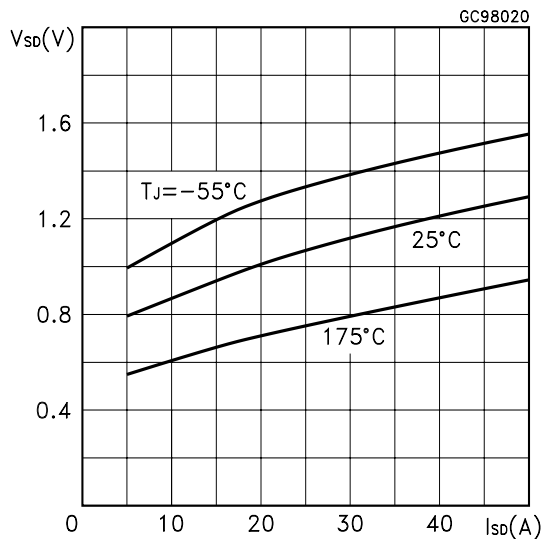
Normalized Gate Threshold Voltage vs Temperature



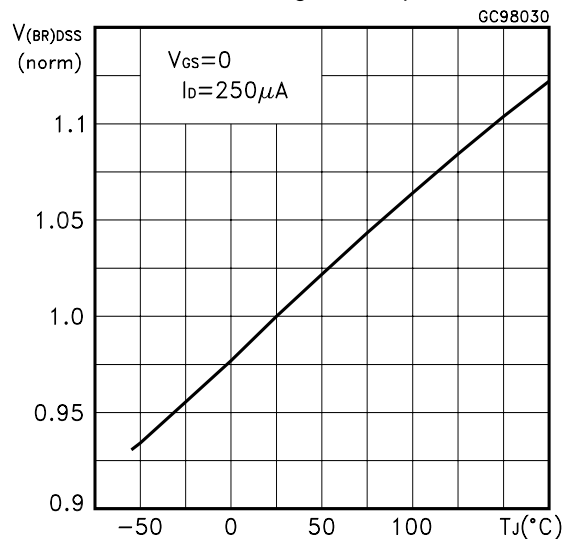
Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics

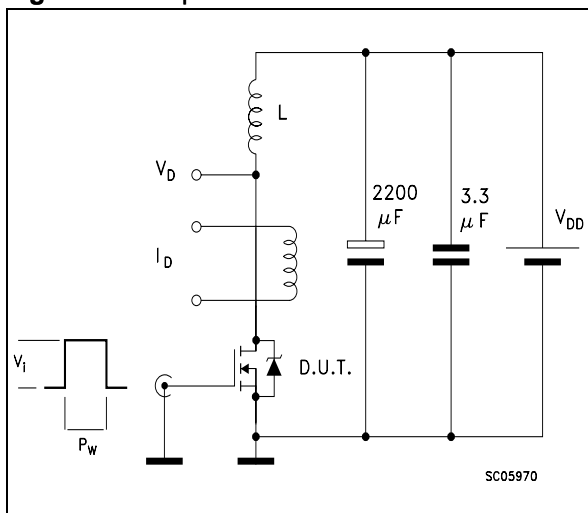


Normalized Breakdown Voltage vs Temperature

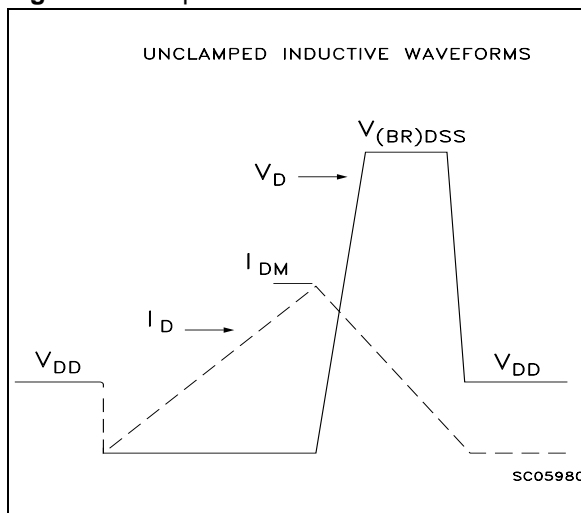


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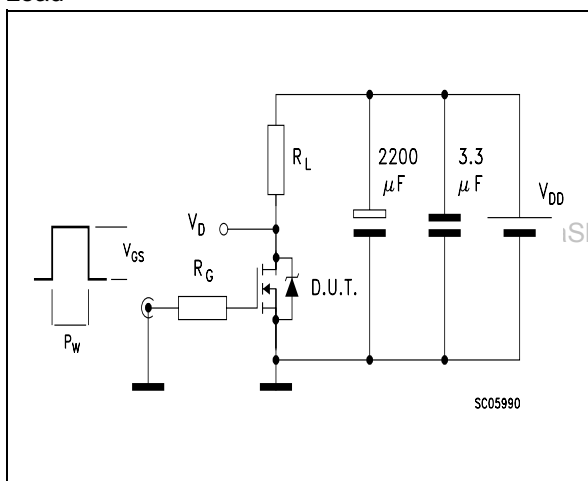
**Fig. 1: Unclamped Inductive Load Test Circuit**



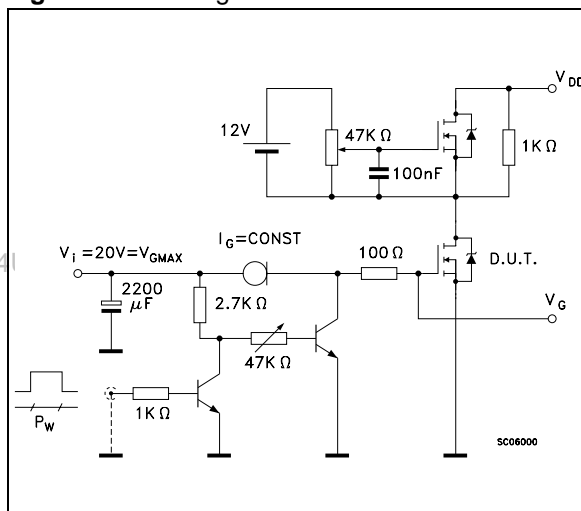
**Fig. 2: Unclamped Inductive Waveform**



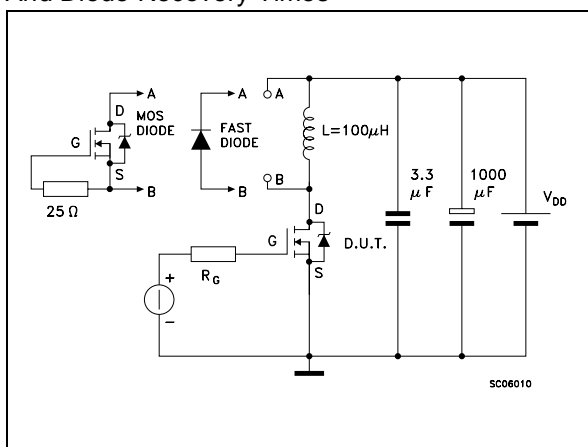
**Fig. 3: Switching Times Test Circuits For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

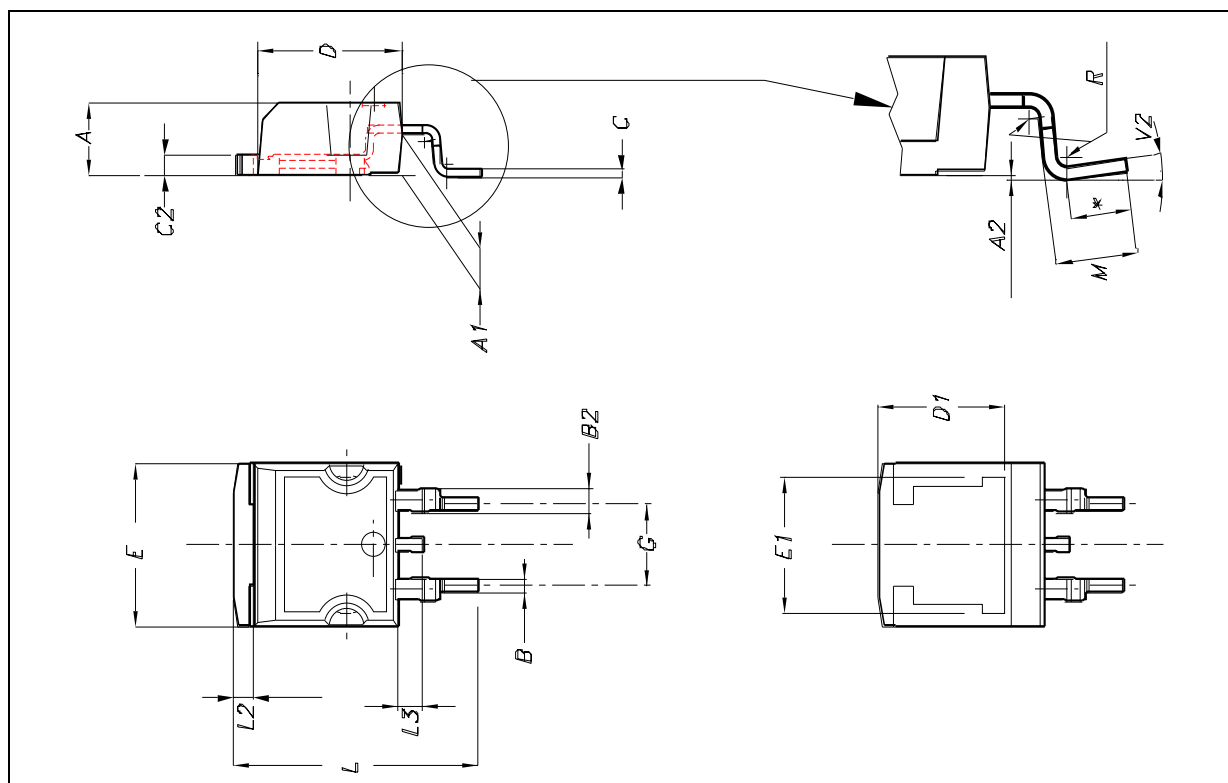


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



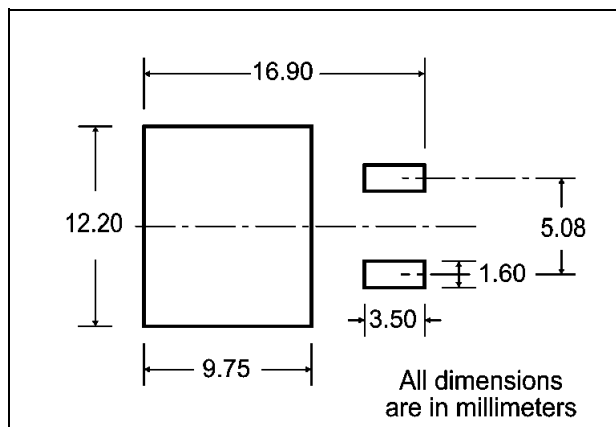
**STB50NH02L****D<sup>2</sup>PAK MECHANICAL DATA**

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
<b>A</b>	4.4		4.6	0.173		0.181
<b>A1</b>	2.49		2.69	0.098		0.106
<b>A2</b>	0.03		0.23	0.001		0.009
<b>B</b>	0.7		0.93	0.028		0.037
<b>B2</b>	1.14		1.7	0.045		0.067
<b>C</b>	0.45		0.6	0.018		0.024
<b>C2</b>	1.21		1.36	0.048		0.054
<b>D</b>	8.95		9.35	0.352		0.368
<b>D1</b>		8			0.315	
<b>E</b>	10		10.4	0.394		0.409
<b>E1</b>		8.5			0.334	
<b>G</b>	4.88		5.28	0.192		0.208
<b>L</b>	15		15.85	0.591		0.624
<b>L2</b>	1.27		1.4	0.050		0.055
<b>L3</b>	1.4		1.75	0.055		0.069
<b>M</b>	2.4		3.2	0.094		0.126
<b>R</b>		0.4			0.015	
<b>V2</b>	0°		4°	0°		4°

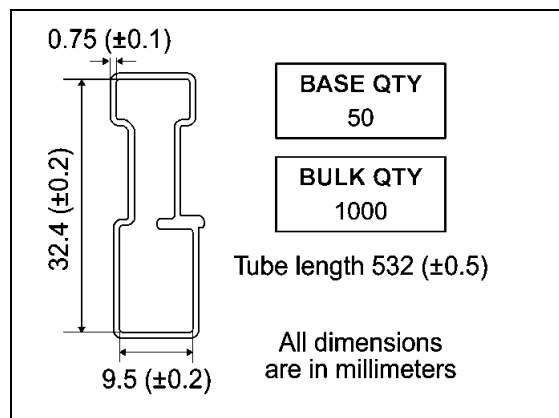


# STB50NH02L

## D2PAK FOOTPRINT



## TUBE SHIPMENT (no suffix)\*



## TAPE AND REEL SHIPMENT (suffix "T4")\*

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

Dimensions: A, B, C, D, G, N, T

G measured at hub

### REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

### TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

TOP COVER TAPE

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

FEED DIRECTION

Bending radius R min.

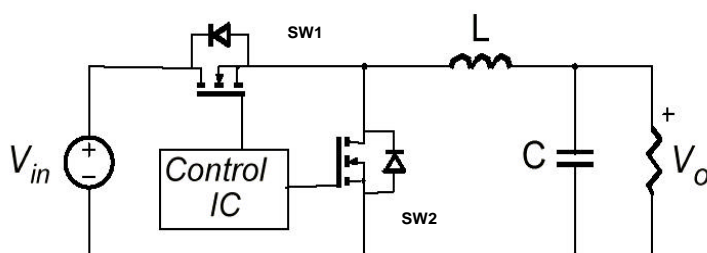
\* on sales type





## APPENDIX A

### Buck Converter: Power Losses Estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low  $R_{DS(on)}$  to reduce conduction losses
- Small  $Q_{gls}$  to reduce the gate charge losses
- Small  $C_{oss}$  to reduce losses due to output capacitance
- Small  $Q_{rr}$  to reduce losses on SW<sub>1</sub> during its turn-on
- The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{gg}$  ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small  $R_g$  and  $L_s$  to allow higher gate current peak and to limit the voltage feedback on the gate
- Small  $Q_g$  to have a faster commutation and to reduce gate charge losses
- Low  $R_{DS(on)}$  to reduce the conduction losses.

**STB50NH02L**

		<b>High Side Switch (SW1)</b>	<b>Low Side Switch (SW2)</b>
<b>P<sub>conduction</sub></b>		$R_{DS(on)SW1} * I_L^2 * d$	$R_{DS(on)SW2} * I_L^2 * (1-d)$
<b>P<sub>switching</sub></b>		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
<b>P<sub>diode</sub></b>	Recovery	Not Applicable	$^1 V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
<b>P<sub>gate(Q<sub>G</sub>)</sub></b>		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
<b>P<sub>Qoss</sub></b>		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

<b>Parameter</b>	<b>Meaning</b>
<b>d</b>	Duty-cycle
<b>Q<sub>gsth</sub></b>	Post threshold gate charge
<b>Q<sub>gls</sub></b>	Third quadrant gate charge
<b>P<sub>conduction</sub></b>	On state losses
<b>P<sub>switching</sub></b>	On-off transition losses
<b>P<sub>diode</sub></b>	Conduction and reverse recovery diode losses
<b>P<sub>gate</sub></b>	Gate drive losses
<b>P<sub>Qoss</sub></b>	Output capacitance losses

<sup>1</sup> Dissipated by SW1 during turn-on

## STB50NH02L

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