300mA SmartOR^{TM} Regulator with V$_{AUX}$ Switch

Features

- Automatic detection of V$_{CC}$ input supply
- Glitch-free output during supply transitions
- Built-in hysteresis during supply selection
- 300mA output maximum load current
- Overload current protection
- Short circuit current protection
- Operates from either V$_{CC}$ or V$_{OUT}$
- 8-pin SOIC package
- Lead-free version available

Applications

- PCI adapter cards
- Network Interface Cards (NICs)
- Dual power systems
- Systems with standby capabilities

Product Description

The SmartOR^{TM} CMPWR130 is a low dropout regulator that delivers up to 300mA of load current at a fixed 3.3V output. An internal threshold level (TYP 4.1V) is used to prevent the regulator from being operated below dropout voltage. The device continuously monitors the input supply and will automatically disable the regulator when V$_{CC}$ falls below the threshold level. When the regulator is disabled, the DRIVE control signal (Active Low) is enabled, which allows an external PMOS switch to power the load from an auxiliary 3.3V supply.

When V$_{CC}$ is restored to a level above the select threshold, the control signal for the external PMOS switch is disabled and the regulator is once again enabled.

All the necessary control circuitry needed to provide a smooth and automatic transition between the supplies has been incorporated. This allows V$_{CC}$ to be dynamically switched without loss of output voltage.

The CMPWR130 is housed in a 8-pin SOIC package and is available with optional lead-free finishing.
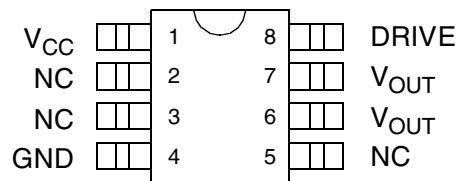
Typical Application Circuit
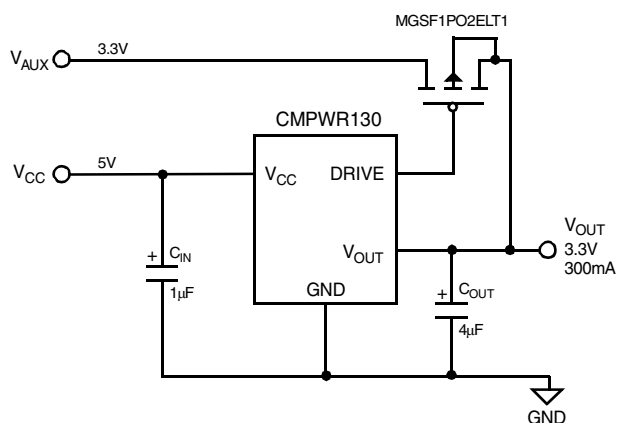
Simplified Electrical Schematic
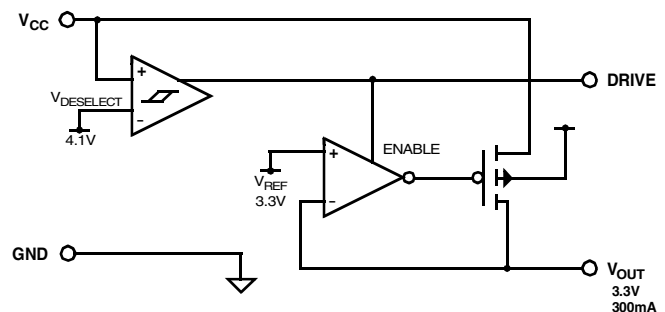
PACKAGE / PINOUT DIAGRAM

TOP VIEW

V_{CC} 1   8   DRIVE
NC   2   7 V_{OUT}
NC   3   6 V_{OUT}
GND   4   5   NC

8-pin SOIC

Note: This drawing is not to scale.

PIN DESCRIPTIONS

PIN(S)	NAME	DESCRIPTION
1	V_{CC}	V_{CC} is the power source for the internal regulator and is monitored continuously by an internal controller circuit. Whenever V_{CC} exceeds V_{CCSEL} (4.30V TYP), the internal regulator (300mA MAX) will be enabled and deliver a fixed 3.3V at V_{OUT}. When V_{CC} falls below V_{CCDES} (4.10V TYP) the regulator will be disabled. Internal loading on this pin is typically 0.6mA when the regulator is enabled, which reduces to 0.2mA whenever the regulator is disabled. If V_{CC} falls below the voltage on the V_{OUT} pin the V_{CC} loading will further reduce to only a few microamperes. During a V_{CC} power up sequence, there will be an effective step increase in V_{CC} line current when the regulator is enabled. The amplitude of this step increase will depend on the dc load current and any necessary current required for charging/discharging the load capacitance. This line current transient will cause a voltage disturbance at the V_{CC} pin. The magnitude of the disturbance will be directly proportional to the effective power supply source impedance being delivered to the V_{CC} input. To prevent chatter during Select and Deselect transitions, a built-in hysteresis voltage of 200mV has been incorporated. It is recommended that the power supply connected to the V_{CC} input should have a source resistance of less than 0.25Ω to minimize the event of chatter during the enabling/disabling of the regulator. An input filter capacitor in close proximity to the V_{CC} pin will reduce the effective source impedance and help minimize any disturbances. If the V_{CC} pin is within a few inches of the main input filter, a capacitor may not be necessary. Otherwise an input filter capacitor in the range of 1µF to 10µF will ensure adequate filtering.
2 - 3, 5	NC	NC pins are electrically isolated from the internal circuitry. These pins can be connected to any external voltage level without impacting the device functionality.
4	GND	GND is the negative reference for all voltages. The current that flows in the ground connection is very low (typically 550µA) and has minimal variation over all load conditions.
6 - 7	V_{OUT}	V_{OUT} is the regulator output voltage connection used to power the load. An output capacitor of 4.7µF is used to provide the necessary phase compensation, thereby preventing oscillation. The capacitor also helps to minimize the peak output disturbance during power supply changeover. When V_{CC} falls below V_{OUT}, then V_{OUT} will be used to provide the necessary quiescent current for the internal reference circuits. This ensures excellent start-up characteristics for the regulator.
8	DRIVE	DRIVE is an active LOW logic output intended to be used as the control signal for driving an external PFET whenever the regulator is disabled. This will allow the voltage at V_{OUT} to be powered from an auxiliary supply voltage (3.3V). The DRIVE pin is pulled HIGH to V_{CC} whenever the regulator is enabled, this ensures the auxiliary remains isolated during normal regulator operation. The output current sinking ability of this logic signal is equivalent to a 100Ω resistor. The current sourcing ability is equivalent to a $4k\Omega$ resistor.

Ordering Information

PART NUMBERING INFORMATION					
		Standard FInish		Lead-free Finish	
Pins	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
8	Power SOIC	CMPWR130S	CMPWR130S	CMPWR130R	CMPWR130R

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
ESD Protection (HBM)	±2000	V

Pin Input Voltages
    V_{CC}
    V_{OUT}
    DRIVE
	
	[GND - 0.5] to +6.0
	[GND - 0.5] to +6.0
	[GND - 0.5] to [V_{CC} + 0.5]
		
		V
		V
		V

Storage Temperature Range	-40 to +150	°C

Operating Temperature Range
    Ambient
    Junction
	
	0 to +70
	0 to +125
		
		°C
		°C

Power Dissipation (See Note 1)	0.6	W

Note 1: The power rating is based on a printed circuit board heat spreading capability equivalent to 2 square inches of copper con-
nected to the GND pins. Typical multi-layer boards using power plane construction will provide this heat spreading ability
without the need for additional dedicated copper area. (Please consult with factory for thermal evaluation assistance).

STANDARD OPERATING CONDITIONS		
PARAMETER	VALUE	UNITS
V_{CC}	5.0 $\pm$0.5	V
Ambient Operating Temperature Range	0 to +70	°C
Load Current	0 to 300	mA
C_{EXT}	4.7 $\pm$20%	µF

	ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OUT}	Regulator Output Voltage	$0mA < I_{LOAD} < 300mA$	3.10	3.300	3.50	V
V_{CCSEL}	V_{CC} Select Voltage	Regulator enabled		4.30	4.45	V
V_{CCDES}	V_{CC} Deselect Voltage	Regulator disabled	3.90	4.10		V
V_{CCHYST}	Hysteresis Voltage	See Note 2		0.20		V
I_{SC}	Short Circuit Output Current	$V_{CC} = 5V$, $V_{OUT}= 0V$	310			mA
$V_{R\ LOAD}$	Load Regulation	$V_{CC}=5V$, $30mA \leq I_{LOAD} \leq 300mA$		50		mV
$V_{R\ LINE}$	Line Regulation	$I_{LOAD} = 5mA$; $4.5V \leq V_{CC} \leq to\ 5.5V$		50		mV
I_{RCC}	V_{CC} Pin Reverse Leakage	$V_{OUT} = 3.3V$, $V_{CC} = 0V$		2	50	µA
I_{CC}	Quiescent Supply Current	$V_{CC} > V_{CCSEL}$, $I_{LOAD} = 0mA$		0.60	0.80	mA
		$V_{CCDES} > V_{CC} > V_{OUT}$		0.20		mA
		$V_{OUT} > V_{CC}$		0.01	0.02	mA
I_{GND}	Ground Current (see Note 3)	$V_{CCSEL} > V_{CC}$ (Regulator disabled)		0.20	0.40	mA
		$V_{CC} = 5V$, $I_{LOAD} = 5mA$		0.60	0.80	mA
		$V_{CC} = 5V$, $I_{LOAD} = 300mA$		0.70	1.40	mA
R_{OH}	DRIVE Pull-up Resistance	R_{PULLUP} to V_{CC}, $V_{CC} > V_{CCSEL}$		4.0	8.0	kΩ
R_{OL}	DRIVE Pull-down Resistance	$R_{PULLDOWN}$ to GND, $V_{CCDES} > V_{CC}$		0.1	0.4	kΩ

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.

Note 2: The hysteresis defines the maximum level of acceptable disturbance on V_{CC} during switching. It is recommended that the V_{CC} source impedance be kept below 0.25Ω to ensure the switching disturbance remains below the hysteresis during select/deselect transitions. An input capacitor may be required to help minimize the switching transient.

Note 3: Ground pin current consists of controller current (0.15mA) and regulator current if enabled. The controller always draws 0.15mA from either V_{CC} or V_{OUT}, whichever is greater. All regulator current is supplied exclusively from V_{CC}. At high load currents a small increase occurs due to current limit protection circuitry.

Performance Information

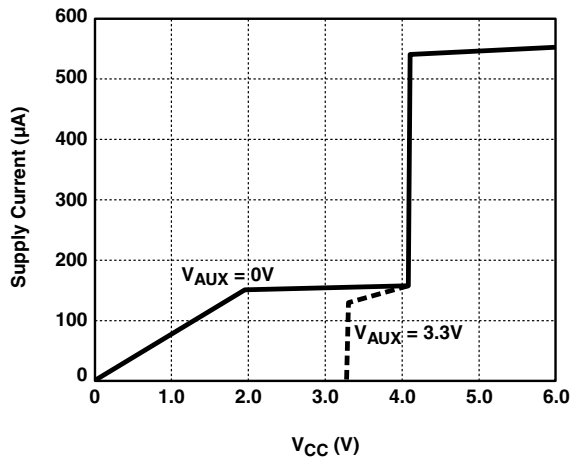**CMPWR130 Typical DC Characteristics (nominal conditions unless specified otherwise)**

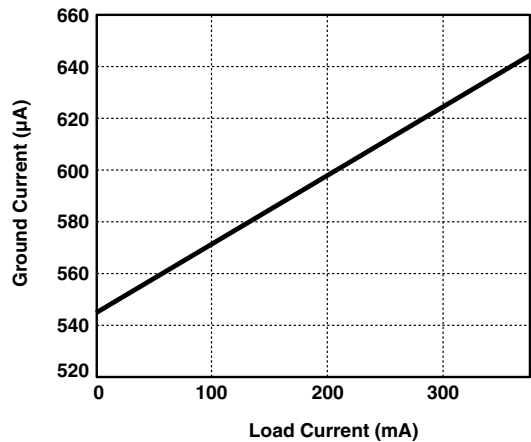Figure 1. Supply Current vs Voltage (V_{AUX} = 3.3V)

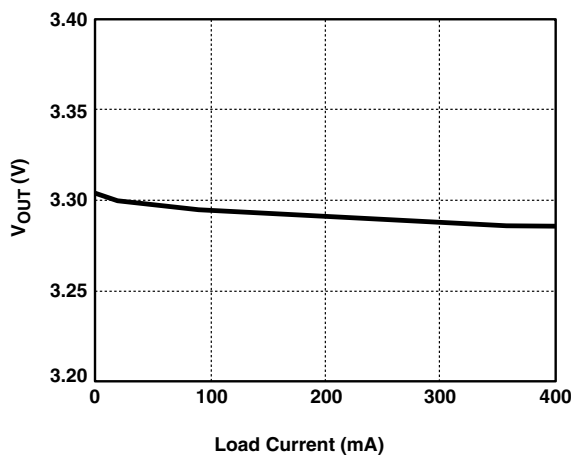Figure 2. Ground Current vs Output Load
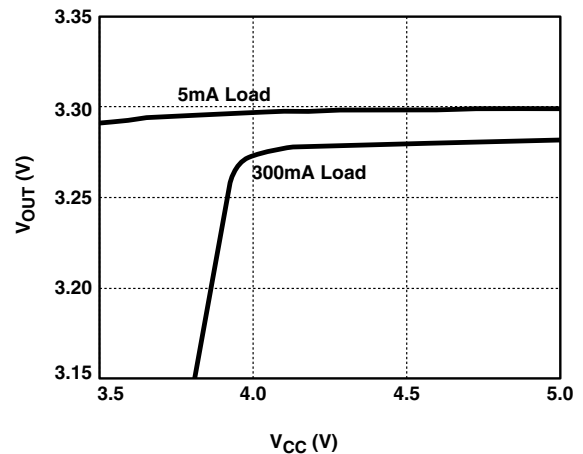
Figure 3. Load Regulation

Figure 4. Line Regulation

Performance Information (cont'd)

CMPWR130 Transient Characteristics (nominal conditions unless specified otherwise)
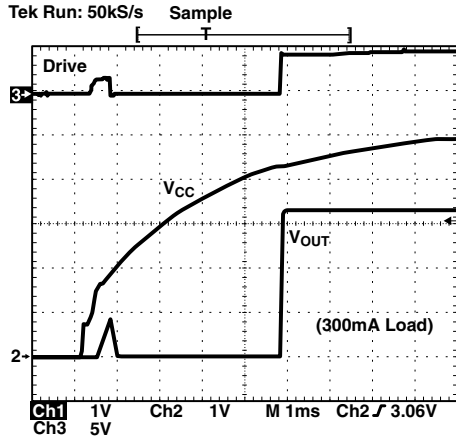(Supply source resistance set to 0.2Ω)
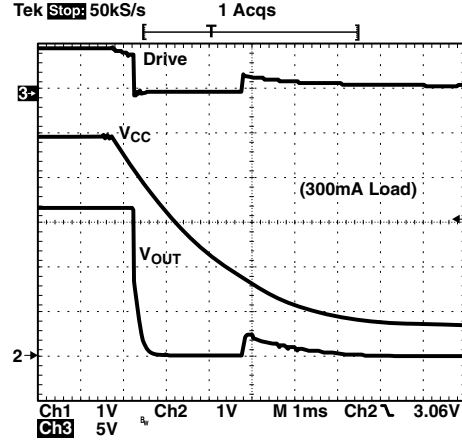
Figure 5. V_{CC} Cold Start Power UP (V_{AUX} = 0V)

Figure 6. V_{CC} Complete Power Down (V_{AUX} = 0V)
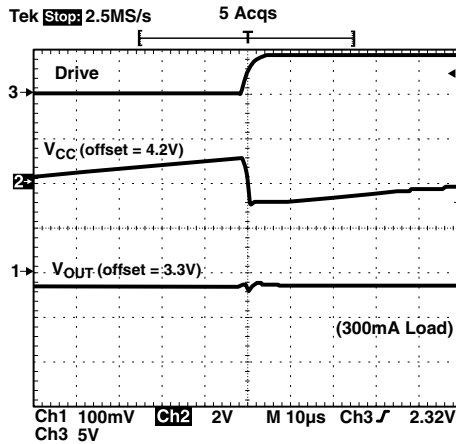
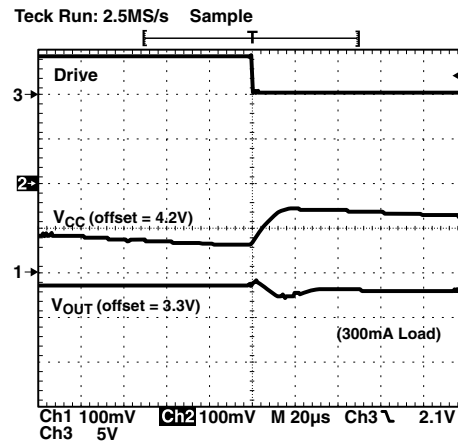**Figure 7. V_{CC} Power UP (V_{AUX} = 3.3V)**

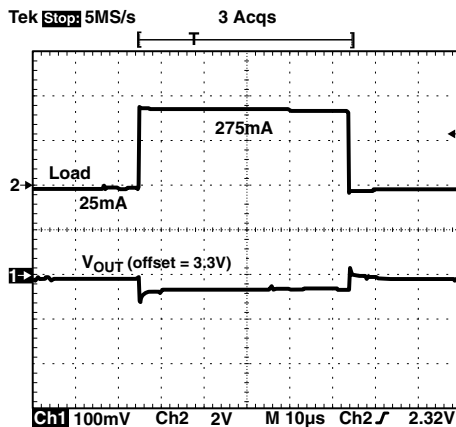**Figure 8. V_{CC} Power Down (V_{AUX} = 3.3V)**

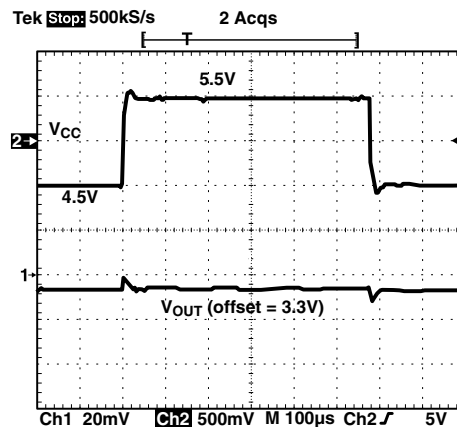**Figure 9. Load Transient (10% to 90%) Step Response**

Figure 10. Line Transient ($1V_{pp}$) Step Response

Performance Information (cont'd)

CMPWR130 Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D \, (\theta_{JC}) + P_D \, (\theta_{CA})$$

$$= T_{AMB} + P_D \, (\theta_{JA})$$

The CMPWR130 uses a standard SOIC package. When this package is mounted on a double-sided printed circuit board with two square inches of copper allocated for "heat spreading", the resulting θ_{JA} is 85°C/W.

Based on a maximum power dissipation of 0.51W (1.7V x 300mA) with an ambient of 70°C, the resulting junction temperature will be:

$$T_{JUNC} = T_{AMB} + P_D \, (\theta_{JA})$$

$$= 70°C + 0.51W \, (85°C/W)$$

$$= 70°C + 43°C = 113°C$$

Thermal characteristics were measured using a double-sided board with two square inches of copper area connected to the GND pin for "heat spreading".

Measurements showing performance up to junction temperature of 125°C were performed under light load conditions (5mA). This allows the ambient temperature to be representative of the internal junction temperature.

Note: The use of multi-layer board construction with separate ground and power planes will further enhance the overall thermal performance. In the event of no copper area being dedicated for heat spreading, a multi-layer board construction, using only the minimum size pad layout, will provide the CMPWR130 with an overall θ_{JA} of 100°C/W which allows up to 550mW to be safely dissipated.
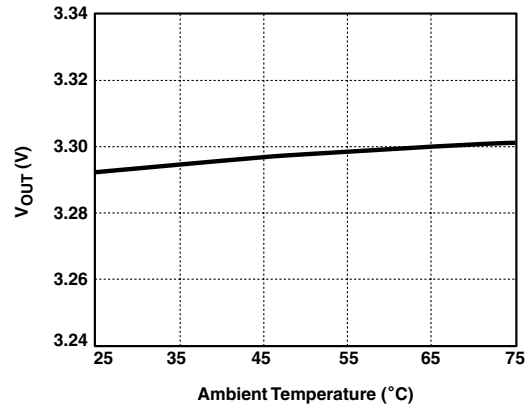
Figure 11. Regulator V_{OUT} vs T_{AMB} (300mA Load)
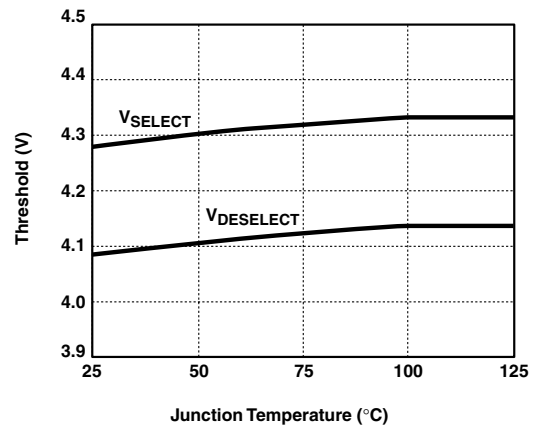
Figure 12. Select and Deselect Threshold vs T_{JUNC}

Mechanical Details
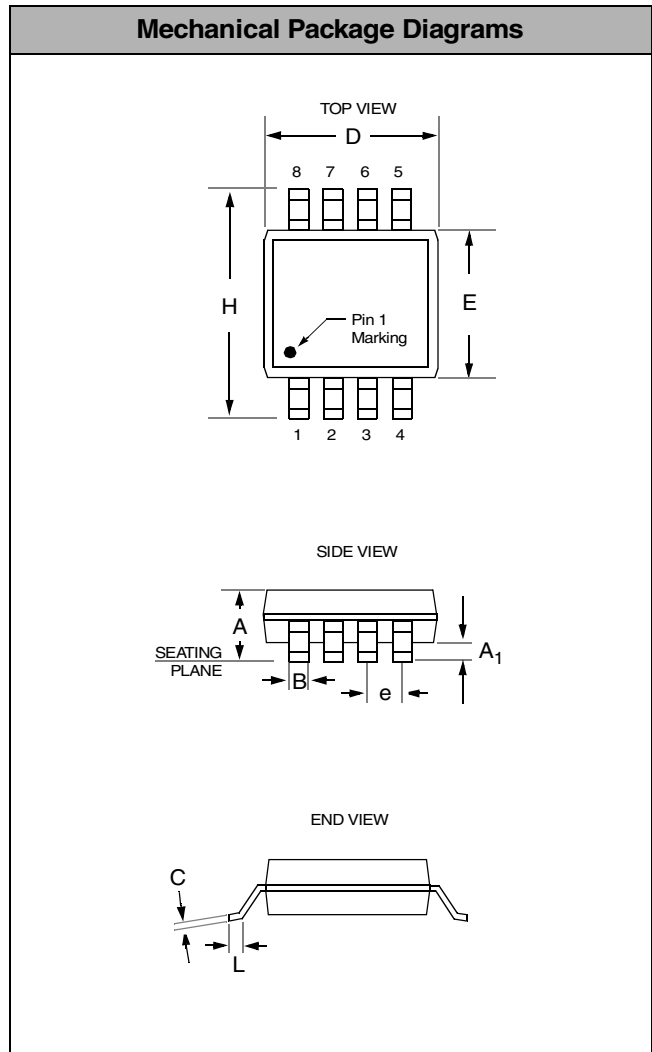
SOIC-8 Mechanical Specifications

Dimensions for CMPWR130 devices packaged in 8-pin SOIC packages are presented below.

For complete information on the SOIC-8 package, see the California Micro Devices SOIC Package Information document.

PACKAGE DIMENSIONS				
Package	SOIC			
Pins	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A$_1$	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.19	0.150	0.165
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

Mechanical Package Diagrams

TOP VIEW

SIDE VIEW

END VIEW

Package Dimensions for SOIC-8