

36Mb DDR SRAM Specification

153BGA with Pb & Pb-Free
(RoHS compliant)

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Document Title

36M DDR SYNCHRONOUS SRAM

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>DraftData</u>	<u>Remark</u>
Rev. 0.0	Initial document.	Nov. 2005	Advance
Rev. 0.1	Change AC Characteristics, Pin Capacitance, DC Characteristics	Apr. 2006	Preliminary
Rev. 0.2	Change Samsung JEDEC Code in ID REGISTER DEFINITION	Jun. 2006	Preliminary
Rev. 1.0	Correct Typo	Aug. 2006	Final

FEATURES

- 1Mx36 or 2Mx18 Organizations.
- 1.8~2.5V V_{DD}/1.5V ~1.8V_{DDQ}.
- HSTL Input and Outputs.
- Single Differential HSTL Clock.
- Synchronous Pipeline Mode of Operation with Self-Timed Late Write.
- Free Running Active High and Active Low Echo Clock Output Pin.
- Registered Addresses, Burst Control and Data Inputs.
- Registered Outputs.
- Double and Single Data Rate Burst Read and Write.
- Burst Count Controllable With Max Burst Length of 4
- Interleaved and Linear Burst mode support
- Bypass Operation Support
- Programmable Impedance Output Drivers.
- JTAG Boundary Scan (subset of IEEE std. 1149.1)
- 153(9x17) Ball Grid Array Package(14mmx22mm)
- No Output enable support.

GENERAL DESCRIPTION

The K7D323674C and K7D321874C are 37,748,736 bit Synchronous Pipeline Burst Mode SRAM devices. They are organized as 1,048,576 words by 36 bits for K7D323674C and 2,097,152 words by 18 bits for K7D321874C, fabricated using Samsung's advanced CMOS technology.

Single differential HSTL level clock, K and $\bar{K}$ are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses and burst control inputs are registered internally. Data inputs are registered one cycle after write addresses are asserted(Late Write), at the rising edge of K clock for single data rate (SDR) write operations and at rising and falling edge of K clock for a double data rate (DDR) write operations.

Data outputs are updated from output registers off the rising edges of K clock for SDR read operations and off the rising and falling edges of K clock for DDR read operations. Free running echo clocks are supported which are representative of data output access time for all SDR and DDR operations.

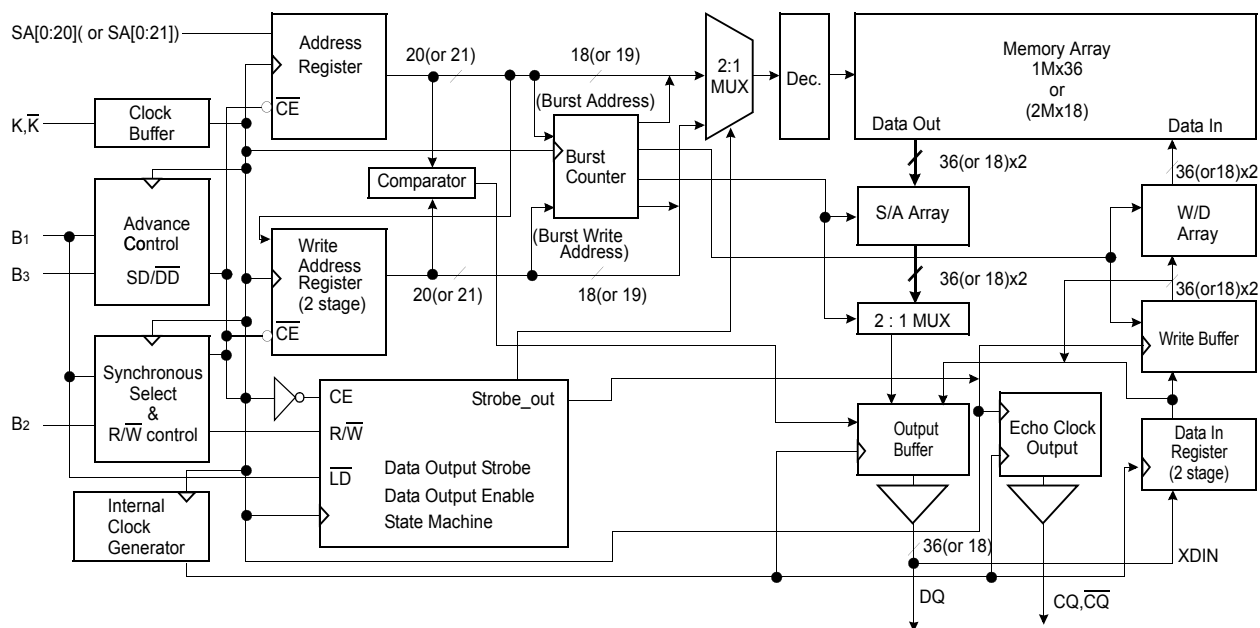
The chip is operated with 1.8~2.5V power supply and is compatible with HSTL input and output. The package is 9x17(153) Ball Grid Array balls on a 1.27mm pitch.

ORDERING INFORMATION

Organization	Maximum Frequency	Part Number
1Mx36	400MHz	K7D323674C-H(G)'C40
	375MHz	K7D323674C-H(G)'C37
	333MHz	K7D323674C-H(G)'C33
2Mx18	400MHz	K7D321874C-H(G)'C40
	375MHz	K7D321874C-H(G)'C37
	333MHz	K7D321874C-H(G)'C33

Note 1. H(G) [Package type] : G-Pb Free, H-Pb

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\bar{K}$	Differential Clocks	TCK	JTAG Test Clock
SA	Synchronous Address Input	TMS	JTAG Test Mode Select
SA0, SA1	Synchronous Burst Address Input (SA0 = LSB)	TDI	JTAG Test Data Input
DQ	Synchronous Data I/O	TDO	JTAG Test Data Output
CQ, $\bar{CQ}$	Differential Output Echo Clocks	VREF	HSTL Input Reference Voltage
B1	Load External Address	VDD	Power Supply
B2	Burst R/W Enable	VDDQ	Output Power Supply
B3	Single/Double Data Selection	VSS	GND
$\bar{LBO}$	Linear Burst Order	NC	No Connection
ZQ	Output Driver Impedance Control Input		

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7D323674C(1Mx36)

	1	2	3	4	5	6	7	8	9
A	Vss	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	Vss
B	DQ	DQ	SA	Vss	B1	Vss	SA	DQ	DQ
C	Vss	VDDQ	SA	SA	SA	SA	SA	VDDQ	Vss
D	DQ	DQ	SA	Vss(5)	VDD	Vss(6)	SA	DQ	DQ
E	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
F	DQ	CQ	DQ	VDD	VDD	VDD	DQ	CQ	DQ
G	Vss	VDDQ	Vss	Vss	K	Vss	Vss	VDDQ	Vss
H	DQ	DQ	DQ	VDD	$\overline{K}$	VDD	DQ	DQ	DQ
J	Vss	VDDQ	Vss	VDD	VDD	VDD	Vss	VDDQ	Vss
K	DQ	DQ	DQ	Vss	B2	Vss	DQ	DQ	DQ
L	Vss	VDDQ	Vss	$\overline{LBO}$	B3	MODE(7)	Vss	VDDQ	Vss
M	DQ	$\overline{CQ}$	DQ	VDD	VDD	VDD	DQ	$\overline{CQ}$	DQ
N	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
P	DQ	DQ	NC*	Vss	VDD(2)	Vss	SA	DQ	DQ
R	Vss	VDDQ	VDD(4)	SA	SA1	SA	VDD(3)	VDDQ	Vss
T	DQ	DQ	SA	Vss	SA0	Vss	SA	DQ	DQ
U	Vss	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	Vss

K7D321874C(2Mx18)

	1	2	3	4	5	6	7	8	9
A	Vss	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	Vss
B	NC	DQ	SA	Vss	B1	Vss	SA	NC	DQ
C	Vss	VDDQ	SA	SA	SA	SA	SA	VDDQ	Vss
D	DQ	NC	SA	Vss(5)	VDD	Vss(6)	SA	DQ	NC
E	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
F	NC	CQ	NC	VDD	VDD	VDD	DQ	NC	DQ
G	Vss	VDDQ	Vss	Vss	K	Vss	Vss	VDDQ	Vss
H	DQ	NC	DQ	VDD	$\overline{K}$	VDD	NC	DQ	NC
J	Vss	VDDQ	Vss	VDD	VDD	VDD	Vss	VDDQ	Vss
K	NC	DQ	NC	Vss	B2	Vss	DQ	NC	DQ
L	Vss	VDDQ	Vss	$\overline{LBO}$	B3	MODE(7)	Vss	VDDQ	Vss
M	DQ	NC	DQ	VDD	VDD	VDD	NC	$\overline{CQ}$	NC
N	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
P	NC	DQ	SA	Vss	VDD(2)	Vss	SA	NC	DQ
R	Vss	VDDQ	VDD(4)	SA	SA1	SA	VDD(3)	VDDQ	Vss
T	DQ	NC	SA	Vss	SA0	Vss	SA	DQ	NC
U	Vss	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	Vss

- (1) Variable address see "Variable address assignment table"
(2) Variable address see "Variable address assignment table"
(3) Variable address see "Variable address assignment table"
(4) Variable address see "Variable address assignment table"
(5) Variable address see "Variable address assignment table"
(6) Variable address see "Variable address assignment table"
(7) Internally NC

VARIABLE ADDRESS ASSIGNMENT TABLE

Density	Ball 5C (1)	Ball 5P (2)	Ball 7R (3)	Ball 3R (4)	Ball 4D (5)	Ball 6D (6)
32 Mb	SA	V _{DD}	V _{DD}	V _{DD}	V _{SS}	V _{SS}
64 Mb	SA	SA	V _{DD}	V _{DD}	V _{SS}	V _{SS}
144 Mb	NC	SA	SA	SA	V _{SS}	V _{SS}
288 Mb	SA	SA	SA	SA	V _{SS}	V _{SS}
576 Mb	NC	SA	SA	SA	SA	SA
1152 Mb	SA	SA	SA	SA	SA	SA

NOTE : - SRAM density definition beyond 144Mb will include the parity bits.

Read Operation(Single and Double)

During SDR read operations, addresses and controls are registered at the first rising edge of K clock and then the internal array is read between first and second rising edges of K clock. Data outputs are updated from output registers off the second rising edge of K clock. During DDR read operations, addresses and controls are registered at the first rising edge of K clock, and then the internal array is read twice between first and second rising edges of K clock. Data outputs are updated from output registers sequentially by burst order off the second rising and falling edge of K clock.

Interleave and linear burst operation is controlled by LBO pin and the burst count is controllable with the maximum burst length of 4. To avoid data contention, at least two NOP operations are required between the last read and the first write operation.

Write Operation(Late Write)

During SDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered at the following rising edge of K clock. During DDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered twice at the following rising and falling edge of K clock. Write addresses and data inputs are stored in the data in registers until the next write operation, and only at the next write operation are data inputs fully written into SRAM array.

Echo clock operation

Free running type of Echo clocks are generated from K clock regardless of read, write and NOP operations. They will stop operation only when K clock is in the stop mode.

Echo clocks are designed to represent data output access time and this allows the echo clocks to be used as reference to capture data outputs.

Bypass Read Operation

Bypass read operation occurs when the last write operation is followed by a read operation where write and read addresses are identical. For this case, data outputs are from the data in registers instead of SRAM array.

Programmable Impedance Output Driver

This HSTL Late Write SRAM has been designed with programmable impedance output buffers. The SRAMs output buffer impedance can be adjusted to match the system data bus impedance, by connecting an external resistor (RQ) between the ZQ pin of the SRAM and Vss. The value of RQ must be five times the value of the intended line impedance driven by the SRAM. For example, a 250Ω resistor will give an output buffer impedance of 50Ω. The allowable range of RQ is from 175Ω to 350Ω. Internal circuits evaluate and periodically adjust the output buffer impedance, as the impedance is affected by drifts in supply voltage and temperature. One evaluation occurs every 32 clock cycles, with each evaluation moving the output buffer impedance level only one step at a time toward the optimum level. Impedance updates occur when the SRAM is in High-Z state, and thus are triggered by write and deselect operations. Updates will also be triggered with G HIGH initiated High-Z state, providing the specified G setup and hold times are met. Impedance match is not instantaneous upon power-up. In order to guarantee optimum output driver impedance, the SRAM requires a minimum number of non-read cycles (1,024) after power-up. The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to Vss or VDDQ.

Power-Up/Power-Down Supply Voltage Sequencing

The following power-up supply voltage application is recommended: Vss, VDD, VDDQ, VREF, then VIN. VDD and VDDQ can be applied simultaneously, as long as VDDQ does not exceed VDD by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: VIN, VREF, VDDQ, VDD, Vss. VDD and VDDQ can be removed simultaneously, as long as VDDQ does not exceed VDD by more than 0.5V during power-down.

TRUTH TABLE

K	B1	B2	B3	DQ	Operation
↑	H	L	X	Hi-Z	No Operation, Pipeline High-Z
↑	L	H	H	DOUT	Load Address, Single Read
↑	L	H	L	DOUT	Load Address, Double Read
↑	L	L	H	DIN	Load Address, Single Write
↑	L	L	L	DIN	Load Address, Double Write
↑	H	H	X	B	Increment Address, Continue

NOTE : - B(Both) is DIN in write cycle and DOUT in read cycle. Byte write function is not supported. X means "Don't Care".
- K & $\bar{K}$ are complementary.

OUTPUT TRISTATE TRUTH TABLE

K	Operation	DQ (n)	DQ (n+1)
↑	Write (B2=L)	X	High-Z
↑	Deselect (NOP) (B1=H, B2=L)	X	High-Z

BURST SEQUENCE TABLE

4 Burst Operation for Interleaved Burst ($\overline{LBO} = V_{DDQ}$)

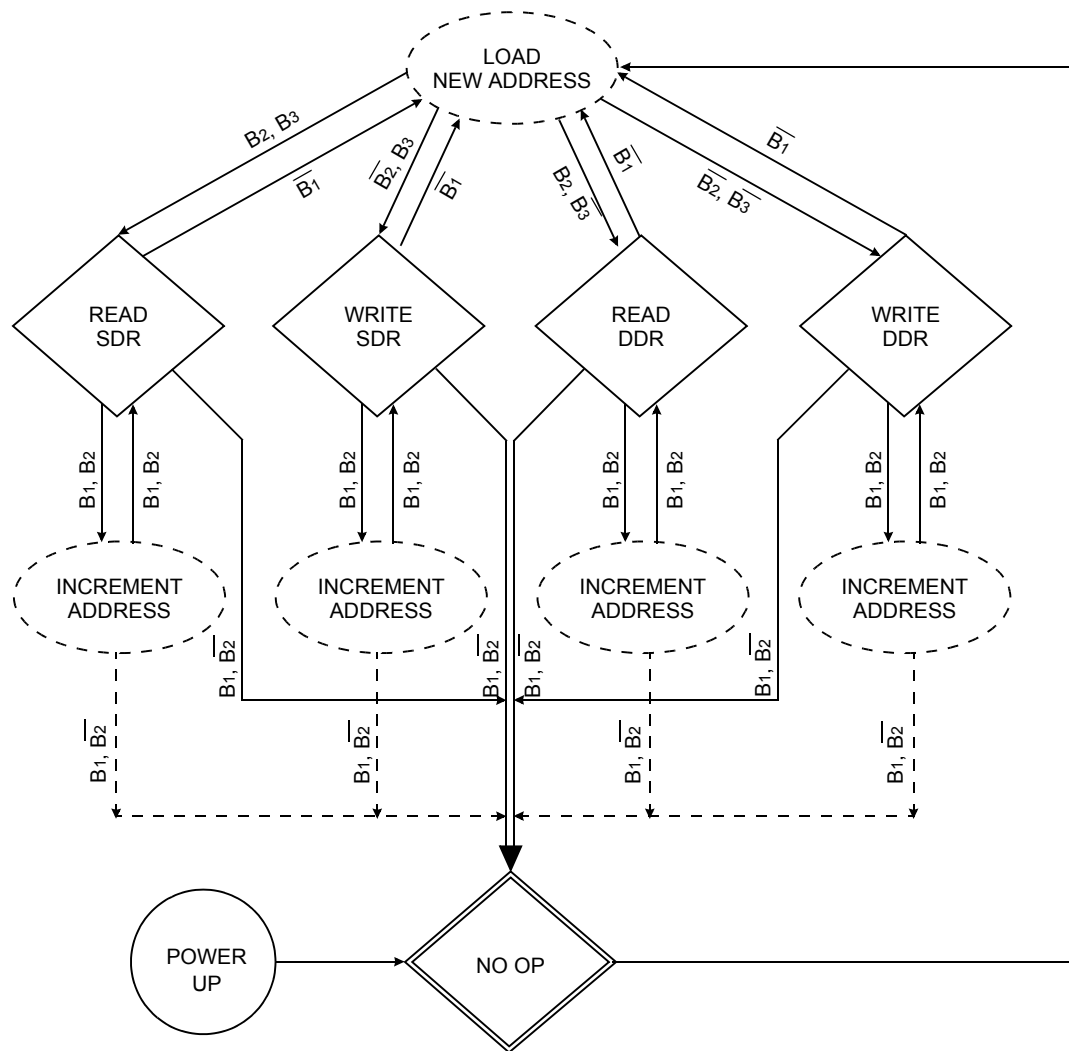
Interleaved Burst Mode	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

NOTE : - For Interleave Burst $\overline{LBO} = V_{DDQ}$ is recommended. If $\overline{LBO} = V_{DD}$, it must not exceed 2.63V.

4 Burst Operation for Linear Burst ($\overline{LBO} = V_{SS}$)

Linear Burst Mode	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

BUS CYCLE STATE DIAGRAM



NOTE :

1. State transitions ; $\overline{B_1}$ =(Load Address), B_1 =(Increment Address, Continue)
 B_2 =(Read), $\overline{B_2}$ =(Write)
 B_3 =(Single Data Rate), $\overline{B_3}$ =(Double Data Rate)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	VDD	-0.5 to 3.13	V
Output Supply Voltage Relative to Vss	VDDQ	-0.5 to 2.3	V
Voltage on any pin Relative to Vss	VIN	-0.5 to VDDQ+0.5 (2.3V MAX)	V
Output Short-Circuit Current(per I/O)	IOUT	25	mA
Storage Temperature	TSTR	-55 to 125	°C
Maximum Junction Temperature	TJ	110	°C
Maximum Power Dissipation	Pd	3.0	W

NOTE : Power Dissipation Capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	VDD	1.7	2.5	2.6	V	
Output Power Supply Voltage	VDDQ	1.4	1.5	1.9	V	
Input High Level Voltage	VIH	VREF+0.1	-	VDDQ+0.3	V	1, 2
Input Low Level Voltage	VIL	-0.3	-	VREF-0.1	V	1, 3
Input Reference Voltage	VREF	0.68	0.75	1.0	V	

NOTE :1. These are DC test criteria. DC design criteria is VREF±50mV. The AC VIH/VIL levels are defined separately for measuring timing parameters.

2. VIH (Max)DC=VDDQ+0.3, VIH (Max)AC=2.6V (2.1V for DQs) (pulse width ≤ 20% of cycle time).
3. VIL (Min)DC=-0.3V, VIL (Min)AC=-1.0V (-0.5V for DQs) (pulse width ≤ 20% of cycle time).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current(x36) (Cycle time = tKHKH min)	IDD40 IDD37 IDD33	-	700 650 600	mA	1,2
Average Power Supply Operating Current(x18) (Cycle time = tKHKH min)	IDD40 IDD37 IDD33	-	650 600 550	mA	1,2
Stop Clock Standby Current (VIN=VDD-0.2V or 0.2V fixed, K=Low, K̄=High)	ISB1	-	300	mA	1
Input Leakage Current (VIN=Vss or VDDQ)	ILI	-3	3	μA	
Output Leakage Current (VOUT=Vss or VDDQ)	ILO	-5	5	μA	
Output High Voltage(Programmable Impedance Mode)	VOH1	VDDQ/2	VDDQ	V	3
Output Low Voltage(Programmable Impedance Mode)	VOL1	Vss	VDDQ/2	V	4
Output High Voltage(IoH=-0.1mA)	VOH2	VDDQ-0.2	VDDQ	V	
Output Low Voltage(IoL=0.1mA)	VOL2	Vss	0.2	V	

NOTE :1. Minimum cycle. Iout=0mA.

2. 50% read cycles.
3. |IoH|=(VDDQ/2)/(RQ/5)±15% @VOH=VDDQ/2 for 175Ω ≤ RQ ≤ 300Ω.
4. |IoL|=(VDDQ/2)/(RQ/5)±15% @VOL=VDDQ/2 for 175Ω ≤ RQ ≤ 300Ω.

PIN CAPACITANCE

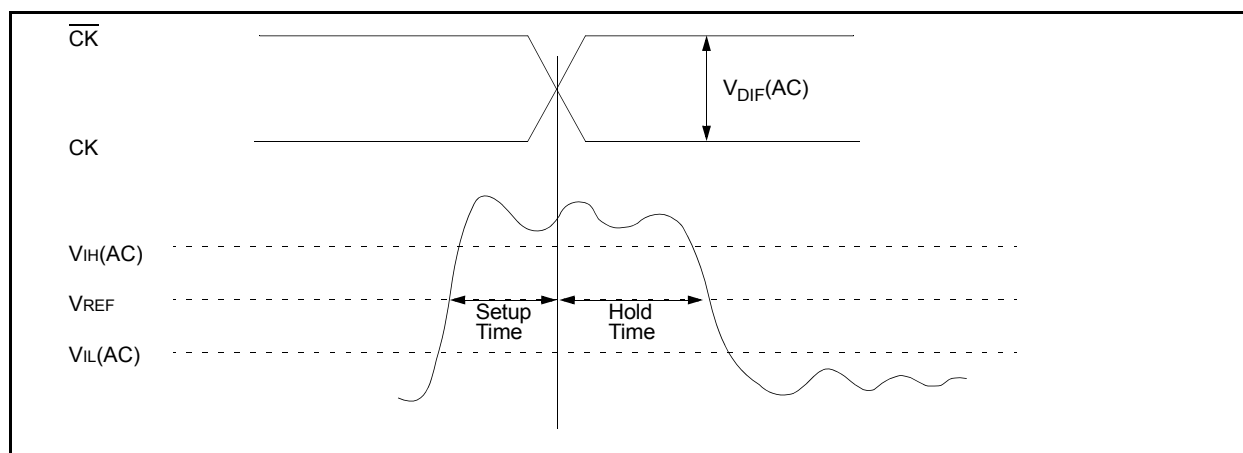
Parameter	Symbol	Test Condition	TYP	Max	Unit
Input Capacitance	C _{IN}	V _{IN} =0V	-	4	pF
Data Output Capacitance	C _{OUT}	V _{OUT} =0V	-	5	pF

NOTE : Periodically sampled and not 100% tested.(T_A=25°C, f=500MHz)

AC INPUT CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
AC Input Logic High	V _{IH} (AC)	V _{REF} + 0.4		V	-
AC Input Logic Low	V _{IL} (AC)		V _{REF} - 0.4	V	-
Clock Input Differential Voltage	V _{DIF} (AC)	0.8		V	-
V _{REF} Peak-to-Peak AC Voltage	V _{REF} (AC)		5% V _{REF} (DC)	V	-

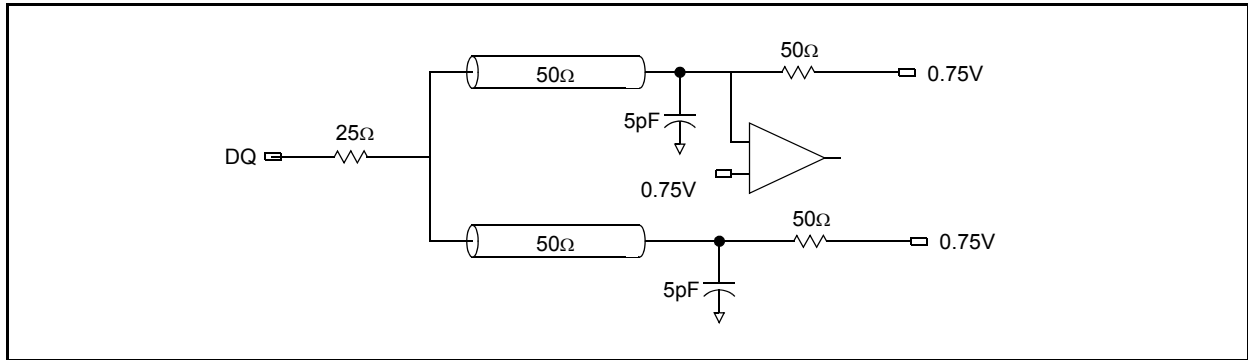
AC INPUT DEFINITION



AC TEST CONDITIONS (T_A=0 to 70°C, V_{DD}=2.37 -2.63V, V_{DDQ}=1.5V)

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	1.25/0.25	V	-
Input Reference Level	V _{REF}	0.75	V	-
Input Rise/Fall Time	T _R /T _F	0.5/0.5	ns	-
Output Timing Reference Level		0.75	V	-
Clock Input Timing Reference Level		Cross Point	V	-
Output Load		See Below		-

AC TEST OUTPUT LOAD

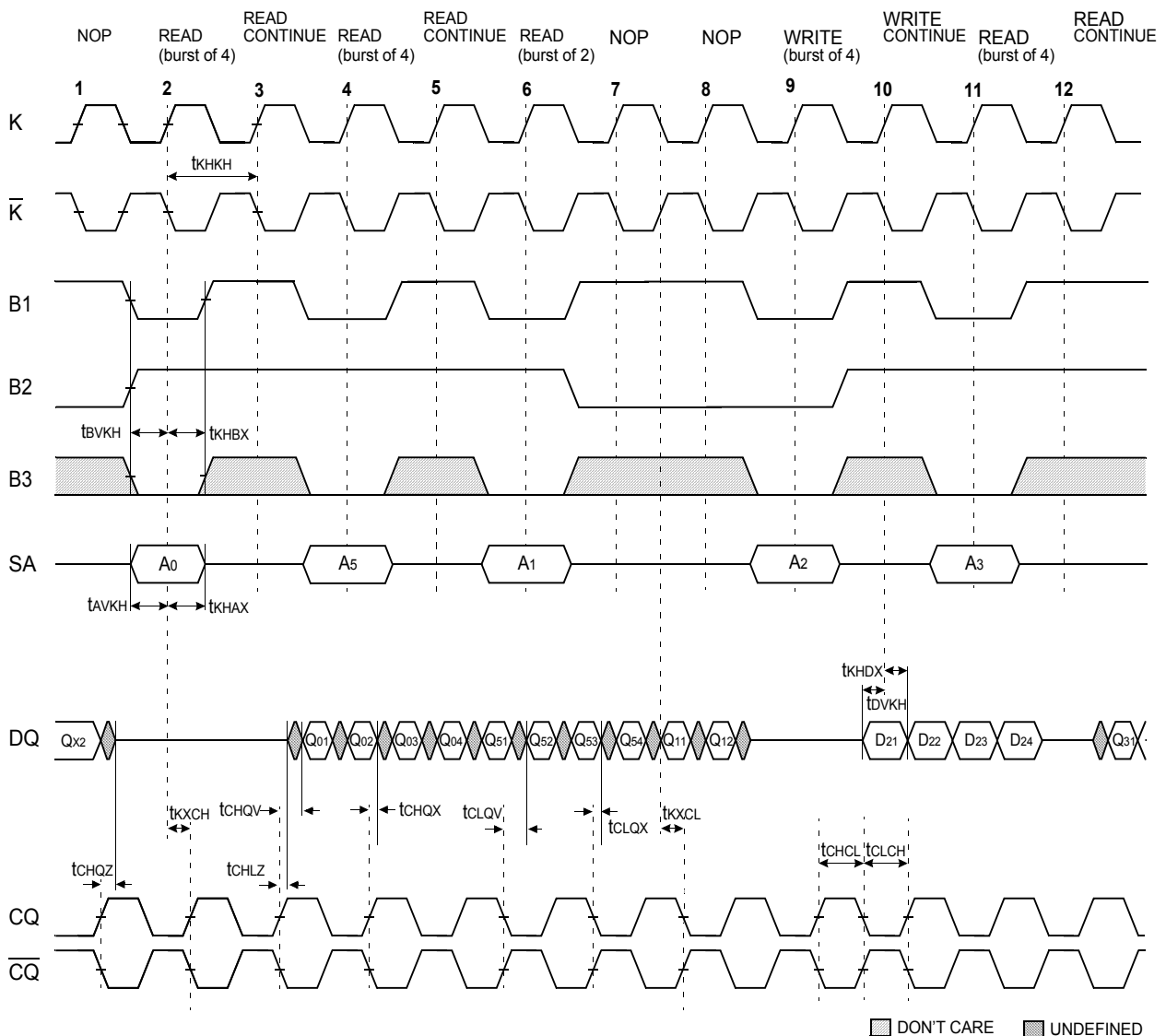


AC TIMING CHARACTERISTICS

PARAMETER	SYMBOL	-40		-37		-33		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Clock									
Clock Cycle Time	tkHKH	2.50		2.67		3.00		ns	1
Clock High Pulse Width	tkHKL	1.15		1.25		1.40		ns	
Clock Low Pulse Width	tkLKH	1.15		1.25		1.40		ns	
Setup Times									
Address Setup Time	tAVKH	0.30		0.33		0.35		ns	
Control(B1,B2,B3) Setup Time	tBVKH	0.30		0.33		0.35		ns	
Data Setup Time	tDVKX	0.20		0.25		0.30		ns	2
Hold Times									
Address Hold Time	tkHAX	0.30		0.33		0.35		ns	
Control(B1,B2,B3) Hold Time	tkHBX	0.30		0.33		0.35		ns	
Data Hold Time	tkXDX	0.20		0.25		0.30		ns	2
Output Times									
Echo Clock High Pulse Width	tCHCL	tkHKL-0.1	tkHKL+0.1	tkHKL-0.1	tkHKL+0.1	tkHKL-0.1	tkHKL+0.1	ns	2
Echo Clock Low Pulse Width	tCLCH	tkLKH-0.1	tkLKH+0.1	tkLKH-0.1	tkLKH+0.1	tkLKH-0.1	tkLKH+0.1	ns	2
Clock Crossing to Echo Clock	tkXCH	1.0	2.5	1.0	2.5	1.0	2.5	ns	3
Clock Crossing to Echo Clock	tkXCL	1.0	2.5	1.0	2.5	1.0	2.5	ns	3
Echo Clock High to Output Valid	tkHQV		0.20		0.20		0.20	ns	
Echo Clock Low to Output Valid	tCLQV		0.20		0.20		0.20	ns	
Echo Clock High to Output Hold	tCHQX	-0.20		-0.20		-0.20		ns	
Echo Clock Low to Output Hold	tCLQX	-0.20		-0.20		-0.20		ns	
Echo Clock High to Output High-Z	tCHQZ		0.20		0.20		0.20	ns	
Echo Clock High to Output Low-Z	tCHLZ	-0.20		-0.20		-0.20		ns	

Notes: 1. The maximum cycle time must be limited to guarantee AC timing specification.
2. This parameter is guaranteed by design, and may not be tested at values shown in the table.
3. This parameter refers to CQ and CQ rising and falling edges.
4. K and K Clocks must be used differentially to meet AC timing specifications.

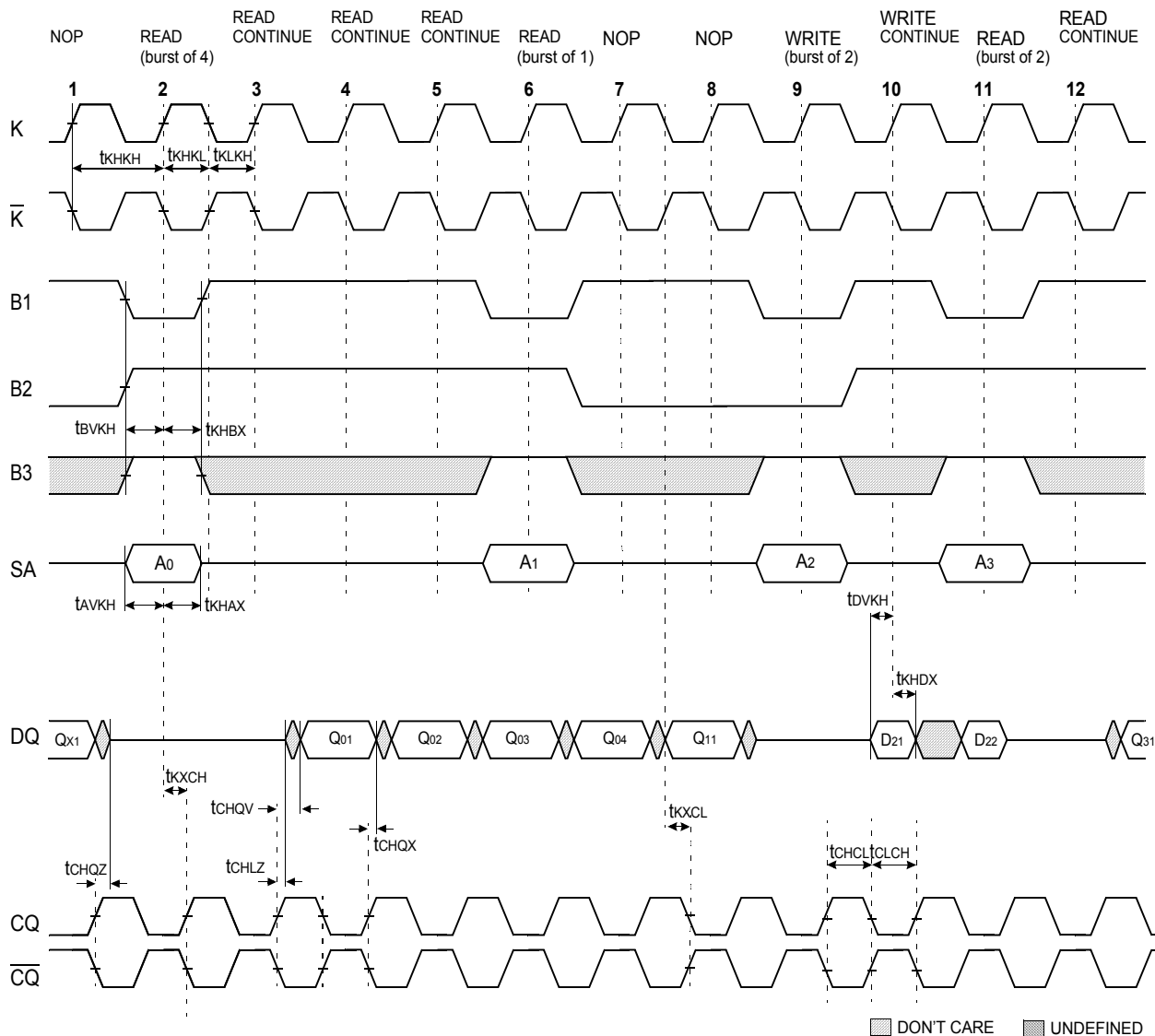
**TIMING WAVEFORMS FOR DOUBLE DATA RATE CYCLES
(Burst Length=4, 2)**



NOTE

1. Q₀₁ refers to output from address A. Q₀₂ refers to output from the next internal burst address following A, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. Doing more than one Read Continue or Write Continue will cause the address to wrap around.

TIMING WAVEFORMS FOR SINGLE DATA RATE CYCLES
(Burst Length=4, 2, 1)



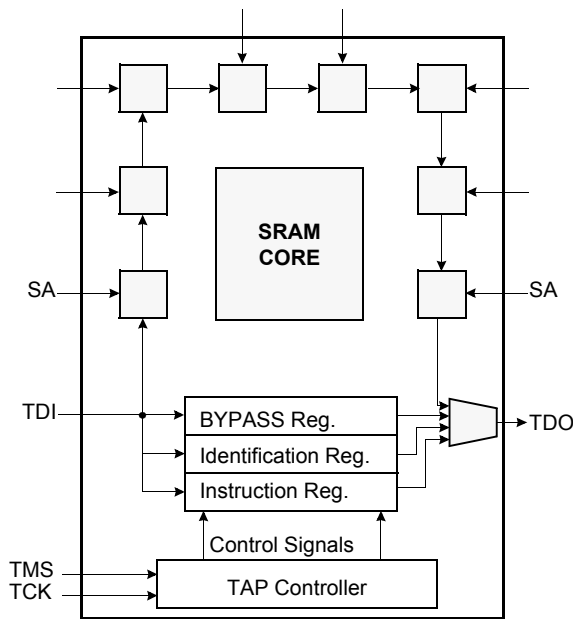
NOTE :

1. Q₀₁ refers to output from address A₀. Q₀₂ refers to output from the next internal burst address following A₀, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. This device supports cycle lengths of 1, 2, 4. Continue(B1=HIGH, B2=HIGH, B3=X) up to three times following a B1 operation. Any further Continue assertions constitute invalid operations.
4. This device will have an address wraparound if further Continues are applied.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

The SRAM provides a limited set of IEEE standard 1149.1 JTAG functions. This is to test the connectivity during manufacturing between SRAM, printed circuit board and other components. Internal data is not driven out of SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and therefore can be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



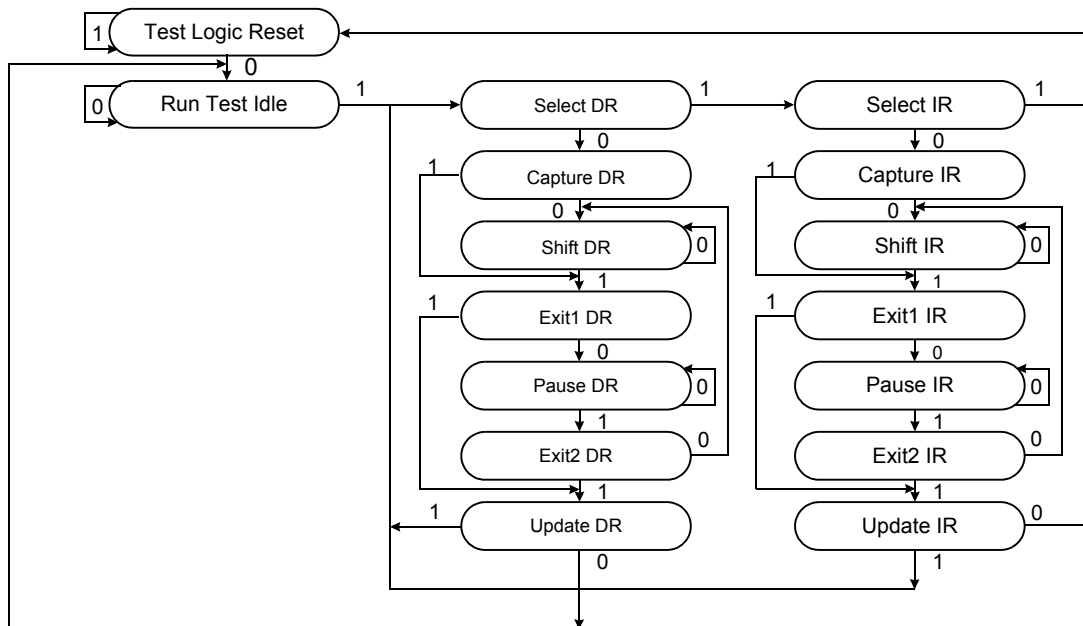
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	PRIVATE3	Bypass Register	3,5
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	PRIVATE2	Bypass Register	3,5
1	1	0	PRIVATE1	Bypass Register	3,5
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. Input terminators are switched off.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked.
The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.
5. PRIVATE1 and PRIVATE2 are reserved for the exclusive use of SAM-SUNG. This instruction should not be used.

TAP Controller State Diagram



BOUNDARY SCAN EXIT ORDER(x36)

1	5P	VDD(2)		38	5C	SA
2	5R	SA1		39	4A	SA
3	5T	SA0		40	4C	SA
4	6R	SA		41	4D	Vss(2)
5	7T	SA		42	3A	SA
6	7R	VDD(2)		43	3B	SA
7	7P	SA		44	3C	SA
8	8T	DQ1		45	3D	SA
9	9T	DQ2		46	2B	DQ19
10	8P	DQ10		47	1B	DQ20
11	7M	DQ0		48	2D	DQ28
12	9P	DQ12		49	3F	DQ18
13	8M	$\overline{\text{CQ}}(3)$		50	1D	DQ30
14	9M	DQ3		51	2F	CQ(3)
15	7K	DQ9		52	1F	DQ21
16	8K	DQ11		53	3H	DQ27
17	9K	DQ13		54	2H	DQ29
18	6L	MODE		55	1H	DQ31
19	5H	$\overline{\text{K}}$		56	5A	ZQ(1)
20	5G	K		57	5B	B1
21	9H	DQ4		58	5K	B2
22	8H	DQ6		59	5L	B3
23	7H	DQ8		60	4L	$\overline{\text{LBO}}$
24	9F	DQ14		61	1K	DQ22
25	8F	CQ(3)		62	2K	DQ24
26	9D	DQ5		63	3K	DQ26
27	7F	DQ17		64	1M	DQ32
28	8D	DQ7		65	2M	$\overline{\text{CQ}}(3)$
29	9B	DQ15		66	1P	DQ23
30	8B	DQ16		67	3M	DQ35
31	7D	SA		68	2P	DQ25
32	7C	SA		69	1T	DQ33
33	7B	SA		70	2T	DQ34
34	7A	SA		71	3R	VDD(2)
35	6D	Vss(2)		72	3T	SA
36	6C	SA		73	4R	SA
37	6A	SA		74	7U	NC

* Reserved for Mode Pin

BOUNDARY SCAN EXIT ORDER(x18)

1	5P	VDD(2)		28	5C	SA
2	5R	SA1		29	4A	SA
3	5T	SA0		30	4C	SA
4	6R	SA		31	4D	Vss(2)
5	7T	SA		32	3A	SA
6	7R	VDD(2)		33	3B	SA
7	7P	SA		34	3C	SA
8	8T	DQ1		35	3D	SA
				36	2B	DQ10
9	9P	DQ2				
10	8M	$\overline{\text{CQ}}(3)$		37	1D	DQ11
				38	2F	CQ(3)
11	7K	DQ0				
				39	3H	DQ9
12	9K	DQ3				
13	6L	MODE		40	1H	DQ12
14	5H	$\overline{\text{K}}$		41	5A	ZQ(1)
15	5G	K		42	5B	B1
				43	5K	B2
16	8H	DQ6		44	5L	B3
				45	4L	$\overline{\text{LBO}}$
17	9F	DQ4				
				46	2K	DQ15
18	7F	DQ8		47	1M	DQ13
19	8D	DQ7				
20	9B	DQ5				
				48	3M	DQ17
21	7D	SA		49	2P	DQ16
22	7C	SA		50	1T	DQ14
23	7B	SA		51	3P	SA
24	7A	SA		52	3R	VDD(2)
25	6D	Vss(2)		53	3T	SA
26	6C	SA		54	4R	SA
27	6A	SA		55	7U	NC

* Reserved for Mode Pin

NOTE :

1. This pin is place holder for higher density. TDO will be low for Vss and high for VDD

SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1M x 36	3 bits	1 bits	32 bits	74 bits
2M x 18	3 bits	1 bits	32 bits	55 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit (0)
1M x 36	0000	01000 00100	XXXXXX	00011001110	1
2M x 18	0000	01001 00011	XXXXXX	00011001110	1

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	1.7	2.5	2.6	V	
Input High Level	V _{IH}	0.65*V _{DD}	-	V _{DD} +0.3	V	
Input Low Level	V _{IL}	-0.3	-	0.35*V _{DD}	V	
Output High Voltage(I _{OH} =-2mA)	V _{OH}	0.75*V _{DD}	-	V _{DD}	V	
Output Low Voltage(I _{OL} =2mA)	V _{OL}	V _{SS}	-	0.25*V _{DD}	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

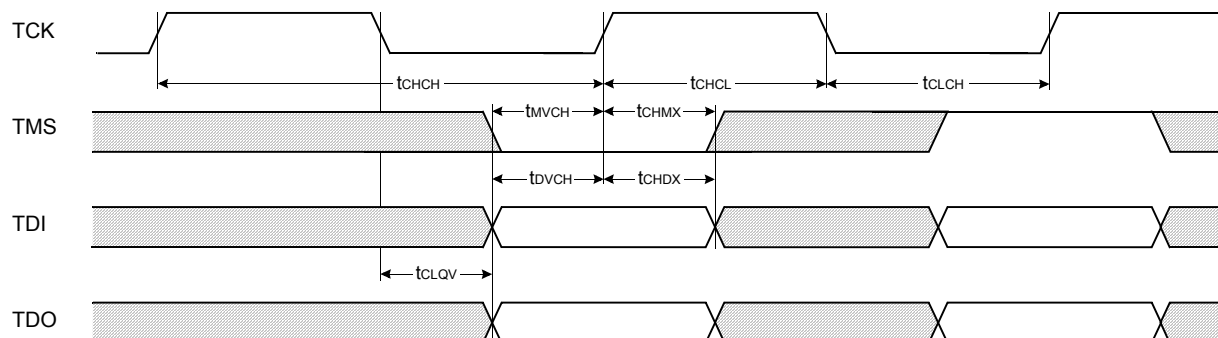
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	V _{DD} /0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		V _{DD} /2	V	1

NOTE : 1. See SRAM AC test output load on page 5.

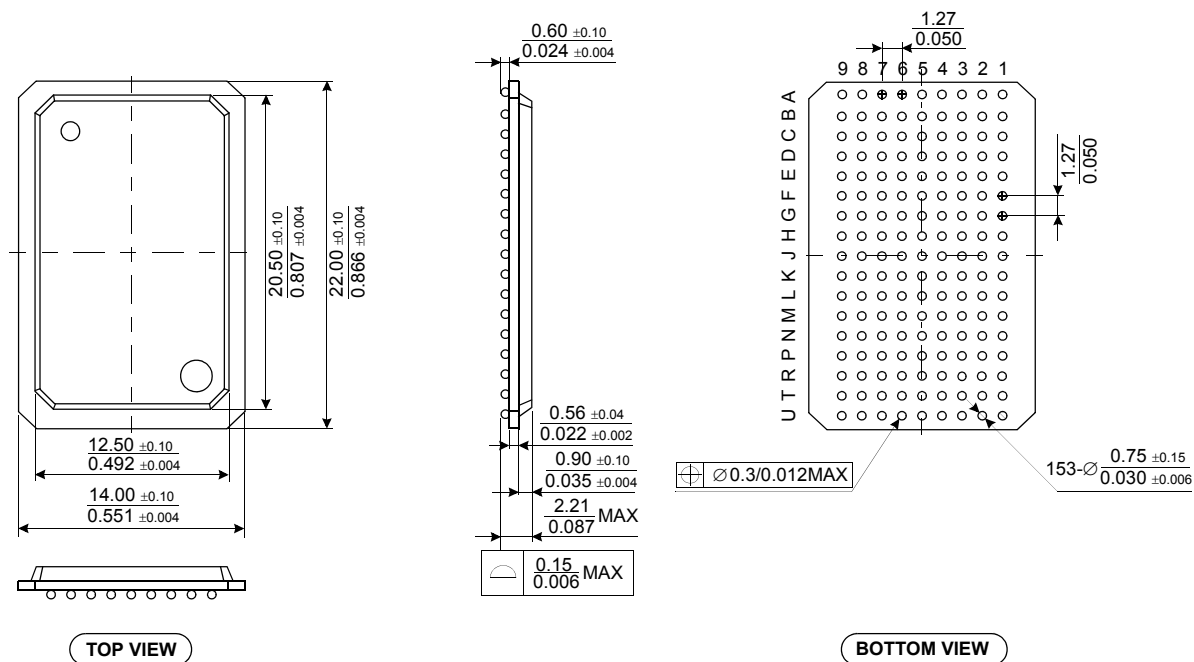
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{dvCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



153 BGA PACKAGE DIMENSIONS



NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCS Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

153 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Thermal Resistance	Unit	Note
Junction to Ambient(at still air)	Theta_JA	19.5	°C/W	
Junction to Case	Theta_JC	0.9	°C/W	
Junction to Board	Theta_JB	6.9	°C/W	

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times \text{Theta_JA}$.