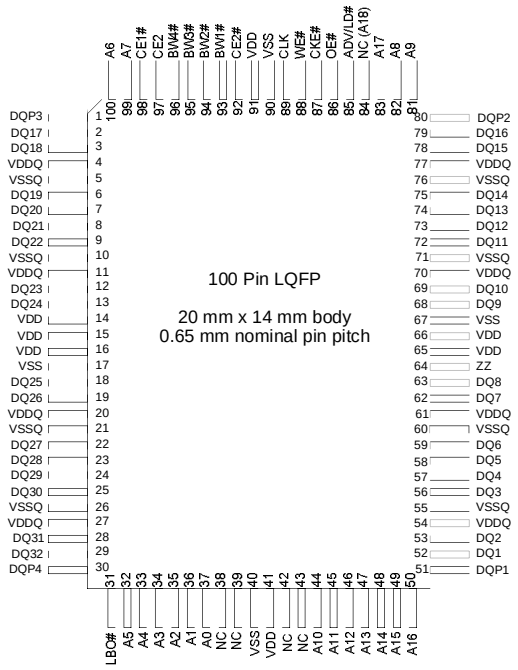
MC805256K36

9-MBIT: 256KX36

SYMMETRIC PIPELINED BURST SRAM

- **High Performance**
  - 133-200MHz Speed grades
  - 3-1-1-1 Burst Read
  - 3-1-1-1 Burst Write
  - 3-1-1-1-1-1-1-1... pipelined operation
- **Symmetric Pipeline**
  - No bus turnaround latency allowing 100% bus efficiency
- **Low Power**
  - Low active power
  - Low power ZZ standby mode
  - 2.5V Core power supply (V_{DD})
  - 2.5-3.3V I/O power supply (V_{DDQ})
- **Compatibility**
  - Individual Byte Write masking
  - Interleaved and burst address support
  - Three chip enable inputs
  - Clock Enable and Suspend
  - Industry standard 100-Pin pinout
- **Applications**
  - Ideal for high speed, low power data and tele-communications applications



Overview

The MoSys MC805256K36 is a high performance, low power symmetric pipelined-burst-SRAM (SPSRAM). Fabricated using an advanced low power, high performance CMOS process, the MoSys MC805256K36 is backward pin and function compatible with industry standard 64Kx36 and 128Kx36. With proper implementation, PC boards can work transparently with 64Kx36, 128Kx36 or 256Kx36 configurations, allowing the designer maximum configuration flexibility within a single footprint layout.

The MoSys MC805256K36 supports SPSRAM operating modes at maximum burst frequency including indefinite pipelined read or write (3-1-1-1-1-1-1-1...)

The MC805256K36 is packaged in a standard 100 lead LQFP.

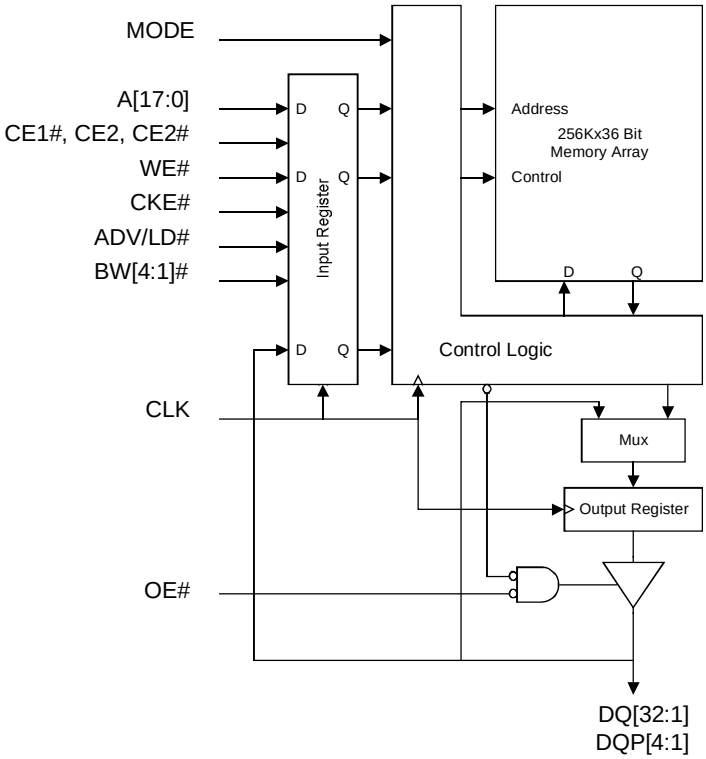
Low Power

The MC805256K36 affords systems power savings due to the benefits of its proprietary MoSys technology. Making it ideal for convection cooled applications, as well as applications requiring a large amount of SRAM.

Part Number Designation

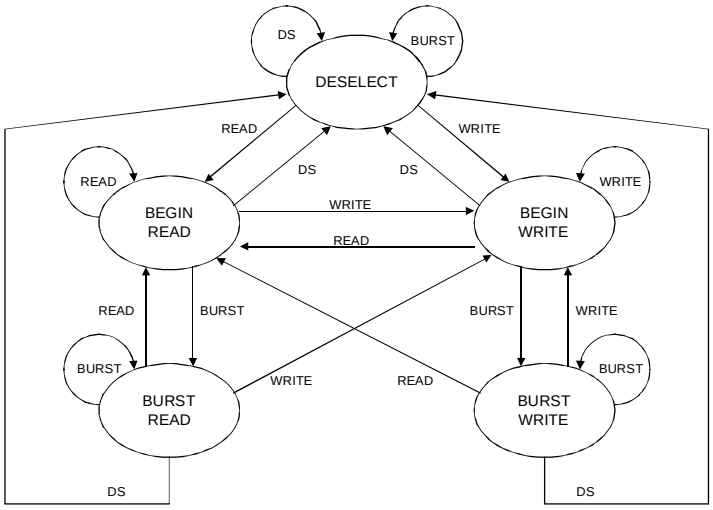
Example: *MC805256K36L-7R5I*
Device Designation: *MC8*:, Series: *05*
Organization: *256K36*
Package Type: L=LQFP
Speed: – 7R5 133MHz
– 6 166MHz
– 5 200MHz
Temp: *I* = Industrial Temperature

Parameter	Symbol	-7R5	-6	-5	Units
Cycle Time	tKC	7.5	6	5	ns
Access Time	tKQ	4.2	3.5	3.0	ns
Clock to High-Z	tKQHZ	3.8	3.1	2.9	ns



Functional Block Diagram

Command	Action
DS	DESELECT
READ	Begin READ
WRITE	Begin WRITE
BURST	Begin READ Begin WRITE Continue DESELECT



State Diagram

Command Truth Table

CE1#	CE2	CE2#	ZZ	ADV/ LD#	WE#	BWx#	OE#	CKE#	CLK	Address Used	Operation
H	X	X	L	L	X	X	X	L	↑	None	Deselect
X	L	X	L	L	X	X	X	L	↑	None	Deselect
X	X	H	L	L	X	X	X	L	↑	None	Deselect
X	X	X	L	H	X	X	X	L	↑	None	Continue Deselect
L	H	L	L	L	H	X	L	L	↑	External	Read Start
X	X	X	L	H	X	X	L	L	↑	Next	Read Burst
L	H	L	L	L	H	X	H	L	↑	External	Dummy Read
X	X	X	L	H	X	X	H	L	↑	Next	Dummy Read
L	H	L	L	L	L	L	X	L	↑	External	Write Start
X	X	X	L	H	X	L	X	L	↑	Next	Write Burst
L	H	L	L	L	L	H	X	L	↑	None	Write Abort
X	X	X	L	H	X	H	X	L	↑	Next	Write Abort
X	X	X	L	X	X	X	X	H	↑	Current	Ignore Clock
X	X	X	H	X	X	X	X	X	X	None	Sleep

Partial Read/Write Truth Table

WE#	BW4#	BW3#	BW2#	BW1#	Operation
H	X	X	X	X	READ
L	L	H	H	H	WRITE DQ[32:25] & DQP[4]
L	H	L	H	H	WRITE DQ[24:17] & DQP[3]
L	H	H	L	H	WRITE DQ[16:9] & DQP[2]
L	H	H	H	L	WRITE DQ[8:1] & DQP[1]
L	L	L	L	L	WRITE All DQ & DQP
L	H	H	H	H	WRITE Abort/NOP

Address Burst Sequence Tables

A[1:0]	A[1:0]	A[1:0]	A[1:0]	Linear Address, LBO#=L
00	01	10	11	1st Address
01	10	11	00	2nd Address
10	11	00	01	3rd Address
11	00	01	10	4th Address

A[1:0]	A[1:0]	A[1:0]	A[1:0]	Interleaved Address, LBO#=H
00	01	10	11	1st Address
01	00	11	10	2nd Address
10	11	00	01	3rd Address
11	10	01	00	4th Address

Pin Description

Pin Number	Symbol	Type	Description
83, 50, 49, 48, 47, 46, 45, 44, 81, 82, 99, 100, 32, 33, 34, 35, 36 ,37	A[17:0]	Input	Processor Addresses
96,95, 94, 93	BW[4:1]#	Input	Processor host bus byte enables
88	WE#	Input	Read/Write Control
87	CKE#	Input	Clock Enable
89	CLK	Input	Processor host bus clock
98	CE1#	Input	Chip enable
97	CE2	Input	Chip enable for depth expansion
92	CE2#	Input	Chip enable for depth expansion
86	OE#	Input	Asynchronous output enable
85	ADV/LD#	Input	Address Advance/Load# control
64	ZZ	Input	Low power sleep mode
31	LBO#	Input	Linear Burst Order
29, 28, 25, 24, 23, 22, 19, 18, 13, 12, 9, 8, 7, 6, 3, 2, 79, 78, 75, 74, 73, 72, 69, 68, 63, 62, 59, 58, 57, 56, 53, 52	DQ[32:1]	I/O	Data I/O pins
30, 1, 80, 51	DQP[4:1]	-	Data Parity I/O pins
38, 39, 42, 43, 84	NC	-	unused
14, 15, 16, 41, 65, 66, 91	VDD	2.5 Volts	Power
17, 40, 67, 90	VSS	Ground	Ground
4, 11, 20, 27, 54, 61, 70, 77	VDDQ	2.5 Volts	I/O Buffer Supply
5, 10, 21, 26, 55, 60, 71, 76	VSSQ	Ground	I/O Buffer Ground

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Core Supply Voltage		3.6	V
V_{DDQ}	I/O Supply Voltage		$V_{DDQ} \leq V_{DD} + 1.0$, $V_{DDQ} \leq 3.6$	V
V_{ih}	Input High Voltage		$V_{DDQ} + 1$	V
V_{il}	Input Low Voltage	V_{SSQ}-0.5		V
Ts	Storage Temperature	-65	150	°C

Notes: Max Vih is not to exceed maximum VDDQ

Capacitance

Symbol	Parameter	Typ	Max	Units
C_I	Input Capacitance	3	4	V
C_{IO}	I/O Capacitance	4	5	V

LQFP Thermal Resistance

Symbol	Parameter	Typ	Units
θ_{JA}	Junction to Ambient	45	°C/W
θ_{JC}	Junction to Case	9	°C/W

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Units
V_{DD}	Supply Voltage	2.5V ± 5%	2.375	2.625	V
V_{DDQ}	I/O Supply Voltage	2.5V ± 5%	2.375	2.625	V
V_{ih}	Input High Voltage		1.7	V_{DDQ} + .8	V
V_{il}	Input Low Voltage		-0.3	0.7	V
V_{oh}	Output High Voltage	I_{oh} = -1 mA	2.0		V
V_{ol}	Output Low Voltage	I_{ol} = 1 mA		0.2	V
T_{oprc}	Commercial Operating Temp.		0	70	°C
T_{opri}	Industrial Operating Temp.		-40	85	°C

Absolute Maximum AC Operating Conditions

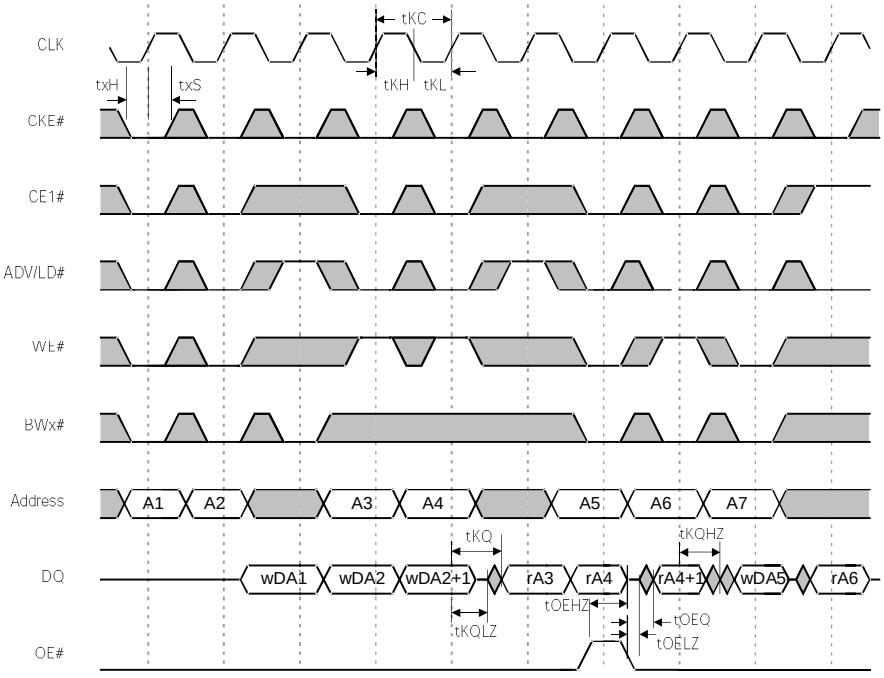
Symbol	Parameter	Min	Max	Units
V_{ih}	Input High Voltage	1.7	V_{DDQ}+1.0	V
V_{il}	Input Low Voltage	V_{SSQ} - 1.0	0.7	V
tOVR	Overshoot/Undershoot Voltage Duration		0.2*tCY	ns
tSET	Overshoot/Undershoot Settling Time		0.8*tCY	ns

Maximum DC Current Requirements

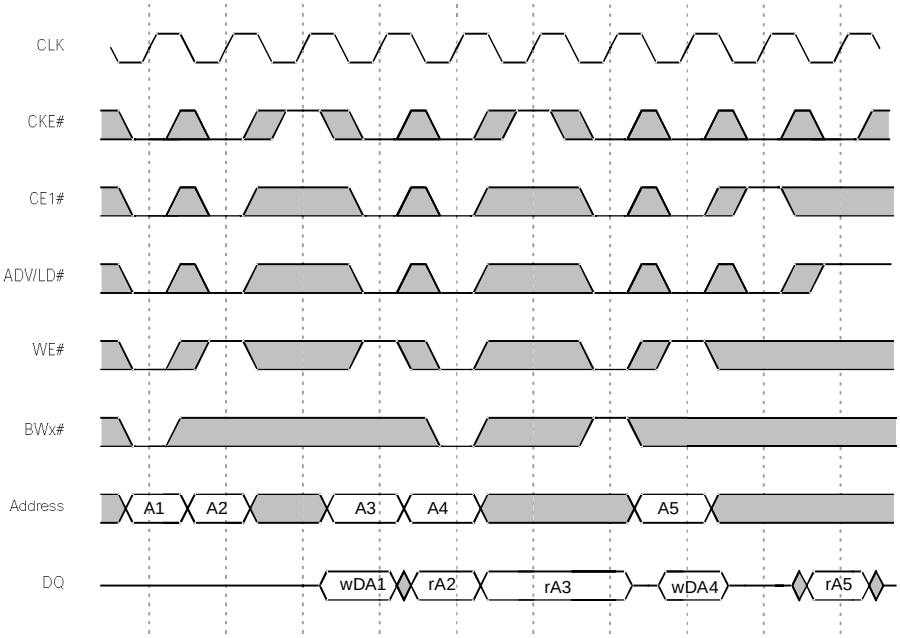
Symbol	Condition	Current	Units
I_{DD}	Operating current, device selected; all inputs ≤ Vil or ≥ Vih; cycle time ≥ 7.5ns, V_{DD}= max, 0 pF load	150	mA
I_{DD1}	Idle current; ADV/LD#, GW#, BW#s, CKE# and all other inputs ≥ 2.8 volts; cycle time ≥ tKC min, V_{DD}= max, 0 pF load	40	mA
I_{DDZ}	Sleep mode, clock stopped, all inputs ≥ 2.8 v, V_{DD}= max	20	mA

AC Timing Characteristics at Recommended Operating Conditions

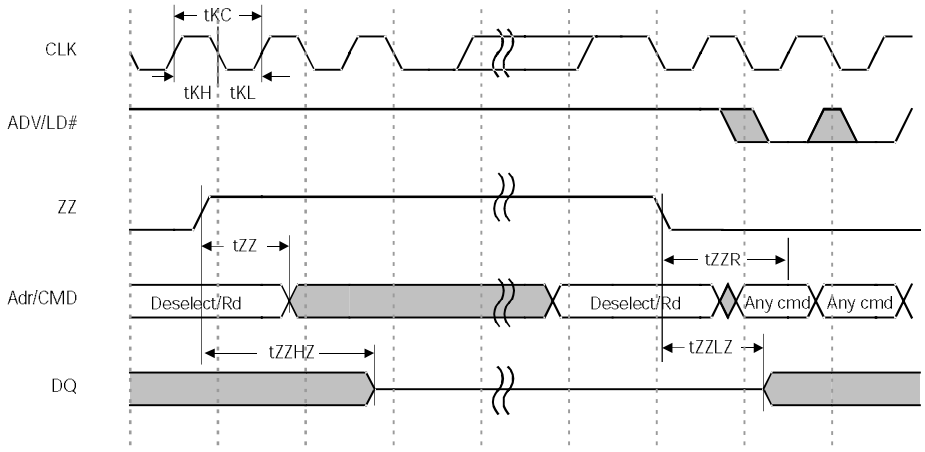
		-5 (200 MHz)		-6 (166 MHz)		-7R5 (133 MHz)		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
tKEH	CKE# hold	0.5		0.5		0.5		ns
tKES	CKE# setup	1.3		1.5		1.7		ns
tAAH	ADV/LD# hold	0.5		0.5		0.5		ns
tAAS	ADV/LD# setup	1.3		1.5		1.7		ns
tAH	Address hold	0.5		0.5		0.5		ns
tAS	Address setup	1.3		1.5		1.7		ns
tCEH	Chip Enable hold	0.5		0.5		0.5		ns
tCES	Chip Enable setup	1.3		1.5		1.7		ns
tDH	Write Data hold	0.5		0.5		0.5		ns
tDS	Write Data setup	1.3		1.5		1.7		ns
tWS	WE#, BWx# setup	1.3		1.5		1.7		ns
tWH	WE#, BWx# hold	0.5		0.5		0.5		ns
tKC	Clock cycle	5		6		7.5		ns
tKH	Clock high	2		2.5		3		ns
tKL	Clock low	2		2.5		3		ns
tKQ	Clock to output valid		3		3.5		4.2	ns
tKQHZ	Clock to output high-Z	1.5	2.9	1.5	3.1	1.5	3.8	ns
tKQLZ	Clock to output low-Z	1.5		1.5		1.5		ns
tKQX	Clock to output invalid	1.5		1.5		1.5		ns
tOELZ	OE# to output low-Z	0		0		0		ns
tOEHZ	OE# to output high-Z		3		3.5		4.2	ns
tOEQ	OE# to output valid		3		3.5		4.2	ns
tOEQX	OE# to output invalid	0		0		0		ns
tZZ	ZZ activation		2		2		2	tKC
tZZR	ZZ deactivation		5		5		5	tKC
tZZHZ	ZZ to DQ Hi-Z		100		100		100	tKC
tZZLZ	ZZ to DQ Lo-Z	0		0		0		tKC



Read/Write Timing



NOP, Stall, Deselect Timing



ZZ Timing

Test and Measurement

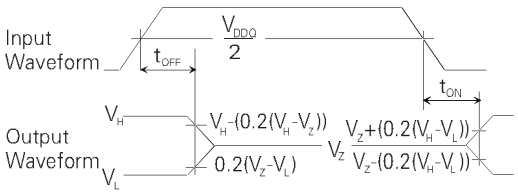
Test Structure and Measurement Points

Notes

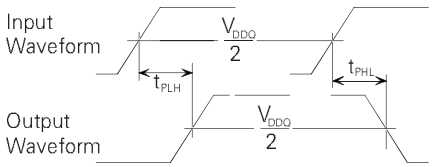
1 Valid Delay Measurement is made from the VDDQ / 2 on the input waveform to the VDDQ / 2 on the output waveform. Input waveform should have a slew rate of 1V/ns.

2 Iri-state t_{off} measurement is made from the VDDQ/2 on the input waveform to the output waveform moving 20% from its initial to final value VDDQ/2.

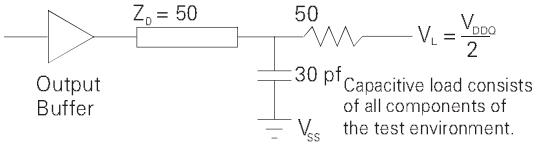
Tri-State Measurement



T_{DLY} Measurement



Output Load



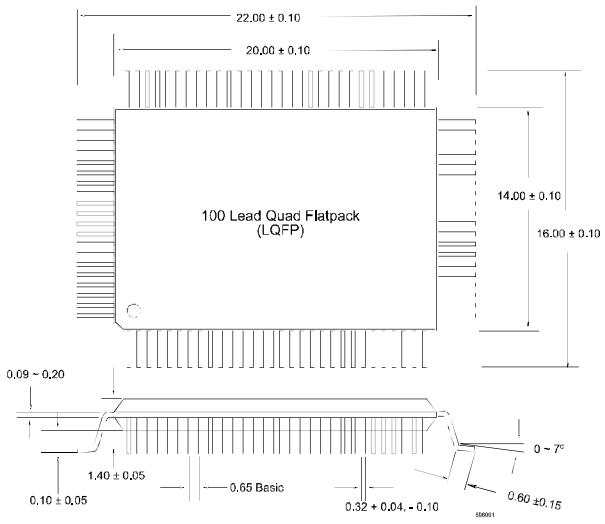


Figure 1. LQFP Mechanical Characteristics