

# NTMS4117N

## Product Preview

## Power MOSFET

### 30 V, 16 A, Single N-Channel, SO-8

#### Features

- Low  $R_{DS(on)}$
- Fast Switching Times
- Pb-Free Package is Available

#### Applications

- Notebooks, Graphics Cards
- Low Side Switch
- DC-DC

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	30	V
Gate-to-Source Voltage			V <sub>GS</sub>	± 20	V
Continuous Drain Current (Note 1)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	13.3	A
		T <sub>A</sub> = 85°C		9.6	
	t ≤ 10 s	T <sub>A</sub> = 25°C		16	
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	1.6	W
	t ≤ 10 s			2.3	
Continuous Drain Current (Note 2)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	9.9	A
		T <sub>A</sub> = 85°C		7.1	
Power Dissipation (Note 2)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	0.9	W
Pulsed Drain Current	tp = 10 μs		I <sub>DM</sub>	48	A
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Source Current (Body Diode)			I <sub>S</sub>	2.9	A
Single Pulse Drain-to-Source Avalanche Energy			E <sub>AS</sub>	TBD	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	79	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 10\text{ s}$ (Note 1)	$R_{\theta JA}$	53.5	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	142.5	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area 1.127 in sq [1 oz] including traces).
2. Surface mounted on FR4 board using the minimum recommended pad size (Cu area = TBD in sq).

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

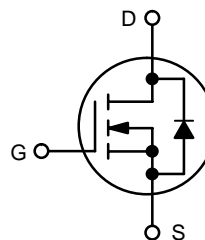


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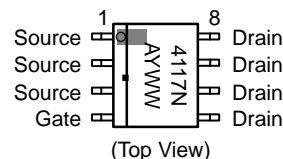
$V_{(BR)DS}$	$R_{DS(on)}$ TYP	$I_D$ MAX (Note 1)
30 V	4.0 m $\Omega$ @ 10 V	16 A
	5.5 m $\Omega$ @ 4.5 V	



#### MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8  
CASE 751  
STYLE 12



4117N = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

#### ORDERING INFORMATION

Device	Package	Shipping†
NTMS4117NR2	SO-8	2500/Tape & Reel
NTMS4117NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMS4117N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			TBD		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 125°C		10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.5		2.5	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			TBD		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13.3 A		4.0	5.25	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 11.5 A		5.5	7.0	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		TBD		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 24 V		4700		pF
Output Capacitance	C <sub>OSS</sub>			TBD		
Reverse Transfer Capacitance	C <sub>RSS</sub>			TBD		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 11.5 A		34.5	45	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			TBD		
Gate-to-Source Charge	Q <sub>GS</sub>			TBD		
Gate-to-Drain Charge	Q <sub>GD</sub>			TBD		
Gate Resistance	R <sub>G</sub>			1.2		Ω

### SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 4.5 V (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.0 A, R <sub>G</sub> = 3.0 Ω		34		ns
Rise Time	t <sub>r</sub>			TBD		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			TBD		
Fall Time	t <sub>f</sub>			TBD		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.9 A	T <sub>J</sub> = 25°C		0.8	1.0	V
			T <sub>J</sub> = 125°C		TBD		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, di <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 2.9 A			40		ns
Charge Time	t <sub>a</sub>				TBD		
Discharge Time	t <sub>b</sub>				TBD		
Reverse Recovery Charge	Q <sub>RR</sub>				TBD		nC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

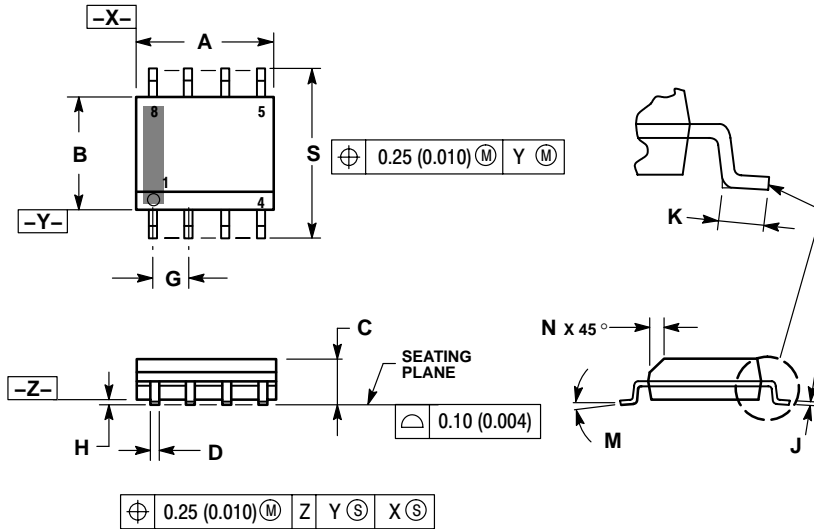
4. Switching characteristics are independent of operating junction temperatures.

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## PACKAGE DIMENSIONS

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SO-8  
CASE 751-07  
ISSUE AF



### NOTES:

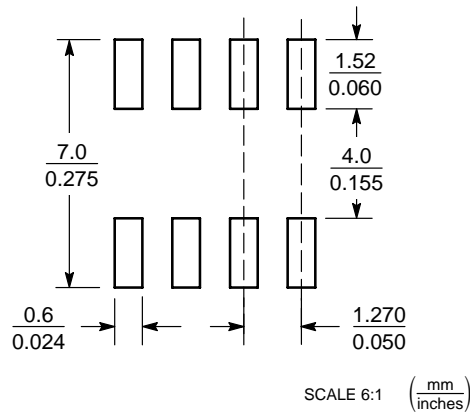
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244


### STYLE 12:

- PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN  
6. DRAIN  
7. DRAIN  
8. DRAIN

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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