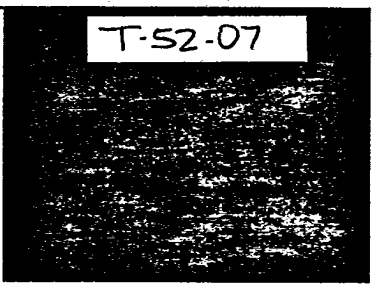
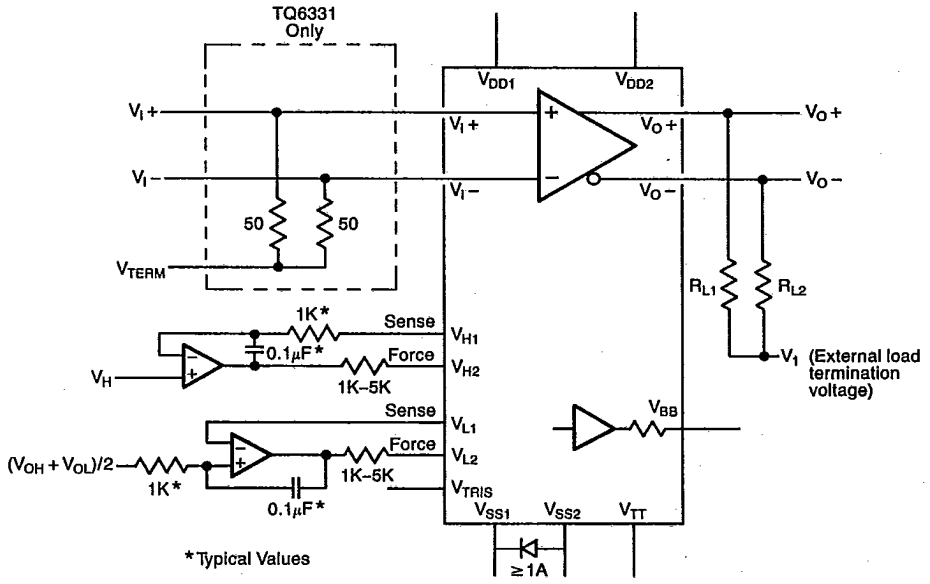


Pin Driver/ Line Receiver

Block Diagram:



Functional Description:

The TQ6330 is a pin or line driver whose output voltage levels can be adjusted between +3.0 Volts and −3.0 Volts when driving 50-Ohm load resistors. The output voltage levels are controlled by driving the level-control inputs. Sense outputs are provided so that the user may provide a level control input to achieve the desired output, either as a calibration procedure or in a feedback control loop. Each output is designed to produce a swing of up to 3 Volts (4V typical) into 50 Ohms with typical rise and fall times of 100ps (1V swing).

The outputs can typically switch from 5 Volts to 0 Volts when driving a high impedance load, making the TQ6330 suitable for driving CMOS or TTL. The inputs and outputs can be differential or single-ended. The inputs are compatible with standard ECL voltage levels.

The outputs can be switched to a "Tri-State" mode where they become 50-Ohm resistors connected to −2 Volts. The "Tri-State" condition of the outputs is controlled by an input which is ECL-compatible.

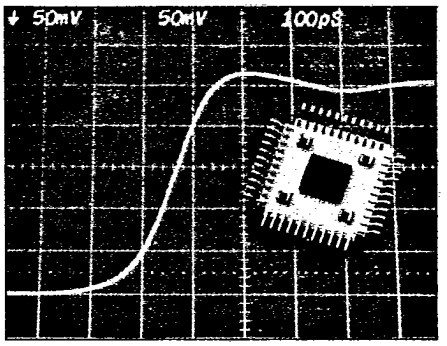
The TQ6331 line receiver is identical to the TQ6330 pin driver with the addition of 50-Ohm input termination resistors from V_I+ and V_I- to the common termination voltage pin, V_{TERM}.

Features:

- 100ps Rise and Fall Times, typical
- 3.0 Gbits/sec Data Rate, typical
- Controllable Output Voltage Levels
- Tri-State Outputs (50 Ohms to −2V)
- ECL-Compatible Inputs
- Inputs and Outputs can be Differential or Single-Ended

Applications:

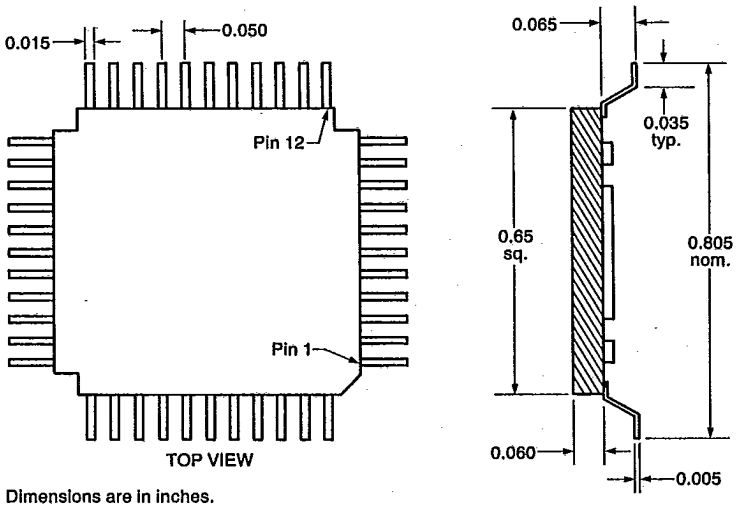
- High-Speed Test Systems
- Clock Driver/Buffer
- Fiber Optic Laser Drivers
- High-Speed Pulse Generators
- High-Speed Line Receivers
- High-Speed Modulators
- Signal Conditioning for High-Speed Counters



100ps risetime, 0.5V/div, differential output

TriQuint SEMICONDUCTOR
A TEKTRONIX COMPANY

Package Description



Dimensions are in inches.

The TQ6330 and TQ6331 are also available in die form, designated as TQ6330D and TQ6331D.

Pin Assignment

Pin	Name	Pin	Name
1	GND	23	GND
2	n.c.	24	V_I-
3	V_{DD1}	25	V_{TERM}
4	GND	26	GND
5	V_{DD1}	27	V_I+
6	V_O-	28	V_{BB}
7	GND	29	GND
8	V_{L1}	30	V_{DD1}
9	V_O+	31	V_{SS2}
10	GND	32	GND
11	V_{SS1}	33	V_{SS1}
12	GND	34	GND
13	V_{H1}	35	V_{TRIS}
14	V_{DD2}	36	V_{L2}
15	GND	37	GND
16	V_{DD2}	38	V_{H2}
17	V_{SS2}	39	V_{TT}
18	GND	40	GND
19	V_{SS1}	41	V_{SS1}
20	n.c.	42	V_{SS1}
21	GND	43	GND
22	V_{SS2}	44	V_{SS2}

Electrical Specifications

$V_{DD1} = V_{DD2} = +6V$ | $V_{SS1} = -6V$ | $V_{SS2} = -8V$ ...DC Specifications (typical)

$V_{IH} = -1.1V$ | $V_{IL} = -1.5V$

$V_{OH}^{(3)} = 3.0V^{(1)}, 5.0V^{(2)}$ | $V_{OL}^{(3)} = -3.0V$

$V_{OH} - V_{OL}^{(3)} = 0$ to $+4V^{(1)}$ | or 0 to $+8V^{(2)}$

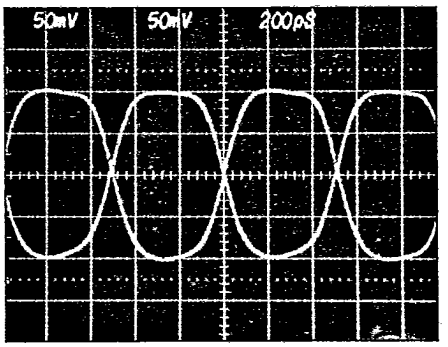
Power dissipation = 2W

$T_C = 27°C$

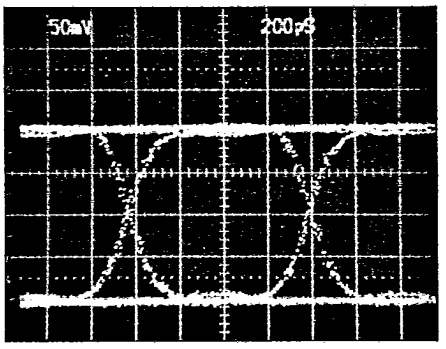
Data Rate NRZ: 3.0 Gbits/sec ...AC Specifications (typical, $V_{OH} - V_{OL} = 1V$)

Rise Time: (20% to 80%) 100ps

Note 1: $R_{LOAD} = 50$ Ohms.
Note 2: 1 TTL or CMOS load.
Note 3: User adjustable.



2 Gbits/sec, 0.5V/div, 50Ω load



Pseudo random data eye pattern
1.2 Gbits/sec NRZ data, 0.5V/div, 50Ω load

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