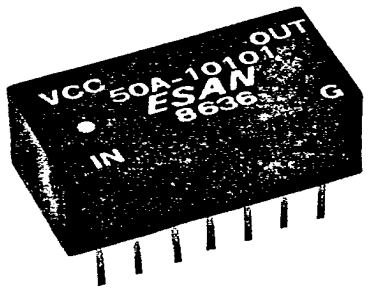
Active Delay Line (TTL Interface)

50A Series

- **10 Tap Output**
- **14 Pin Dip Package**
- **TTL Compatible**



Specifications:

- Delay tolerance : ±5% or 2ns whichever is greater
- Rise time : 4ns max.
- Temp. coefficient : 100 ppm/°C
- Operating Temp. Range : −0°C to 70°C −55°C to +125°C on request)
- Minimum Pulse Width : 40% of total delay
- Supply Voltage : 5VDC ±5%
- Logic 1 Input current : 50 UA max.
- Logic 0 Input current : −2 mA max.
- Logic 1 Output : 2.75V min.
- Logic 0 Output : 0.4V max.
- Logic 1 Fan out : 20/TAP max.
- Logic 0 Fan out : 10/TAP max.
- Power Dissipation : 780 mW max.

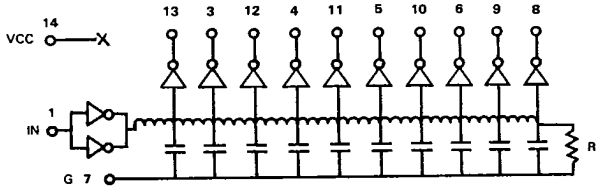
Test Conditions:

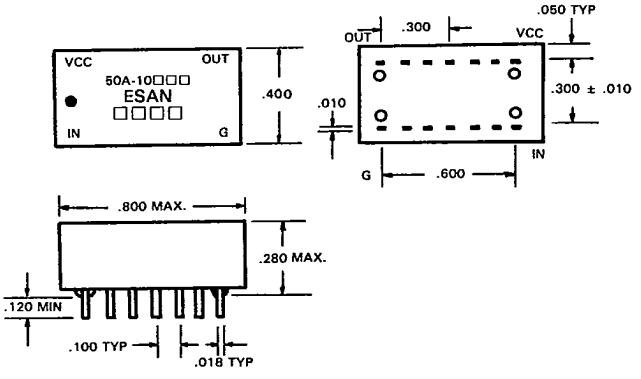
- Input pulse voltage : 3.2V
- Input pulse width : 1.2 * total delay
- Input pulse spacing : 2 * total delay
- Input pulse rise time: : 2 ns
- Rise time : 0.75V to 2.4V
- Time delay measured : @1.5V level
- All measurement : @Vcc=5.0V, TA=25°C

Features:

- Schottky TTL interface
- Low power schottky available named "50AL-10xxx" series
- Both Leading and Trailing edge available under request named "50B-10xxx" series
- Ceramic IC meet MIL-STD 883 level B available named "50AM-10xxx series"

PART NO.	TOTAL DELAY (ns)	DELAY (ns)
50A-10500	50	5
50A-10101	100	10
50A-10151	150	15
50A-10201	200	20
50A-10251	250	25
50A-10301	300	30
50A-10351	350	30
50A-10401	400	40
50A-10451	450	45
50A-10501	500	50





Unit: Inch