Improving System Performance through Intelligent Power Management

By Tony Ochoa

As the processor speeds have increased in the last few years, so has the speed or bandwidth of the data busses between the microprocessors, memory, and the system controller chips. Several bus standards and there respective signaling characteristics are now in use: GTL (Gunning Transceiver Logic) is used primarily for host CPU and the PCI/Memory Host Controller; SSTL (Series Stub Terminated Logic) is used for Host Controller to main memory (DDR SDRAM) or RAMBUS (Reflective Wave Switching) is used as an alternative for Host Controller to main memory (RDRAM).

Each of these bus schemes require a particular electrical bus termination scheme and a bus termination voltage. In addition, along the termination voltages of these buses (VTT), additional voltage references are sometimes needed to support the bus I/O operations. These voltage references are designated as VREF and VDDQ. See Table 1 for common voltage requirements for each of the buses.

In applications where data throughput is foremost and speed is critical, regulating the termination voltages and providing accurate voltage references can be very

Bus	Description	Output Driver	VDDQ	VTT	VREF System Components	Support Industry Examples
GTL+	Gunning Transceiver Bus Plus	Open Drain	5V or 3.3V	1.5V±10% (V_{DDQ})	1.0V ±2%	Processor: PC Chipsets: GTLP 16xxx Buffers: Fairchild, Texas Instr.
SSTL_2	Series Stub Terminated Logic for 2V	Symmetric Drive, Series Resistance	2.5V±10%	0.5x (V_{DDQ}) ±3%	2.5V	SSTL SDRAM: Hitachi Fujitsu, NEC, Micro, Mitsubishi
RAMBUS	RAMBUS Signaling Logic	Open Drain	None Specified	2.5V	2.0V	nDRAM, RAMBUS, Intel, Toshiba
LV-TTL	Low Voltage TTL Logic or PECL or 3.3V VME	Symmetric Drive	3.3V±10%	V_{DDQ}/2	3.3V	Processors or backplanes: LV-TTL SDRAM, EDO RAM

Table 1: Typical Bus Termination Voltage & Reference Voltage

important. Embedded applications and multiprocessor applications with shared memory architectures (large memory arrays) commonly will design for higher performance specs by margining the VTT and VREF of the bus. For example, Figure 1 shows a typical DDR SDRAM main memory termination scheme (double parallel stub termination). The SSTL standard specs by JEDEC list the VTT as 1.25V (VREF of 2.5V); however, system designers are finding that the Host Controller chips (or Graphics chips) and the memory chips can

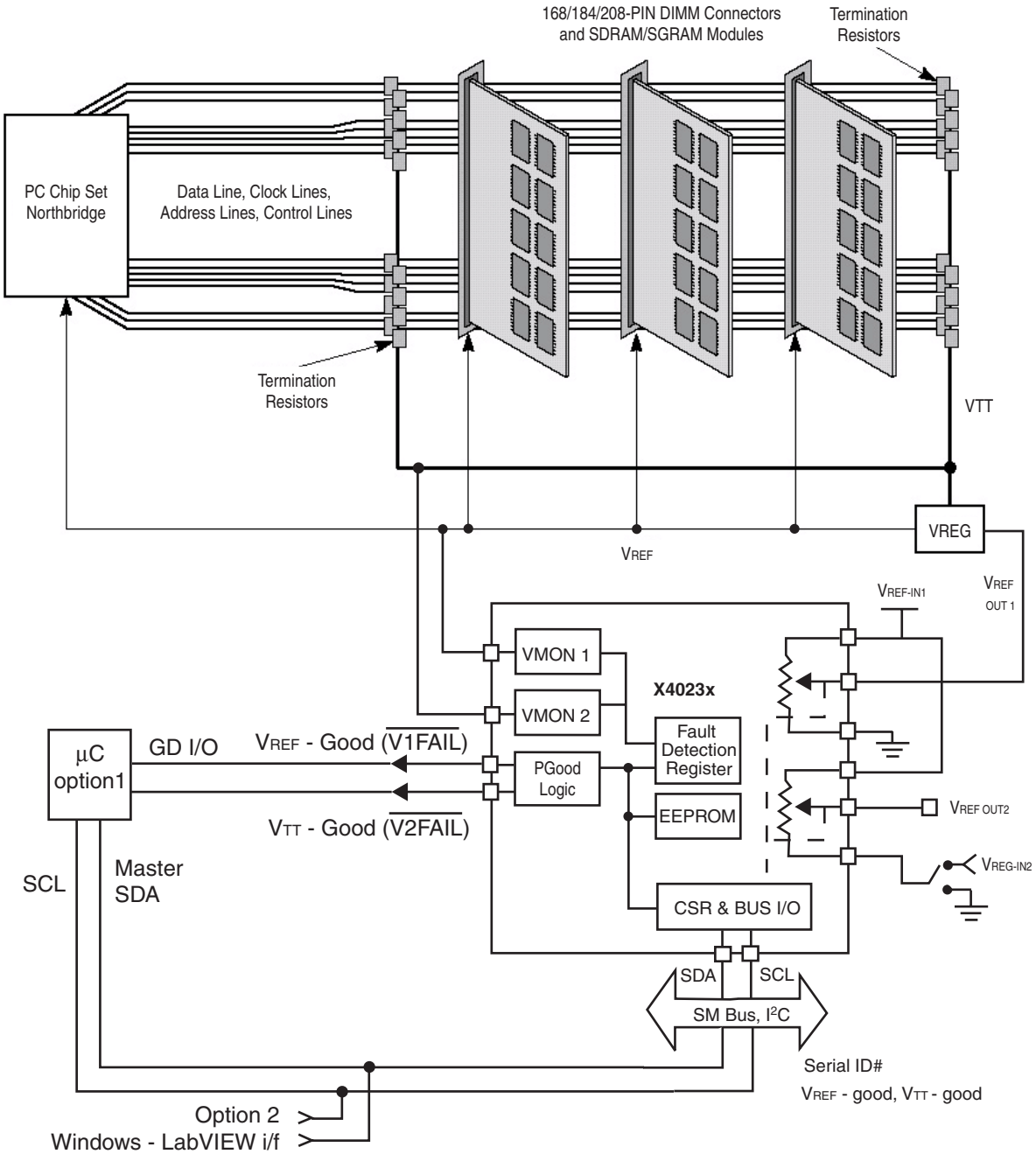

Figure 1: X4023x Used As High Speed Bus Voltage Monitor and VREF Output Control

actually vary in performance based upon the VREF and VTT voltages. For example the design in Figure 1 could operate with high data throughput at a VTT of 1.35V (VREF of 2.7V). The same concept can be applied to GTL or RAMBUS bus schemes as well.

Xicor provides a solution using the X4023x that can monitor and adjust the VTT and VREF voltages of the bus via either system control or through manufacturing calibration using a Windows-LabVIEW interface. The X4023x contains two voltage monitors, one to two digitally controlled potentiometers, a fault detection register, EEPROM, and a two-wire bus interface. Figure 1 depicts the use of the X4023x in a DDR SDRAM application. The two voltage monitors can be programmed to track the VREF and VTT signals. The voltage monitors issue an output signal when the VTT and VREF signals are valid (i.e. VREF_GOOD and VTT_GOOD) and also update the fault detection register. This allows the system to also query the X4023x for remote sensing of the condition of the VTT and VREF signals via the two-wire bus by reading the fault detection register status bits.

The X4023x contains one to two (optional) digitally-controlled potentiometers (XDCP®) that are used in a voltage-divider configuration to set and control the VTT and VREF levels (See Figure 1). Each XDCP acts as a voltage DAC that is programmed via the two-wire interface. The X4023x contains one of three possible XDCPs that can provide various voltage resolution and accuracy. For example, the 256-tap XDCP can provide 0.4% resolution. As a practical example, VTT can be selected from 2.5V to 0V with 0.4% resolution (256 levels).

In addition, since the XDCP is used in a voltage divider configuration or a “ratiometric” mode the voltage variation vs. temperature is typically 20 PPM per degree Celsius. Furthermore if higher accuracy is needed the potentiometer voltages (VH and VL) can be set such that higher resolutions may be achieved by setting VL to a voltage above ground (see Figure 1 VREF_IN2).

Note that once the wiper position of the XDCP has been optimized the position of the wiper is stored in non-volatile memory and is recalled during power up – this feature allows “set-and-forget” applications and provides automation in manufacturing for calibration.

System Control vs. Manufacturing Tuning

The X4023x can be used to make adjustments in a closed-loop system or in an open-loop system. For closed-loop applications a simple microcontroller can be used to monitor the VREF and VTT status signals of the X4023x and to make real-time adjustments of the VTT or VREF signals via the two-wire bus (See Figure 1). For open-loop
applications, where the VTT and VREF are set in manufacturing or calibration modes, Xicor offers LabVIEW-Window drivers for the X4023x. This software tool requires only a PC and the free software from Xicor (www.xicor.com) to program the X4023x. Customers can use the parallel port, serial port, IEEE-488 or any customer interface to access the DUT (device under test). The LabVIEW drivers emulate the 2-wire commands set to program the X4023x while Windows 98 / NT / 2000 provides the GUI interface to program the device (see Figure 2).

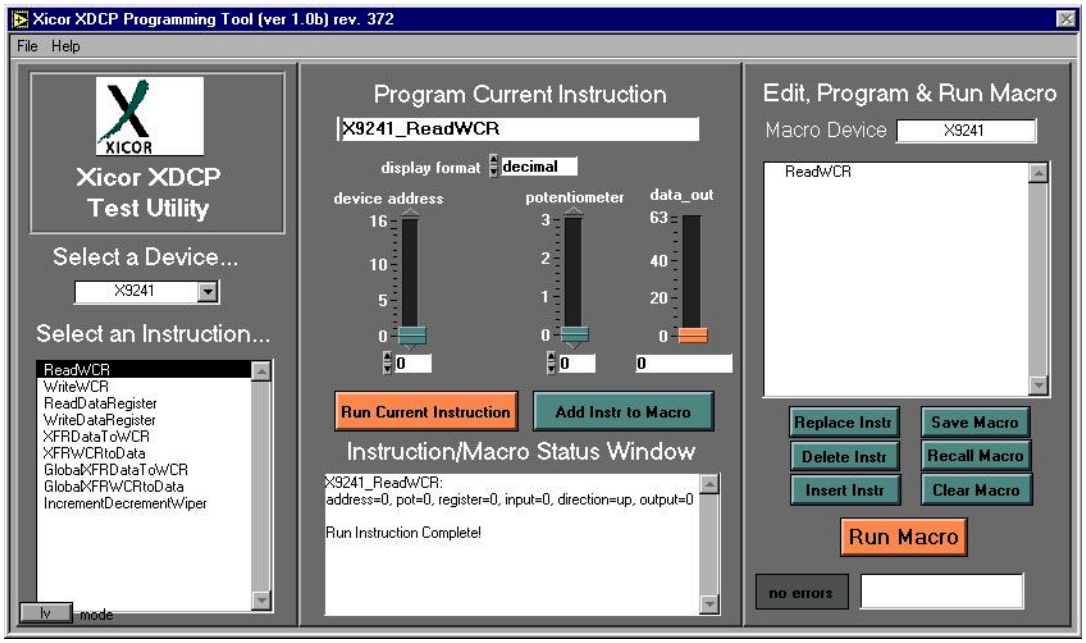

Figure 2: Using LabVIEW-Windows Interface to Program VTT and VREF

In summary, the X4023x provides excellent bus voltage monitoring and VTT and VREF output voltage adjustment to improve high speed data throughput and signal integrity. It also provides system level monitoring of the VTT and VREF signals. The X4023x is easy to use via system control for “set and forget” applications. The X4023x is ideal for applications with embedded controller designs, fault tolerant systems, large memory array or multiprocessor systems.