Genesys Logic, Inc.

GL9714

PCI Express™ PIPE x4 PHY

Datasheet
Revision 1.32
Apr. 16, 2007

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Revision History

Revision	Date	Description
1.00	09/27/2004	First formal release
1.10	04/04/2005	Update for mass production version
1.11	04/12/2005	Revise register description(SW, DEM), p.19
1.12	04/20/2005	1. Add operating current for DC electrical characteristics in Table7.1 2. Correct Power Consumption
1.13	09/20/2005	Modify Package Dimension ,Ch9 , p.39
1.14	10/13/2005	1. Add "Bottom View", Ch3.1, p.10 2. Change Pin E15 from "TXDK1" to "TXDKA", Table3.1, p.11 3. Change TXDKA~D type from "O" to "I", Table3.4, p.15 4. Add a column "I/O Standard", Table3.4, p.15 5. Change VDDPLL from "C18" to "C8", Table3.4, p.16 6. Add comment for SCC and OPMODE[1:0], Table3.4 , p.17
1.16	11/15/2005	1. Update Table3.4, p.15~p.17 2. Add Table3.5, p.17 3. Modify the default value of REG0 and REG1 in Table4.1, p.18 4. Modify Ch4.2 Registers Descriptions for REG0 and REG1, p.19 5. Add Ch 4.3, p.21~p.24 6. Update Table 7.5 and Table 7.6 for power consumption, p.36~p.37 7. Change TXDx to RXDx, Figure8.4, p.41 8. The minimum and maximum value of $T_{CYCLE,}$ Table8.2 and Table 8.5, p.42
1.17	12/15/2005	1. Update Table 7.9 for temperature ranges (p.39) 2. Update Table 8.1~8.4 for output delay of RX bus (p.41~p.42)
1.18	03/15/2006	1. Modify the description of OSC25MI and OSC25MO signals, Table 3.4, p.17 2. Update Table 7.1 for deleting I_{DD1-X4}, I_{DD2-X4}, I_{DD3-X4}, I_{DD1-X2}, I_{DD2-X2}, and I_{DD3-X2} six items, p.34 3. Update Table 7.9 for deleting the $I_{SUPPLY-1.8}$ item and adding θ_{JA}, Ψ_{JT} and θ_{JC} three items, p.39
1.19	03/28/2006	Swap the Pin Out of OSC25MI and OSC25MO in Table 3.1~Table 3.4.
1.20	03/30/2006	Update Table 7.9 for the illustration and the value of thermal parameters, p.39
1.21	04/26/2006	Divide Table 7.9 into Table 7.9(Temperature Range) and Table 7.10(Thermal Characteristics), p.39
1.22	05/08/2006	Update Fig. 8.1, 8.2 and Table 8.1~8.5 for PIPE input and output timing characteristic, p.40~p.42
1.23	06/09/2006	Update Table 8.1~8.5 for the description of T_{CO} and T_{OH}, p.41~p.42
1.24	06/20/2006	1.Update Table 3.5 for the parameter of buffer I/O, p.17 2.Remove Table 7.2, p.34
1.25	07/31/2006	1.Remove REN and PLPBK bits of SMBus register REGC, p.20 2.Add REG14 ~ REG17 for SLPBK error count result, p.21 3.Add "PS: Please write "0" to……." description, p.21
1.26	10/27/2006	Add $Duty\text{-}_H$ field for Table 8.3 and Table 8.5, p.43
1.30	02/06/2007	Update Table 8.1~8.5 for timing issue, p.42~44
1.31	03/19/2007	1. Add a note to Table 8.1, p.42 2. Update Table 7.4, 7.5 for the power consumption of reference voltage 1.25V, p37~p38, correct the index of table7.2, 7.3, p35
1.32	04/16/2007	Complies with PCI Express Base Specification rev. 1.1, p9

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CHAPTER 1 GENERAL DESCRIPTION

The GL9714 is a 4-lane PCI Express PHY Layer Controller, which is compliant with PCI Express Base Specification rev. 1.0a and Intel's PHY Interface for the PCI Express Architecture rev. 1.0. It integrates a quad SerDes and the Physical Coding Sublayer (PCS) which performs 8b/10b encoding and decoding, elastic buffer and receiver detection, data serialization and deserialization for each lane. The quad SerDes in the GL9714 supports an effective serial interface speed (2.5 Gb/s) of data bandwidth for each lane, intended for use in ultrahigh-speed bi-directional data transmission system. The GL9714 can also be externally configured for various combinations of lane number and parallel bus width which is flexible and suitable for x1, x2 or x4 lane implementation. It also supports four operational states for power management to minimize power consumption. For production and self-test purposes, the GL9714 provides BIST and an internal loopback capability.

The primary application of this chip is to provide very high-speed I/O data channels for point-to-point baseband data transmission over an on-chip termination resister of 50 Ohm +/- 10%.

This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector pins, and transmit/receive pins. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel. It is then reconstructed into its original parallel format. The maximum data transfer rate in each direction is 1 Giga byte per second with the 4-lane configuration. It also offers various power saving modes to significantly reduce power consumption as well as scalability for a higher data rate in the future.

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CHAPTER 2 FEATURES

- Complies with PCI Express Base Specification rev. 1.1
- Complies with Intel's PHY Interface for PCI Express Architecture rev. 1.0
- Integrates quad 2.5 gigabit per second (Gbps) Serializer/Deserializer
- Supports 8-bit or 10-bit parallel interface @250MHz for x1, x2 and x4 implementation
- Supports 16-bit parallel interface @125MHz for x1 and x2 configuration
- Supports DDR configuration for 8-bit or 10-bit mode
- Beacon transmission and reception
- Receiver detection
- Transmission and detection of electrical idle
- Clock tolerance for 600 ppm in frequencies between bit rates at the two end of a Link
- On-chip 8-bit/10-bit encoding/decoding and comma alignment
- On-chip PLL provides clock synthesis
- 1.8-V power supply for core
- 2.5-V power supply for IO
- Above 2.0 kV ESD protection
- 0.18 µm process
- Available in LFBGA-233 package

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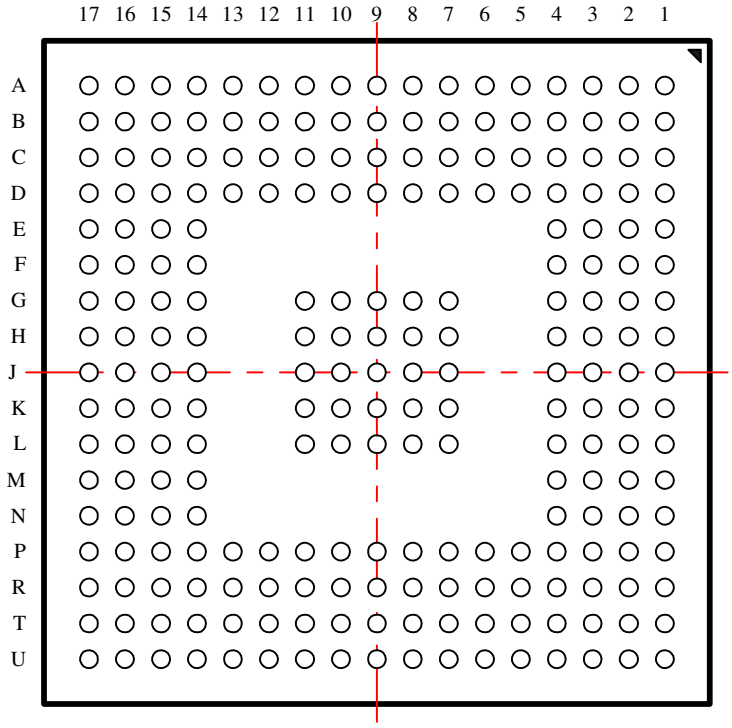
CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout



Bottom View

Figure 3.1 - 233 Pin LFBGA Pinout Diagram

3.2 Ball Out

Table 3.1 - Ball Out

	1	2	3	4	5	6	7	8	9
A	REFCLKP	TXND	VDDTXD	RXND	VDDRXD	TXNC	VDDTXC	RXNC	VDDRXC
B	REFCLKN	TXPD	VSSTXD	RXPD	VSSRXD	TXPC	VSSTXC	RXPC	VSSRXC
C	OSC25MO	RXDD7	NC	VDD18	NC	NC	VSSTXC	VDDPLL	NC
D	OSC25MI	VDD25	RXDD3	VSS	VSS	NC	VDD18	RTERM	VSSPLL
E	RXDKD	RXDD1	RXDD4	RXDD5					
F	VSS	RXSTSD1	RXDD2	RXDD6					
G	TXCMPD	VDD25	RXSTSD2	RXDD0			VSS	VSS	VSS
H	TXDD4	TXDD6	TXDD7	RXSTSD0			VSS	VSS	VSS
J	TXDD2	VSS	TXDD5	TXDD3			VSS	VSS	VSS
K	VDD25	TXDD0	TXDD1	VDD12			VSS	VSS	VSS
L	VSS	VSS	TXDKD	VDD18			VSS	VSS	VSS
M	VSS	RXDC7	VDD18	RXDC4					
N	RXDC5	VSS	RXDC6	RXDC0					
P	VDD25	RXDC1	RXDC2	RXSTSC2	RXSTSC0	TXDC3	TXDKC	RXIDLED	VSS
R	RXDC3	RXSTSC1	TXCMPC	TXDC7	TXDC5	TXDC1	VSS	RXPLRD	OPMODE0

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T	RXDKC	VDD25	TXDC6	TXDC2	VDD25	VDD18	TXIDLED	RXIDLEC	RXPLRC
U	VSS	TXDC4	VSS	TXDC0	PHYSTS	RXVLDD	RXVLDC	TXIDLEC	VDD25
	1	2	3	4	5	6	7	8	9

	10	11	12	13	14	15	16	17	
A	TXNB	VDDTXB	RXNB	VDDRXB	TXNA	VDDTXA	RXNA	VDDRXA	
B	TXPB	VSSTXB	RXPB	VSSRXB	TXPA	VSSTXA	RXPA	VSSRXA	
C	VDD18	NC	VDD18	NC	TXDA1	VSSGR	TXDA6	TXDA7	
D	NC	NC	NC	TXDA0	TXDA3	TXDA4	VDD25	RXSTSA2	
E					TXDA5	TXDKA	TXDA2	RXDKA	
F					RXSTSA0	TXCMPA	RXDA0	VDD25	
G	VSS	VSS			RXSTSA1	RXDA1	RXDA2	RXDA4	
H	VSS	VSS			RXDA5	RXDA3	RXDA7	VDD18	
J	VSS	VSS			VDD12	VSS	RXDA6	VDD18	
K	VSS	VSS			TXDB2	VDD25	TXDKB	NC	
L	VSS	VSS			TXCMPB	TXDB6	TXDB1	TXDB0	
M					RXSTSB1	TXDB4	TXDB3	VSS	
N					RXDB3	RXDKB	TXDB7	TXDB5	
P	PD1	RXVLDB	RXVLDA	RXDB7	RXDB5	RXDB1	VSS	RXSTSB0	
R	SCC	TXDET/ LPBK	TXIDLEB	VDD25	TXIDLEA	RXDB4	RXDB0	VDD25	
T	TESTD	PD0	RXIDLEB	RXIDLEA	PCLK	VSS	RXDB2	RXSTSB2	
U	OPMODE1	TESTC	RST_N	RXPLRB	VSS	RXPLRA	RXDB6	VDD25	
	10	11	12	13	14	15	16	17	

3.3 Pin List

Table 3.2 - Numeric Pin List

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
A1	REFCLKP	C1	OSC25MO	E1	RXDKD	G1	TXCMPD	J1	TXDD2
A2	TXND	C2	RXDD7	E2	RXDD1	G2	VDD25	J2	VSS
A3	VDDTXD	C3	NC	E3	RXDD4	G3	RXSTSD2	J3	TXDD5
A4	RXND	C4	VDD18	E4	RXDD5	G4	RXDD0	J4	TXDD3
A5	VDDRXD	C5	NC	E5		G5		J5	
A6	TXNC	C6	NC	E6		G6		J6	
A7	VDDTXC	C7	VSSTXC	E7		G7	VSS	J7	VSS
A8	RXNC	C8	VDDPLL	E8		G8	VSS	J8	VSS
A9	VDDRXC	C9	NC	E9		G9	VSS	J9	VSS
A10	TXNB	C10	VDD18	E10		G10	VSS	J10	VSS
A11	VDDTXB	C11	NC	E11		G11	VSS	J11	VSS
A12	RXNB	C12	VDD18	E12		G12		J12	
A13	VDDRXB	C13	NC	E13		G13		J13	

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A14	TXNA	C14	TXDA1	E14	TXDA5	G14	RXSTSA1	J14	VDD12
A15	VDDTXA	C15	VSSGR	E15	TXDKA	G15	RXDA1	J15	VSS
A16	RXNA	C16	TXDA6	E16	TXDA2	G16	RXDA2	J16	RXDA6
A17	VDDRXA	C17	TXDA7	E17	RXDKA	G17	RXDA4	J17	VDD18
B1	REFCLKN	D1	OSC25MI	F1	VSS	H1	TXDD4	K1	VDD25
B2	TXPD	D2	VDD25	F2	RXSTSD1	H2	TXDD6	K2	TXDD0
B3	VSSTXD	D3	RXDD3	F3	RXDD2	H3	TXDD7	K3	TXDD1
B4	RXPD	D4	VSS	F4	RXDD6	H4	RXSTSD0	K4	VDD12
B5	VSSRXD	D5	VSS	F5		H5		K5	
B6	TXPC	D6	NC	F6		H6		K6	
B7	VSSTXC	D7	VDD18	F7		H7	VSS	K7	VSS
B8	RXPC	D8	RTERM	F8		H8	VSS	K8	VSS
B9	VSSRXC	D9	VSSPLL	F9		H9	VSS	K9	VSS
B10	TXPB	D10	NC	F10		H10	VSS	K10	VSS
B11	VSSTXB	D11	NC	F11		H11	VSS	K11	VSS
B12	RXPB	D12	NC	F12		H12		K12	
B13	VSSRXB	D13	TXDA0	F13		H13		K13	
B14	TXPA	D14	TXDA3	F14	RXSTSA0	H14	RXDA5	K14	TXDB2
B15	VSSTXA	D15	TXDA4	F15	TXCMPA	H15	RXDA3	K15	VDD25
B16	RXPA	D16	VDD25	F16	RXDA0	H16	RXDA7	K16	TXDKB
B17	VSSRXA	D17	RXSTSA2	F17	VDD25	H17	VDD18	K17	NC

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin	Pin Name
L1	VSS	N1	RXDC5	R1	RXDC3	U1	VSS
L2	VSS	N2	VSS	R2	RXSTSC1	U2	TXDC4
L3	TXDKD	N3	RXDC6	R3	TXCMPC	U3	VSS
L4	VDD18	N4	RXDC0	R4	TXDC7	U4	TXDC0
L5		N5		R5	TXDC5	U5	PHYSTS
L6		N6		R6	TXDC1	U6	RXVLDD
L7	VSS	N7		R7	VSS	U7	RXVLDC
L8	VSS	N8		R8	RXPLRD	U8	TXIDLEC
L9	VSS	N9		R9	OPMODE0	U9	VDD25
L10	VSS	N10		R10	SCC	U10	OPMODE1
L11	VSS	N11		R11	TXDET/LPBK	U11	TESTC
L12		N12		R12	TXIDLEB	U12	RST_N
L13		N13		R13	VDD25	U13	RXPLRB
L14	TXCMPB	N14	RXDB3	R14	TXIDLEA	U14	VSS
L15	TXDB6	N15	RXDKB	R15	RXDB4	U15	RXPLRA

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L16	TXDB1	N16	TXDB7	R16	RXDB0	U16	RXDB6
L17	TXDB0	N17	TXDB5	R17	VDD25	U17	VDD25
M1	VSS	P1	VDD25	T1	RXDKC		
M2	RXDC7	P2	RXDC1	T2	VDD25		
M3	VDD18	P3	RXDC2	T3	TXDC6		
M4	RXDC4	P4	RXSTSC2	T4	TXDC2		
M5		P5	RXSTSC0	T5	VDD25		
M6		P6	TXDC3	T6	VDD18		
M7		P7	TXDKC	T7	TXIDLED		
M8		P8	RXIDLED	T8	RXIDLEC		
M9		P9	VSS	T9	RXPLRC	Blank	
M10		P10	PD1	T10	TESTD		
M11		P11	RXVLDB	T11	PD0		
M12		P12	RXVLDA	T12	RXIDLEB		
M13		P13	RXDB7	T13	RXIDLEA		
M14	RXSTSB1	P14	RXDB5	T14	PCLK		
M15	TXDB4	P15	RXDB1	T15	VSS		
M16	TXDB3	P16	VSS	T16	RXDB2		
M17	VSS	P17	RXSTSB0	T17	RXSTSB2		

Table 3.3 - Alphabetic Pin List

Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#
NC	C3	RXDD0	G4	TXCMPA	F15	TXNC	A6	VSS	H7
NC	C5	RXDD1	E2	TXCMPB	L14	TXND	A2	VSS	H8
NC	C6	RXDD2	F3	TXCMPC	R3	TXPA	B14	VSS	H9
NC	C9	RXDD3	D3	TXCMPD	G1	TXPB	B10	VSS	H10
NC	C11	RXDD4	E3	TXDA0	D13	TXPC	B6	VSS	H11
NC	C13	RXDD5	E4	TXDA1	C14	TXPD	B2	VSS	J2
NC	D6	RXDD6	F4	TXDA2	E16	VDD12	J14	VSS	J7
NC	D10	RXDD7	C2	TXDA3	D14	VDD12	K4	VSS	J8
NC	D11	RXDKA	E17	TXDA4	D15	VDD18	C4	VSS	J9
NC	D12	RXDKB	N15	TXDA5	E14	VDD18	C10	VSS	J10
NC	K17	RXDKC	T1	TXDA6	C16	VDD18	C12	VSS	J11
OPMODE0	R9	RXDKD	E1	TXDA7	C17	VDD18	D7	VSS	J15
OPMODE1	U10	RXIDLEA	T13	TXDB0	L17	VDD18	H17	VSS	K7
OSC25MO	C1	RXIDLEB	T12	TXDB1	L16	VDD18	J17	VSS	K8
OSC25MI	D1	RXIDLEC	T8	TXDB2	K14	VDD18	L4	VSS	K9
PCLK	T14	RXIDLED	P8	TXDB3	M16	VDD18	M3	VSS	K10

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PD0	T11	RXNA	A16	TXDB4	M15	VDD18	T6	VSS	K11
PD1	P10	RXNB	A12	TXDB5	N17	VDD25	D2	VSS	L1
PHYSTS	U5	RXNC	A8	TXDB6	L15	VDD25	D16	VSS	L2
REFCLKN	B1	RXND	A4	TXDB7	N16	VDD25	F17	VSS	L7
REFCLKP	A1	RXPA	B16	TXDC0	U4	VDD25	G2	VSS	L8
RST_N	U12	RXPB	B12	TXDC1	R6	VDD25	K1	VSS	L9
RTERM	D8	RXPC	B8	TXDC2	T4	VDD25	K15	VSS	L10
RXDA0	F16	RXPD	B4	TXDC3	P6	VDD25	P1	VSS	L11
RXDA1	G15	RXPLRA	U15	TXDC4	U2	VDD25	R13	VSS	M1
RXDA2	G16	RXPLRB	U13	TXDC5	R5	VDD25	R17	VSS	M17
RXDA3	H15	RXPLRC	T9	TXDC6	T3	VDD25	T2	VSS	N2
RXDA4	G17	RXPLRD	R8	TXDC7	R4	VDD25	T5	VSS	P9
RXDA5	H14	RXSTSA0	F14	TXDD0	K2	VDD25	U9	VSS	P16
RXDA6	J16	RXSTSA1	G14	TXDD1	K3	VDD25	U17	VSS	R7
RXDA7	H16	RXSTSA2	D17	TXDD2	J1	VDDPLL	C8	VSS	T15
RXDB0	R16	RXSTSB0	P17	TXDD3	J4	VDDRXA	A17	VSS	U1
RXDB1	P15	RXSTSB1	M14	TXDD4	H1	VDDRXB	A13	VSS	U3
RXDB2	T16	RXSTSB2	T17	TXDD5	J3	VDDRXC	A9	VSS	U14
RXDB3	N14	RXSTSC0	P5	TXDD6	H2	VDDRXD	A5	VSSGR	C15
RXDB4	R15	RXSTSC1	R2	TXDD7	H3	VDDTXA	A15	VSSPLL	D9
RXDB5	P14	RXSTSC2	P4	TXDET/LPBK	R11	VDDTXB	A11	VSSRXA	B17
RXDB6	U16	RXSTSD0	H4	TXDKA	E15	VDDTXC	A7	VSSRXB	B13
RXDB7	P13	RXSTSD1	F2	TXDKB	K16	VDDTXD	A3	VSSRXC	B9
RXDC0	N4	RXSTSD2	G3	TXDKC	P7	VSS	D4	VSSRXD	B5
RXDC1	P2	RXVLDA	P12	TXDKD	L3	VSS	D5	VSSTXA	B15
RXDC2	P3	RXVLDB	P11	TXIDLEA	R14	VSS	F1	VSSTXB	B11
RXDC3	R1	RXVLDC	U7	TXIDLEB	R12	VSS	G7	VSSTXC	B7
RXDC4	M4	RXVLDD	U6	TXIDLEC	U8	VSS	G8	VSSTXC	C7
RXDC5	N1	SCC	R10	TXIDLED	T7	VSS	G9	VSSTXD	B3
RXDC6	N3	TESTC	U11	TXNA	A14	VSS	G10		
RXDC7	M2	TESTD	T10	TXNB	A10	VSS	G11		

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3.4 Pin Descriptions

Table 3.4 - Pin Descriptions

PIPE Interface				
Pin Name	**I/O Standard**	**Pin#**	**Type**	**Description**
RST_N	LVCMOS2	U12	I	Global reset
PCLK	SSTL2_I	T14	O	Parallel interface clock All data movement across the parallel interface is synchronous to this clock. 1. For 8-bit mode: PCLK operates at 250 MHz and is applied to synchronize all TXDx, RXDx data bus and all commands. 2. For 16-bit mode: PCLK operates at 125 MHz and is applied to synchronize all TXDx, RXDx data bus and all commands. 3. For 10-bit mode(TBC): PCLK operates at 250 MHz and is applied to synchronize the TXDx data bus and all commands.
RXSTSA[2:0] RXSTSB[2:0] RXSTSC[2:0] RXSTSD[2:0]	SSTL2_I	D17, G14, F14 T17, M14, P17 P4, R2, P5 G3, F2, H4	O	1. For 8-bit and 16-bit modes: Encodes receiver status and error codes for the received data stream and receiver detection 000 Received data OK 001 1 SKP added 010 1 SKP removed 011 Receiver detected 100 8B/10B decode error 101 Elastic Buffer overflow 110 Elastic Buffer underflow 111 Receiver disparity error 2. For 10-bit modes: RXSTSx[2]: RBCx, synchronize the RXDx data bus RXSTSx[1]: RXPRSNTx, report the result of receiver detection RXSTSx[0]: RXDx9, bit 9 of RXDx data bus
RXIDLEA~D	LVCMOS2	T13, T12, T8, P8	O	Indicates receiver detection of an electrical idle This is an asynchronous signal.
PHYSTS	SSTL2_I	U5	O	Used to communicate completion of several PHY functions including power state transitions and receiver detection
RXVLDA~D	LVCMOS2	P12, P11, U7, U6	O	Indicates symbol lock and valid data on RXDx and RXDKx
TXCMPA~D	SSTL2_I	F15, L14, R3, G1	I	Sets the running disparity to negative
TXIDLEA~D	LVCMOS2	R14, R12, U8, T7	I	Forces Tx output to electrical idle
RXDKA~D	SSTL2_I	E17, N15, T1, E1	O	K-code indication for the received symbols
RXDA[7:0]	SSTL2_I	H16, J16, H14, G17, H15, G16, G15, F16	O	Parallel data output bus

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RXDB[7:0] RXDC[7:0] RXDD[7:0]		P13, U16, P14, R15, N14, T16, P15, R16 M2, N3, N1, M4, R1, P3, P2, N4 C2, F4, E4, E3, D3, F3, E2, G4		
TXDKA~D	SSTL2_I	E15, K16, P7, L3	I	K-code indication for the transmitted symbols
TXDA[7:0] TXDB[7:0] TXDC[7:0] TXDD[7:0]	SSTL2_I	C17, C16, E14, D15, D14, E16, C14, D13 N16, L15, N17, M15, M16, K14, L16, L17 R4, T3, R5, U2, P6, T4, R6, U4 H3, H2, J3, H1, J4, J1, K3, K2	I	Parallel data input bus
TXDET/LPBK	LVCMOS2	R11	I	Receiver detection/Loopback
PD[1:0]	LVCMOS2	P10, T11	I	Sets the power states 00 P0, normal operation 01 P0s, low recovery time latency, power saving state 10 P1, longer recovery time(64us max) latency, lower power state 11 P2, lowest power state
RXPLRA~D	LVCMOS2	U15, U13, T9, R8	I	Inverts the polarity on the RXP/RXN

Power and Ground Signals			
Pin Name	**Pin#**	**Type**	**Description**
VDD25	D2, D16, F17, G2, K1, K15, P1, R13, R17, T2, T5, U9, U17	P	2.5V Power Supplies for general I/O
VDD18	C4, C10, C12, D7, H17, J17, L4, M3, T6	P	1.8V Power Supplies for core and bias voltage
VDD12	J14, K4	P	1.25V Reference Voltage for high speed I/O
VSS	D4, D5, F1, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J2, J7, J8, J9, J10, J11, J15, K7, K8, K9, K10, K11, L1, L2, L7, L8, L9, L10, L11, M1, M17, N2, P9, P16, R7, T15, U1, U3, U14	P	Digital ground
VDDPLL	C8	P	1.8V Power Supplies for internal PLL
VSSPLL	D9	P	Ground for internal PLL
VDDRXA~D VSSRXA~D	A17, A13, A9, A5 B17, B13, B9, B5	P	1.8V Power Supplies for receiver part
VDDTXA~D VSSTXA~D	A15, A11, A7, A3 B15, B11, B7, C7, B3	P	1.8V Power Supplies for transceiver part
VSSGR	C15	P	Ground for the guard ring of the SerDes block

Serial Signals			
Pin Name	**Pin#**	**Type**	**Description**
RXNA~D	A16, A12, A8, A4	I	Received serial input, complement
RXPA~D	B16, B12, B8, B4	I	Received serial input, true
RTERM	D8	I	Connects an external 5.1KΩ resistor to ground

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			for calibrating the on-chip termination resistors
TXNA~D	A14, A10, A6, A2	O	Transmitted serial output, complement
TXPA~D	B14, B10, B6, B2	O	Transmitted serial output, true

Other Signals				
Pin Name	**I/O Standard**	**Pin#**	**Type**	**Description**
REFCLKP	Analogue	A1	I	Reference clock signal
REFCLKN	Analogue	B1	I	Reference clock signal
OSC25MO	Crystal	C1	O	Connect to 25MHz crystal when using crystal as the reference clock source
OSC25MI	Crystal/ Oscillator	D1	I	Connect to 25MHz crystal/oscillator when using crystal/oscillator as the reference clock source
TESTC/SMC	LVCMOS2	U11	I	Test clock/SMBus clock
TESTD/SMD	LVCMOS2	T10	I/O	Test data/SMBus data
SCC	LVCMOS2	R10	I	Configures clock input source When SCC=1, the chip clock sources from a pair of differential signals, REFCLKP and REFCLKN, with a nominal frequency of 100 MHz. When SCC=0, the chip clock sources from a crystal at 25MHz.
OPMODE[1:0]	LVCMOS2	U10, R9	I	Operational Mode of the GL9714 00 4 lanes, 8 bit mode 01 2 lanes, 16 bit mode 10 4 lanes, 10 bit mode 11 Internal use only
NC	-	C3, C5, C6, C9, C11, C13, D6, D10, D11, D12, K17	-	No connection

Table 3.5 - Parameter of Buffer I/O

Buffer type	**V_{IH} (Input High Voltage, V)**			**V_{IL} (Input Low Voltage, V)**			**V_{OH} (Output High Voltage, V)**			**V_{OL} (Output Low Voltage, V)**		
	Min	**Norm**	**Max**	**Min**	**Norm**	**Max**	**Min**	**Norm**	**Max**	**Min**	**Norm**	**Max**
LVCMOS2	1.7	-	-	-	-	0.7	2.4	-	-	-	-	0.4
SSTL2	1.57	-	-	-	-	0.93	1.76	-	-	-	-	0.74

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CHAPTER 4 REGISTERS

There are some registers built-in the GL9714 for test purpose. These registers can be accessed through a serial bus interface using pin TESTC and TESTD. Registers at Offset 05h ~ 0Bh are for internal test only. Please be careful to leave them as default values.

4.1 Registers Base Address

Table 4.1 - Base Address for Registers

Mnemonic	Offset	Description	Default
REVID	00h	Revision ID and Auto-calibration Result Register	8'bxxxx0xxx
XCVROPT	01h	Transceiver Option Register	8'hE9
LPBKTEST	02h	BIST and Beacon/Test Data Pattern Register, Part 1	8'h00
BCNPAT2	03h	Beacon/Test Data Pattern Register, Part 2	8'h03
BCNPAT3	04h	Beacon/Test Data Pattern Register, Part 3	8'hFF
-	05h	For internal test only	-
-	06h	For internal test only	-
-	07h	For internal test only	-
-	08h	For internal test only	-
-	09h	For internal test only	-
-	0Ah	For internal test only	-
-	0Bh	For internal test only	-
BT	0Ch	Buffer Test Register	8'h00
SLCDT	0Dh	Serial Loopback and Comma Detect Test Register	8'h00

Notation:

R/W	Read / Write
R/O	Read Only
W/O	Write Only
R/W1C	Read / Write "1" to Clear
R/W/C	Read / Write and hardware automatic Clear

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4.2 Registers Descriptions

Offset 00h – REVID …… Default value = 8'bxxxx0xxx

REV3	REV2	REV1	REV0	BY1	RCAL0	RCAL1	RCAL2
R	R	R	R	R	R	R	R

7-4 REV[3:0] Chip revision code
3 BY1 x1 package
2-0 RCAL[0:2] Calibration result of on-chip termination resistors

Offset 01h – XCVROPT …… Default value = 8'hE9

SW1	SW0	DEM1	DEM0	BW0	BW1	RDEF	FEVAL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 SW[1:0] Swing control of transmitter output
Output Swing (Differential, peak-to-peak)
00 0.6V
01 0.8V
10 1.0V
11 1.2V

5-4 DEM[1:0] De-emphasis control of transmitter output
Amount of De-emphasis
00 No de-emphasis
01 -1.6dB
10 -3.5dB
11 -6.0dB

3-2 BW[0:1] Bandwidth control of clock recovery circuit
Relative Bandwidth
00 1
01 2
10 4
11 Reserved

1 RDEF Disable calibration of on-chip termination resistors and leave the resistors to their default value

0 FEVAL Force calibration of on-chip termination resistors
When **RDEF=**0, writing a one to this bit will make the resistors re-calibrated. This bit is auto-cleared and always read as zero.

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Offset 02h – LPBKTEST ……..……. Default value = 8'h00

BIST0	BIST1	BIST2	--	BCN19	BCN18	BCN17	BCN16
R/W	R/W	R/W	--	R/W	R/W	R/W	R/W

7-5 BIST[0:2] Select of built-in test pattern

Bit	Pattern	
00x	BIST disabled	
100	0000000000	0000000000
010	1111111111	1111111111
110	0101010101	0101010101
101	0011111010	1010101010
	1100000101	0101010101
011	0011111010	1010**0***01010
	1100000101	0101**1***10101
111	PRBS pattern	

It should be noted that the expected pattern while BIST[0:2]=011 is the same as BIST[0:2]=101. But when coming out of the transmitter, the two bits with "*" in BIST[0:2]=011 are different from BIST[0:2]=101. As a result, even when there is no bit error, there will be bit errors intentionally introduced to verify the BIST circuit is functional.

4 RESERVED -

3-0 BCN[19:16] Data pattern for beacon and **TXTEST**

Offset 03h – BCNPAT2 ……. Default value = 8'h03

BCN15	BCN14	BCN13	BCN12	BCN11	BCN10	BCN9	BCN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BCN[15:8] Data pattern for beacon and **TXTEST**

Offset 04h – BCNPAT3 ……. Default value = 8'hFF

BCN7	BCN6	BCN5	BCN4	BCN3	BCN2	BCN1	BCN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BCN[7:0] Data pattern for beacon and **TXTEST**

Offset 0Ch – BT ……..……..……. Default value = 8'h00

--	--	DDR	--	TXTEST	--	SKPDEL	SKPADD
--	--	R/W	--	R/W	--	R/W	R/W

7-6 RESERVED -

5 DDR Enable DDR at PIPE interface and make PCLK = 125MHz @ 8/10-bit mode

3 TXTEST Enable transmitter test with data pattern BCN[19:0], which are programmed in REG02h, 03h and 04h

1 SKPDEL Enable SKP deleting test of SKP ordered sets

0 SKPADD Enable SKP adding test of SKP ordered sets

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Offset 0Dh – SLCDT ……..…….…….. Default value = 8'h00

SLPBKA	SLPBKB	SLPBKC	SLPBKD	FENCDA	FENCDB	FENCDC	FENCDD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 SLPBKA Enable serial loopback of lane A
6 SLPBKB Enable serial loopback of lane B
5 SLPBKC Enable serial loopback of lane C
4 SLPBKD Enable serial loopback of lane D
3 FENCDA Force comma detect of lane A
2 FENCDB Force comma detect of lane B
1 FENCDC Force comma detect of lane C
0 FENCDD Force comma detect of lane D

Offset 14h – SECNTA ……..…….…….. Default value = 8'h00

SECNTA7	SECNTA6	SECNTA5	SECNTA4	SECNTA3	SECNTA2	SECNTA1	SECNTA0
R	R	R	R	R	R	R	R

7-0 SECNTA[7:0] Error count of SLPBKA.

Offset 15h – SECNTB ……..…….…….. Default value = 8'h00

SECNTB7	SECNTB6	SECNTB5	SECNTB4	SECNTB3	SECNTB2	SECNTB1	SECNTB0
R	R	R	R	R	R	R	R

7-0 SECNTB[7:0] Error count of SLPBKB.

Offset 16h – SECNTC ……..…….…….. Default value = 8'h00

SECNTC7	SECNTC6	SECNTC5	SECNTC4	SECNTC3	SECNTC2	SECNTC1	SECNTC0
R	R	R	R	R	R	R	R

7-0 SECNTC[7:0] Error count of SLPBKC.

Offset 17h – SECNTD ……..…….…….. Default value = 8'h00

SECNTD7	SECNTD6	SECNTD5	SECNTD4	SECNTD3	SECNTD2	SECNTD1	SECNTD0
R	R	R	R	R	R	R	R

7-0 SECNTD[7:0] Error count of SLPBKD.

PS: Please write "0" to the unused bits when programming a register.

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4.3 SMBus Protocol

GL9714 registers are programmed by System Management Bus (SMBus). Fig. 4.1 shows the SMBus topology. The V_{DD} power is 2.5V +/- 10% and the pull up resistor is 1KΩ. Both SMBCLK and SMBDAT lines are bi-directional, connected to 2.5V supply voltage through a pull-up resistor. The operating frequency is 10~100KHz and the SMBus address of GL9714 is 7'h2C.

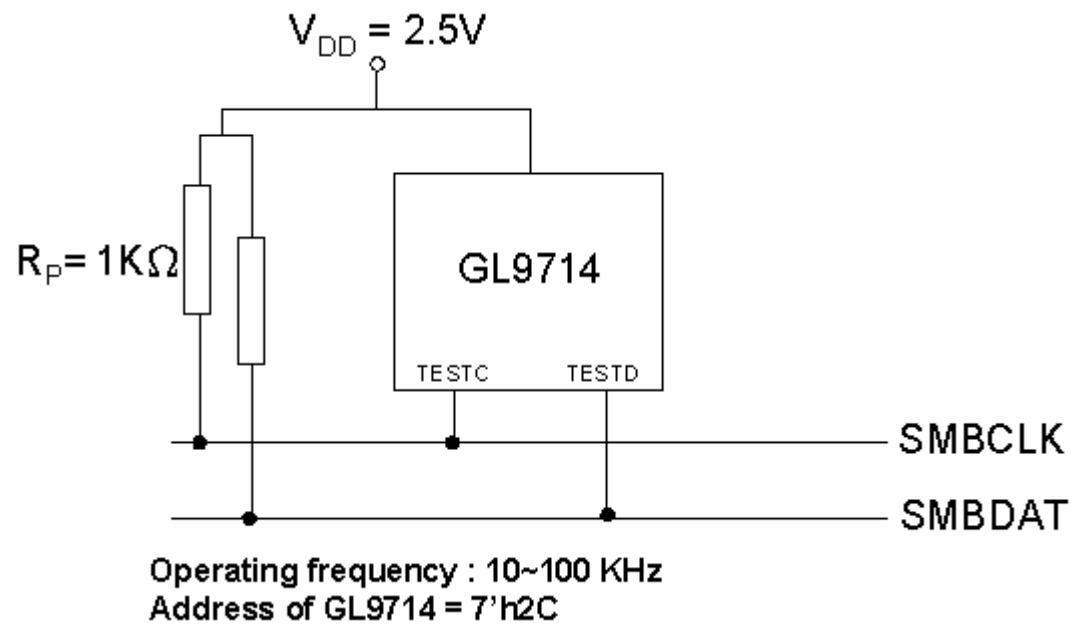

Figure 4.1 – SMBus Topology of GL9714

SMBus uses fixed voltage levels to define the logic "ZERO" and logic "ONE" on the bus respectively. The data on SMBDAT must be stable during the "HIGH" period of the clock. Data can change state only when SMBCLK is low. Fig. 4.2 illustrates the relationships.

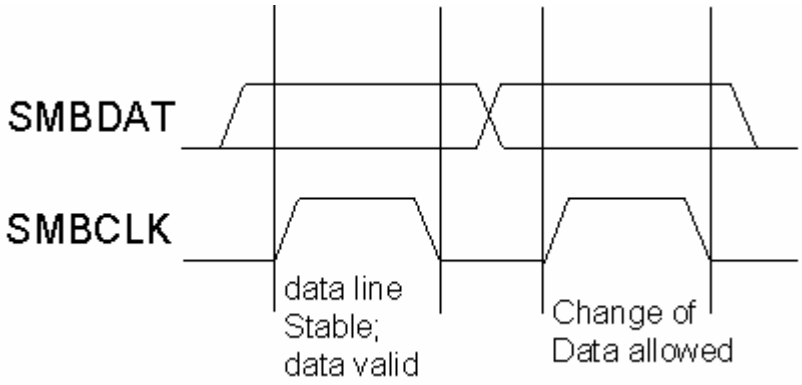

Figure 4.2 – Data Validity

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Two unique bus situations define a message START and STOP condition.
1. A HIGH to Low transition of the SMBDAT line while SMBCLK is HIGH indicates a message START condition.
2. A LOW to HIGH transition of the SMBDAT line while SMBCLK is HIGH defines a message STOP condition.

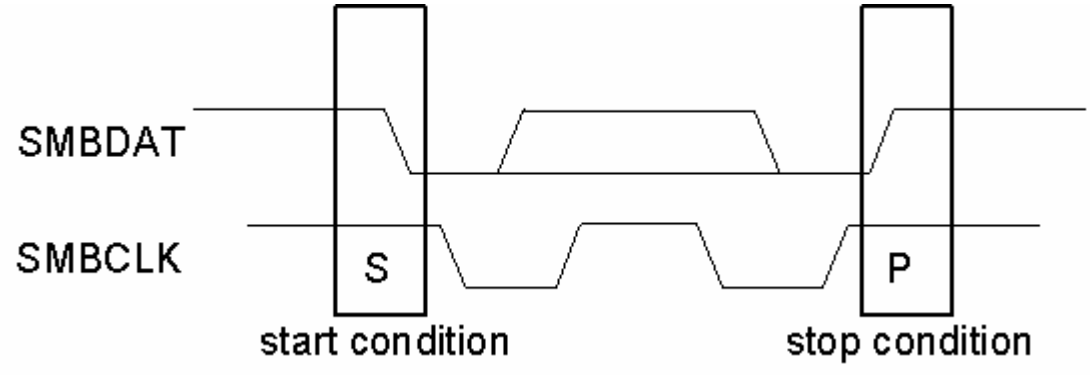

Figure 4.3 – START and STOP Condition

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an acknowledge bit. Bytes are transferred with the most significant bit (MSB) first. Fig. 4.4 illustrates the positioning of acknowledge (ACK) and not acknowledge (NACK) pulses relative to other data.

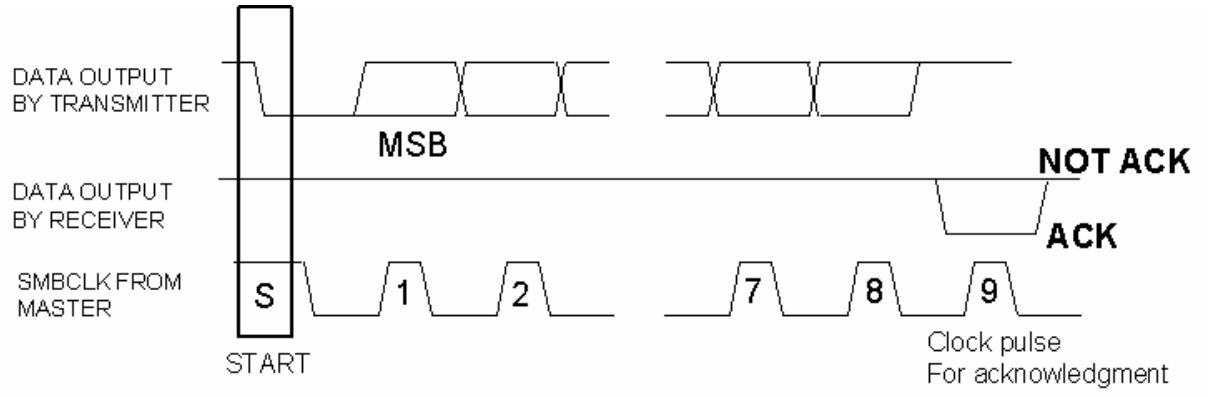

Figure 4.4 – ACK and NACK Signaling of SMBus

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Below is a key to the protocol diagrams.

S	Start Condition
Sr	Repeated Start Condition
Rd	Read (bit value of 1)
Wr	Write (bit value of 0)
x	Shown under a field indicates that that field is required to have the value of 'x'
A	Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK)
P	Stop Condition
☐	Master-to-GL9714
■	GL9714-to-Master

Figure 4.5 – SMBus Packet Protocol Diagram Element Key

The first byte of a Write Byte access is the command code. The next one byte is the data to be written. In this example the master asserts GL9714's address followed by the write bit. GL9714 acknowledges and the master delivers the command code. GL9714 again acknowledges before the master sends the data byte. GL9714 acknowledges the data byte, and the entire transaction is finished with a STOP condition.

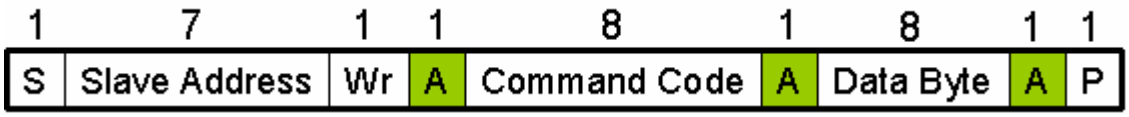

Figure 4.6 – Write Byte Protocol

Reading data is slightly more complicated than writing data. First the host must write a command to GL9714. Then it must follow that command with a repeated START condition to denote a read from GL9714's address. GL9714 then returns one byte of data.
Note that there is no STOP condition before the repeated START condition, and that a NACK signified the end of the read transfer.

Figure 4.7 – Read Byte Protocol

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GL9714 requires a minimum time (16us) to reach the steady state after power on. So the master must start programming at least 16us later after power on.

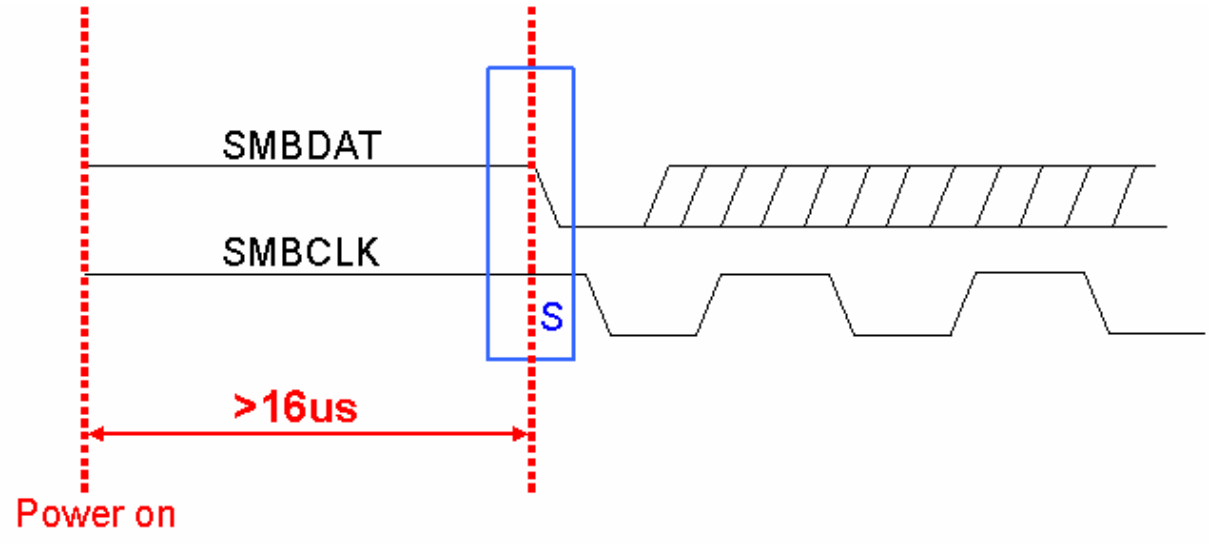

Figure 4.8 – The Minimum Wait Time from Power on to Programming Registers

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CHAPTER 5 BLOCK DIAGRAM

5.1 Simplified Diagram

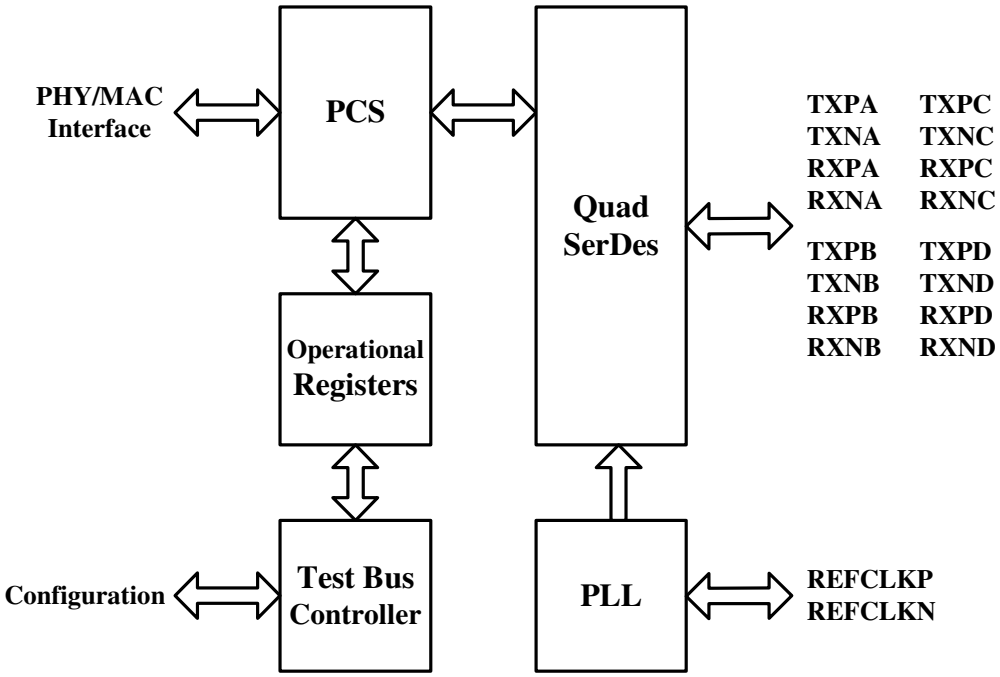

Figure 5.1 - Simplified Diagram

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5.2 Transmitter Data Path Per Lane

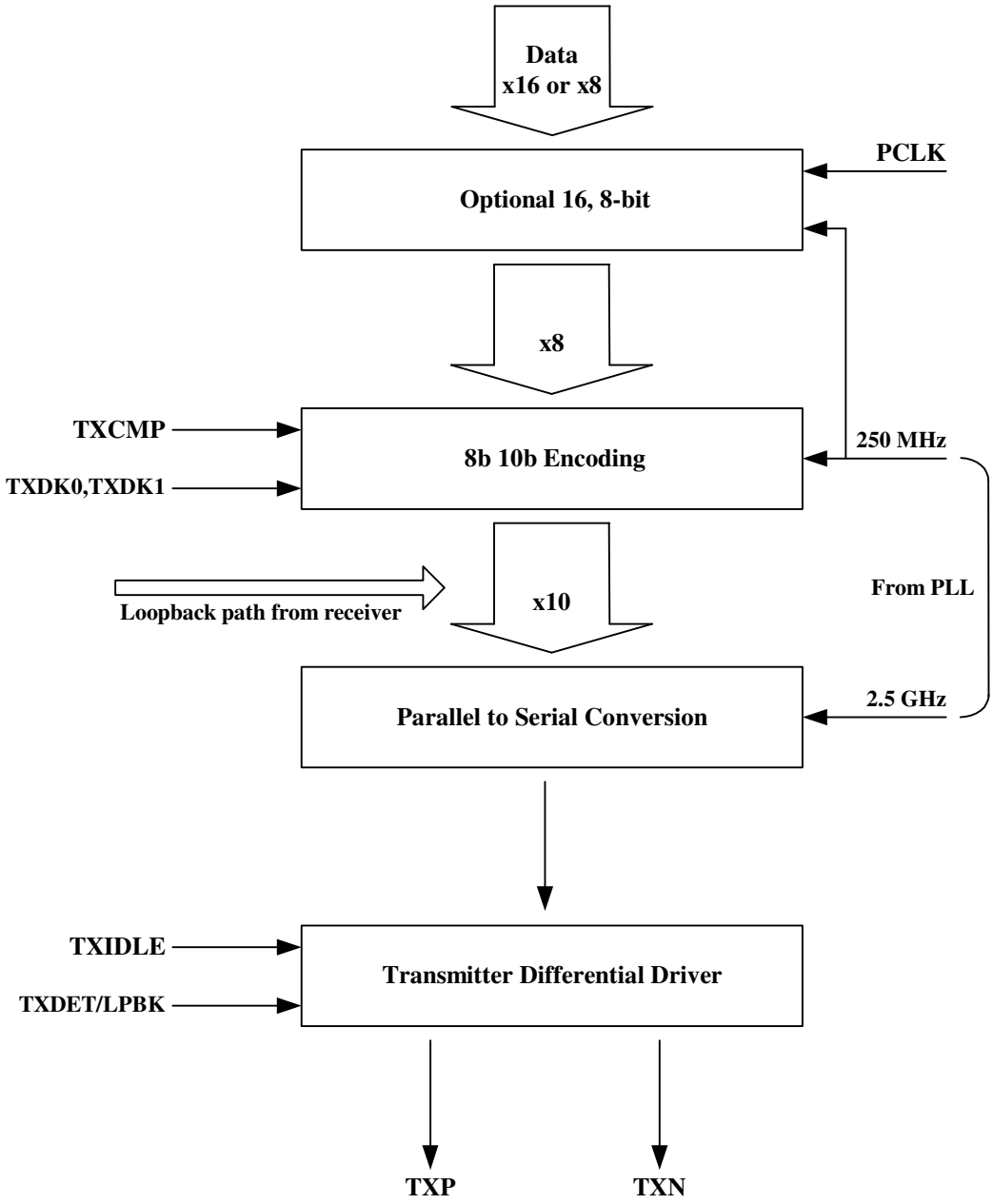

Figure 5.2 - Transmitter Data Path per Lane

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5.3 Receiver Data Path Per Lane

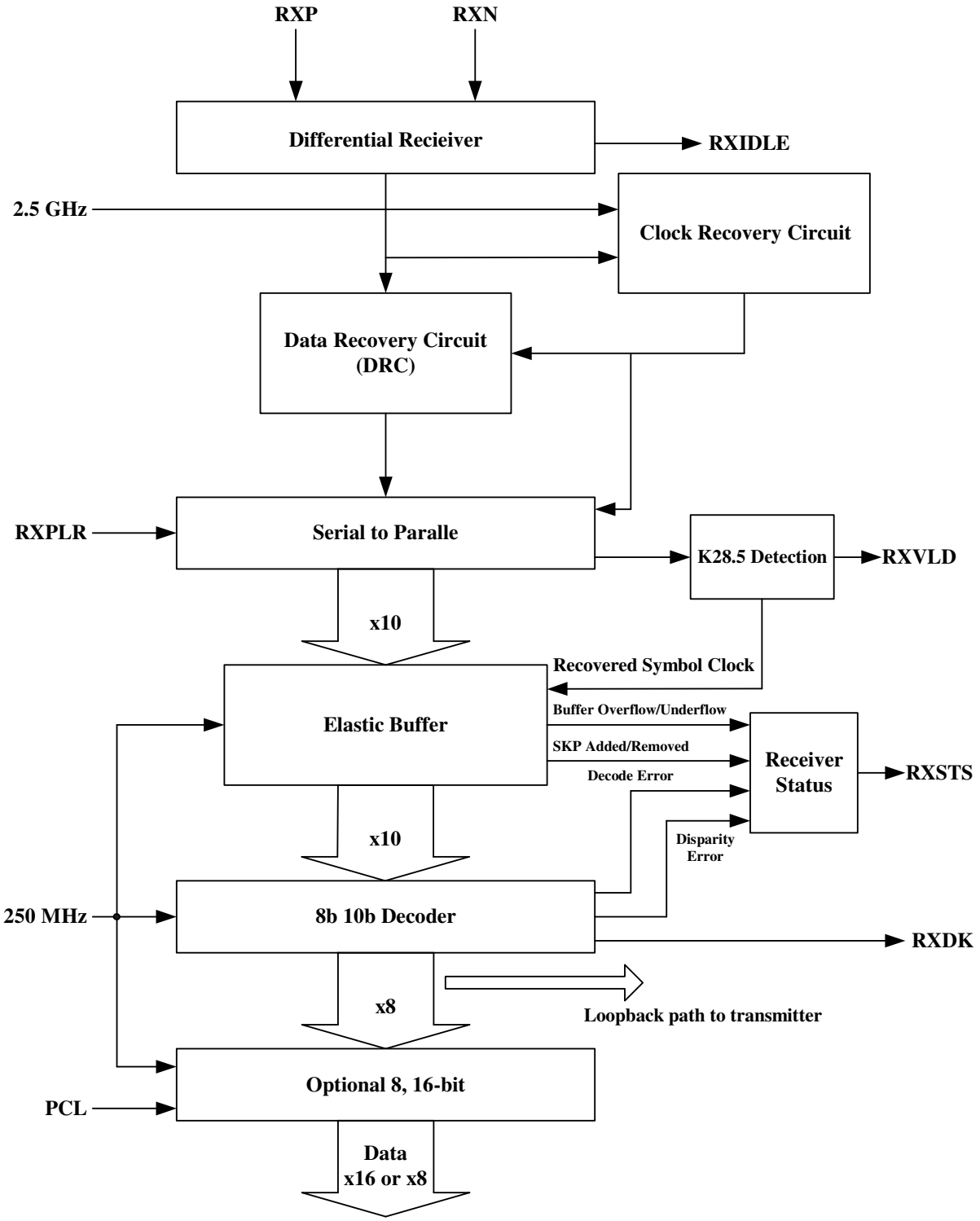

Figure 5.3 - Receiver Data Path per Lane

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CHAPTER 6 FUNCTION DESCRIPTION

6.1 Clock and Reset

The clock source of the GL9714 comes externally from either the 100 MHz differential clock pair or the 25MHz crystal, which is selectable by pin SCC. The GL9714 uses the clock source with its PLL to generate the 2.5 GHz bit rate for transmitting and receiving.

The GL9714 also drives a clock output for the synchronization of MAC interface. Since the MAC interface can be configured to 8-bit and 16-bit mode, the clock, PCLK, runs at 250 MHz for 8-bit mode and 125 MHz for 16-bit mode. The MAC should use the rising edge of the clock to send and receive parallel data.

To initialize the GL9714, the MAC should assert the reset of the GL9714 to low. While the reset is asserted, the MAC should also make TXDET/LPBK deasserted, TXIDLEx asserted, TXCMPx deasserted, RXPLRx deasserted and PD[1:0] = P1. When the GL9714 senses it reset asserted, it will drive its PHYSTS high immediately. After the reset deasserted, the GL9714 requires typically 16.7us for internal PLL stable and then transitions its PHYSTS to low. When MAC deasserts the reset, it should monitor the state of PHYSTS to make sure the GL9714 is ready for normal operation.

6.2 Receiver Detection

The receiver detection can only be performed while the GL9714 is in P1 state. To instruct the GL9714 to enter a receiver detection sequence, the MAC asserts TXDET/LPBK and hold it asserted until the GL9714 asserts PHYSTS for response. While finishing the receiver detection, the GL9714 will assert PHYSTS and present a appropriate value to RXSTSx[2:0] to signal a detection completion. When the MAC detects PHYSTS asserted, it knows the detection result from RXSTSx[2:0] and can deassert TXDET/LPBK.

6.3 Beacon Transmitting and Detection

Beacon transmitting is required for the GL9714 in P2 state to wake up the receiver in the other side of the link. When the GL9714 is in P2 state, the MAC can deassert TXIDLEx to instruct the GL9714 to repeatedly transmit a beacon.

For the beacon receiving side, if the GL9714 receives a beacon, it will transition RXIDLEx to low to indicate an exit from electrical idle. When the GL9714 is in P2 state and MAC senses the RXIDLEx transitioned from high to low, it knows a beacon has been detected.

6.4 Receiver Status Report

- **Add and Remove a SKP**
  The GL9714 implements an elastic buffer to compensate the clock rate difference between the recovery clock and its transmit clock. While receiving a SKP ordered-set, compliant to PCI Express Base specification REV. 1.0a, the GL9714 can insert or remove one SKP symbol in the SKP ordered-set to avoid the buffer overrun or underrun. Whenever adding or removing a SKP symbol, the GL9714 will signal PHYSTS and corresponding RXSTS[2:0] to MAC.

SKP Ordered-Set Received	RXSTS Code
Add a SKP	001b
Remove a SKP	010b

- **Receiver Detected**

Detected Result	RXSTS code
Receiver not present	000b
Receiver present	011b

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- **8B/10B Decode Error**
  When the GL9714 decodes the received 10-bit symbol and detects an error code which does not correspond to any valid data, it will replace the code with an EDB symbol, assert PHYSTS and encode RXSTSx[2:0] with the values of decode error status, 3'b100.

- **Elastic Buffer Overrun and Underrun**
  When the overrun or underrun of the elastic buffer occurs, the GL9714 will assert PHYSTS and encode RXSTSx[2:0] with the values of decode error status.

Elastic Buffer	RXSTS Code
Overrun	101b
Underrun	110b

  In the case of elastic buffer overrun, the GL9714 drops the symbol. For the elastic buffer underrun, the GL9714 inserts the EDB symbol. The PHYSTS and RXSTSx[2:0] are presented on the MAC interface during the clock cycle where GL9714 drops or inserts the symbol.

- **Disparity Errors**
  To report a disparity error detected, the GL9714 asserts PHYSTS and encodes RXSTSx[2:0] with the values of decode error status, 3'b111.

6.5 Loopback

The GL9714 supports a Loopback mode to re-transmit its received data. When the MAC sets the GL9714 in P0 state and asserts TXDET/LPBK, the GL9714 enters a Loopback. In Loopback, the GL9714 transmits data from it received data instead of MAC interface. Meanwhile, it presents the received data on the MAC interface as normal operation.

When set into Loopback mode and acting as a Loopback slave according to the PCI Express Base Specification Rev. 1.0a, the GL9714 received data from the Loopback master. If the master intends to end the Loopback, it sends an electrical idle ordered-set to the GL9714. When the MAC detects the electrical idle ordered-set, it de-asserts TXDET/LPBK and asserts TXIDLE to instruct the GL9714 to stop Loopback. The MAC should take care the GL9714 has retransmit at least three bytes of the electrical idle before it makes the GL9714's transmitter into electrical idle.

6.6 Polarity Inversion

The GL9714 supports lane polarity inversion. While pin RXPLRx asserted, the GL9714 inverts its received data on the MAC interface.

6.7 Setting Negative Disparity

To set the running disparity to negative, the MAC asserts TXCMPx for one PCLK cycle that matches with the data that is to be transmitted where running disparity is negative.

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6.8 Behavior Summary

PD[1:0]	TXDET/LPBK	TXIDLEx	Behavior
P0	0	0	GL9714 is transmitting data from MAC interface normally.
	0	1	GL9714 is not transmitting and is in electrical idle.
	1	0	GL9714 enters Loopback mode.
	1	1	Illegal
P0S	X	0	Illegal
	X	1	GL9714 is not transmitting and is in electrical idle.
P1	X	0	Illegal
	0	1	GL9714 is idle.
	1	1	GL9714 performs a receiver detection.
P2	X	0	GL9714 transmits a beacon.
	X	1	GL9714 is idle.

6.9 Power Saving Support

The GL9714 supports four power states including P0, P0s, P1 and P2 and can be controlled to perform Active State Power Management on a PCI Express link. P0 is the normal operational state where data and control packets can be transmitted and received. When directed from P0 to a lower power state, the GL9714 can immediately take appropriate power saving actions. The power saving scheme of the GL9714 for various power down states is listed in the table below.

PD[1:0]	Transmitter	Receiver	PLL	PCLK Output
P0	On	On	On	On
P0s	High-impedance Electrical Idle	On	On	On
P1	High-impedance Electrical Idle	Off but exit from Electrical Idle is detectable	On	On
P2	High-impedance Electrical Idle (Capable of transmitting a Beacon)	Off but exit from Electrical Idle is detectable	Off	Off

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6.10 Operation Mode and Multi-Functional Pins

There are four modes for GL9714 operation which is selected by pin OPMODE[1:0].

Mode	[1]	[0]	Description
1	0	0	4 lanes, 8 bit mode
2	0	1	2 lanes, 16 bit mode
3	1	0	4 lanes, 10 bit mode
4	1	1	For scan test only

Mode 1: The GL9714 is configured into an x4 lane, 8-bit parallel bus and acts as a 4-lane PCI Express PHY. The parallel bus is synchronous with PCLK at 250 MHz. By transitioning both TXCMPx and TXIDLEx to high for individual lane, the GL9714 in this mode is able to behave as an x1 or x2 PHY.

Mode 2: The GL9714 acts as a 2-lane PHY with a 16-bit parallel interface at 125 MHz. In this mode, only lane B and lane C are activated. Again, by disabling either lane using TXCMPx and TXIDLEx, the GL9714 can be configured into an x1 PHY with16-bit parallel bus.

Mode 3: The GL9714 is configured as a quad SerDes with 10-bit parallel bus.

Mode 4: For scan test only

Table 6.1 - Pin Functions

Pin Number	Mode 1	Mode 2	Mode 3
T14	PCLK(O)	PCLK(O)	TBC(O)
C17	TXDA7(I)	TXDB15(I)	TDA7(I)
C16	TXDA6(I)	TXDB14(I)	TDA6(I)
E14	TXDA5(I)	TXDB13(I)	TDA5(I)
D15	TXDA4(I)	TXDB12(I)	TDA4(I)
D14	TXDA3(I)	TXDB11(I)	TDA3(I)
E16	TXDA2(I)	TXDB10(I)	TDA2(I)
C14	TXDA1(I)	TXDB9(I)	TDA1(I)
D13	TXDA0(I)	TXDB8(I)	TDA0(I)
N16	TXDB7(I)	TXDB7(I)	TDB7(I)
L15	TXDB6(I)	TXDB6(I)	TDB6(I)
N17	TXDB5(I)	TXDB5(I)	TDB5(I)
M15	TXDB4(I)	TXDB4(I)	TDB4(I)
M16	TXDB3(I)	TXDB3(I)	TDB3(I)
K14	TXDB2(I)	TXDB2(I)	TDB2(I)
L16	TXDB1(I)	TXDB1(I)	TDB1(I)
L17	TXDB0(I)	TXDB0(I)	TDB0(I)
R4	TXDC7(I)	TXDC15(I)	TDC7(I)
T3	TXDC6(I)	TXDC14(I)	TDC6(I)
R5	TXDC5(I)	TXDC13(I)	TDC5(I)
U2	TXDC4(I)	TXDC12(I)	TDC4(I)
P6	TXDC3(I)	TXDC11(I)	TDC3(I)
T4	TXDC2(I)	TXDC10(I)	TDC2(I)
R6	TXDC1(I)	TXDC9(I)	TDC1(I)
U4	TXDC0(I)	TXDC8(I)	TDC0(I)
H3	TXDD7(I)	TXDC7(I)	TDD7(I)

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H2	TXDD6(I)	TXDC6(I)	TDD6(I)
J3	TXDD5(I)	TXDC5(I)	TDD5(I)
H1	TXDD4(I)	TXDC4(I)	TDD4(I)
J4	TXDD3(I)	TXDC3(I)	TDD3(I)
J1	TXDD2(I)	TXDC2(I)	TDD2(I)
K3	TXDD1(I)	TXDC1(I)	TDD1(I)
K2	TXDD0(I)	TXDC0(I)	TDD0(I)
E15	TXDKA(I)	TXDKB1(I)	TDA8(I)
K16	TXDKB(I)	TXDKB0(I)	TDB8(I)
P7	TXDKC(I)	TXDKC1(I)	TDC8(I)
L3	TXDKD(I)	TXDKC0(I)	TDD8(I)
R14	TXIDLEA(I)		TXIDLEA(I)
R12	TXIDLEB(I)	TXIDLEB(I)	TXIDLEB(I)
U8	TXIDLEC(I)	TXIDLEC(I)	TXIDLEC(I)
T7	TXIDLED(I)		TXIDLED(I)
F15	TXCMPA(I)		TDA9(I)
L14	TXCMPB(I)	TXCMPB(I)	TDB9(I)
R3	TXCMPC(I)	TXCMPC(I)	TDC9(I)
G1	TXCMPD(I)		TDD9(I)
U15	RXPLRA(I)		RXPLRA(I)
U13	RXPLRB(I)	RXPLRB(I)	RXPLRB(I)
T9	RXPLRC(I)	RXPLRC(I)	RXPLRC(I)
R8	RXPLRD(I)		RXPLRD(I)
H16	RXDA7(O)	RXDB15(O)	RDA7(O)
J16	RXDA6(O)	RXDB14(O)	RDA6(O)
H14	RXDA5(O)	RXDB13(O)	RDA5(O)
G17	RXDA4(O)	RXDB12(O)	RDA4(O)
H15	RXDA3(O)	RXDB11(O)	RDA3(O)
G16	RXDA2(O)	RXDB10(O)	RDA2(O)
G15	RXDA1(O)	RXDB9(O)	RDA1(O)
F16	RXDA0(O)	RXDB8(O)	RDA0(O)
P13	RXDB7(O)	RXDB7(O)	RDB7(O)
U16	RXDB6(O)	RXDB6(O)	RDB6(O)
P14	RXDB5(O)	RXDB5(O)	RDB5(O)
R15	RXDB4(O)	RXDB4(O)	RDB4(O)
N14	RXDB3(O)	RXDB3(O)	RDB3(O)
T16	RXDB2(O)	RXDB2(O)	RDB2(O)
P15	RXDB1(O)	RXDB1(O)	RDB1(O)
R16	RXDB0(O)	RXDB0(O)	RDB0(O)
M2	RXDC7(O)	RXDC15(O)	RDC7(O)
N3	RXDC6(O)	RXDC14(O)	RDC6(O)
N1	RXDC5(O)	RXDC13(O)	RDC5(O)
M4	RXDC4(O)	RXDC12(O)	RDC4(O)
R1	RXDC3(O)	RXDC11(O)	RDC3(O)
P3	RXDC2(O)	RXDC10(O)	RDC2(O)

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P2	RXDC1(O)	RXDC9(O)	RDC1(O)
N4	RXDC0(O)	RXDC8(O)	RDC0(O)
C2	RXDD7(O)	RXDC7(O)	RDD7(O)
F4	RXDD6(O)	RXDC6(O)	RDD6(O)
E4	RXDD5(O)	RXDC5(O)	RDD5(O)
E3	RXDD4(O)	RXDC4(O)	RDD4(O)
D3	RXDD3(O)	RXDC3(O)	RDD3(O)
F3	RXDD2(O)	RXDC2(O)	RDD2(O)
E2	RXDD1(O)	RXDC1(O)	RDD1(O)
G4	RXDD0(O)	RXDC0(O)	RDD0(O)
E17	RXDKA(O)	RXDKB1(O)	RDA8(O)
N15	RXDKB(O)	RXDKB0(O)	RDB8(O)
T1	RXDKC(O)	RXDKC1(O)	RDC8(O)
E1	RXDKD(O)	RXDKC0(O)	RDD8(O)
P12	RXVLDA(O)		RXVLDA(O)
P11	RXVLDB(O)	RXVLDB(O)	RXVLDB(O)
U7	RXVLDC(O)	RXVLDC(O)	RXVLDC(O)
U6	RXVLDD(O)		RXVLDD(O)
D17	RXSTSA2(O)		RBCA(O)
G14	RXSTSA1(O)		RXPRSNTA(O)
F14	RXSTSA0(O)		RDA9(O)
T17	RXSTSB2(O)	RXSTSB2(O)	RBCB(O)
M14	RXSTSB1(O)	RXSTSB1(O)	RXPRSNTB(O)
P17	RXSTSB0(O)	RXSTSB0(O)	RDB9(O)
P4	RXSTSC2(O)	RXSTSC2(O)	RBCC(O)
R2	RXSTSC1(O)	RXSTSC1(O)	RXPRSNTC(O)
P5	RXSTSC0(O)	RXSTSC0(O)	RDC9(O)
G3	RXSTSD2(O)		RBCD(O)
F2	RXSTSD1(O)		RXPRSNTD(O)
H4	RXSTSD0(O)		RDD9(O)
U5	PHYSTS(O)	PHYSTS(O)	PHYSTS(O)
T13	RXIDLEA(O)		RXIDLEA(O)
T12	RXIDLEB(O)	RXIDLEB(O)	RXIDLEB(O)
T8	RXIDLEC(O)	RXIDLEC(O)	RXIDLEC(O)
P8	RXIDLED(O)		RXIDLED(O)

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CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 DC Electrical Characteristics

Table 7.1 - DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VDD25	PHY Interface Voltage	2.375	2.5	2.625	V
VDD18	Core Voltage	1.71	1.8	1.89	V
VDD12	Reference Voltage for PHY Interface	1.1875	1.25	1.3125	V
VDDTXA VDDTXB VDDTXC VDDTXD	Voltage for Transmitters	1.71	1.8	1.89	V
VDDRXA VDDRXB VDDRXC VDDRXD	Voltage for Receivers	1.71	1.8	1.89	V
VDDPLL	Voltage for PLL	1.71	1.8	1.89	V

7.2 Transmit and Receive Latency Time

Table 7.2 - Transmit and Receive Latency Time

Symbol	Parameter	Min	Typ	Max	Unit
T_{TX-LAT}	Transmit Latency, time for data moving from MAC interface (PCLK rising edge) to TX serial lines (the first bit of 10-bit symbol)	25	-	30	ns
T_{RX-LAT}	Receive Latency, time for data moving from RX serial lines (the first bit of 10-bit symbol) to MAC interface (PCLK rising edge)	48	-	54	ns

7.3 Transition Time of Power State

Table 7.3 – Transition Time of Power State

Symbol	Parameter	Min	Typ	Max	Unit
T_{P0S-P0}	Time for PHY to return to P0, after having been in P0s. Time is measured when PD[1:0] are set to P0 until the PHY asserts PHYSTS	52	-	74	ns
T_{P1-P0}	Time for PHY to return to P0, after having been in P1. Time is measured when PD[1:0] are set to P0 until the PHY asserts PHYSTS	52	-	74	ns
T_{P2-P1}	Time for PHY to return to P0, after having been in P2. Time is measured when PD[1:0] are set to P0 until the PHY asserts PHYSTS	16	-	17	µs
T_{P0-P0S}	Time for PHY to return to P0s, after having been in P0. Time is measured when PD[1:0] are set to P0 until the PHY asserts PHYSTS	52	-	74	ns
T_{P0-P1}	Time for PHY to return to P1, after having been	52	-	74	ns

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	in P0. Time is measured when PD[1:0] are set to P0 until the PHY asserts PHYSTS				
T_{P0-P2}	Time for PHY to return to P2, after having been in P0. Time is measured when PD[1:0] are set to P0 until the PHY asserts PHYSTS	16	-	17	µs

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7.4 Power Consumption

- **Power Consumption with 2-Lanes and 4-Lanes Operation**

Table 7.4 – Typical Power Consumption with 2-Lanes, 4-Lanes, and 1.2V Differential Peak to Peak Output Voltage

Current at 2.5V (mA)	Current at Analogue 1.8V (mA)	Current at Digital 1.8V (mA)	Current at Reference Voltage 1.25V (mA)	Operation Condition	Power State	Operation Mode	Power Consumption (mW)
184	285	128	0	All on	P0	8-bit @250MHz PCLK, 4-Lanes	1203.4
14	207	89	0	PLL on TX idle RX on	P0s	8-bit @250MHz PCLK, 4-Lanes	567.8
14	174	48	0	PLL on TX idle RX idle	P1	8-bit @250MHz PCLK, 4-Lanes	434.6
9	146	10	0	PLL off TX idle RX idle	P2	8-bit @3.13MHz PCLK, 4-Lanes	303.3
107	161	81	0	All on	P0	16-bit @125MHz PCLK, 2-Lanes	703.1
17	117	65	0	PLL on TX idle RX on	P0s	16-bit @125MHz PCLK, 2-Lanes	370.1
17	101	45	0	PLL on TX idle RX idle	P1	16-bit @125MHz PCLK, 2-Lanes	305.3
9	74	9	0	PLL off TX idle RX idle	P2	16-bit @1.56MHz PCLK, 2-Lanes	171.9

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- **Power Consumption with Single-Lane Operation**

Table 7.5 – Typical Power Consumption with Single-Lane and 1.2V Differential Peak to Peak Output Voltage

Current at 2.5V (mA)	Current at Analogue 1.8V (mA)	Current at Digital 1.8V (mA)	Current at Reference Voltage 1.25V (mA)	Operation Condition	Power State	Operation Mode	Power Consumption (mW)
51	90	65	0	All on	P0	8-bit @250MHz PCLK	406.5
10	72	56	0	PLL on TX idle RX on	P0s	8-bit @250MHz PCLK	255.4
10	65	45	0	PLL on TX idle RX idle	P1	8-bit @250MHz PCLK	223
6	37	7	0	PLL off TX idle RX idle	P2	8-bit @3.13MHz PCLK	94.2
59	90	57	0	All on	P0	16-bit @125MHz PCLK	412.1
12	71	49	0	PLL on TX idle RX on	P0s	16-bit @125MHz PCLK	246
12	64	38	0	PLL on TX idle RX idle	P1	16-bit @1.56MHz PCLK	213.6
6	36	6	0	PLL off TX idle RX idle	P2	16-bit @125MHz PCLK	90.6

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7.5 Differential Transmitter and Receiver Serial Output

- **Transmitter Serial Output**

Table 7.6 – Transmitter Serial Output

Symbol	Parameter	Min	Typ	Max	Unit
UI	Unit interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential peak to peak output voltage	0.8	-	1.2	V
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum TX eye width	0.7	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	-	0.15	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX output rise/fall time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC peak common mode output voltage	-	-	20	mV
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0	-	100	mV
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection	-	-	600	mV
$V_{TX-DC-CM}$	The TX DC common mode voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX short circuit current limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	50	-	-	UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	-	-	20	UI
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential return loss	12	-	-	dB
RL_{TX-CM}	Common mode return loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC differential TX impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-lane output skew	-	-	500 + 2UI	ps
C_{TX}	AC coupling capacitor	75	-	200	nF
Tcrosslink	Crosslink random timeout	0	-	1	ms

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- **Receiver Serial Output**

Table 7.7 – Receiver Serial Output

Symbol	Parameter	Min	Typ	Max	Unit
UI	Unit interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential input peak to peak voltage	0.175	-	1.2	V
T_{RX-EYE}	Minimum receiver eye width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC peak common mode input voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential return loss	15	-	-	dB
RL_{RX-CM}	Common mode return loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	Ω
Z_{RX-DC}	DC input impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	-	-	10	ms
$L_{RX-SKEW}$	Total skew	-	-	20	ns

7.6 Recommended Operating Conditions

Table 7.8 – Temperature Range

Symbol	Parameter	Min	Typ	Max	Unit
$T_{JUNCTOIN}$	Junction operating temperature range	0	-	125	℃
T_A	Operating ambient temperature range	0	-	75	℃
T_{STG}	Storage temperature range	-40	-	150	℃

Table 7.9 – Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA} (0 m/s)	Thermal resistance from junction to ambient PS: "(x m/s)" means the air flow velocity (JEDEC JESD51-6 moving air, maximum reflow temperature for SMT is 255℃~260℃)	-	33.2	-	℃/W
θ_{JA} (1 m/s)		-	28.7	-	℃/W
θ_{JA} (2 m/s)		-	27.5	-	℃/W
Ψ_{JT}	Thermal characterization parameter from junction-to-top center (JEDEC JESD51-2 still air, maximum reflow temperature for SMT is 255℃~260℃)	-	0.39	-	℃/W
θ_{JC}	Thermal resistance from junction to case (JEDEC JESD51-2 still air, maximum reflow temperature for SMT is 255℃~260℃)	-	12.3	-	℃/W

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CHAPTER 8 PIPE TIMING CHARACTERISTICS

8.1 Input Setup, Hold Time and Output Timing

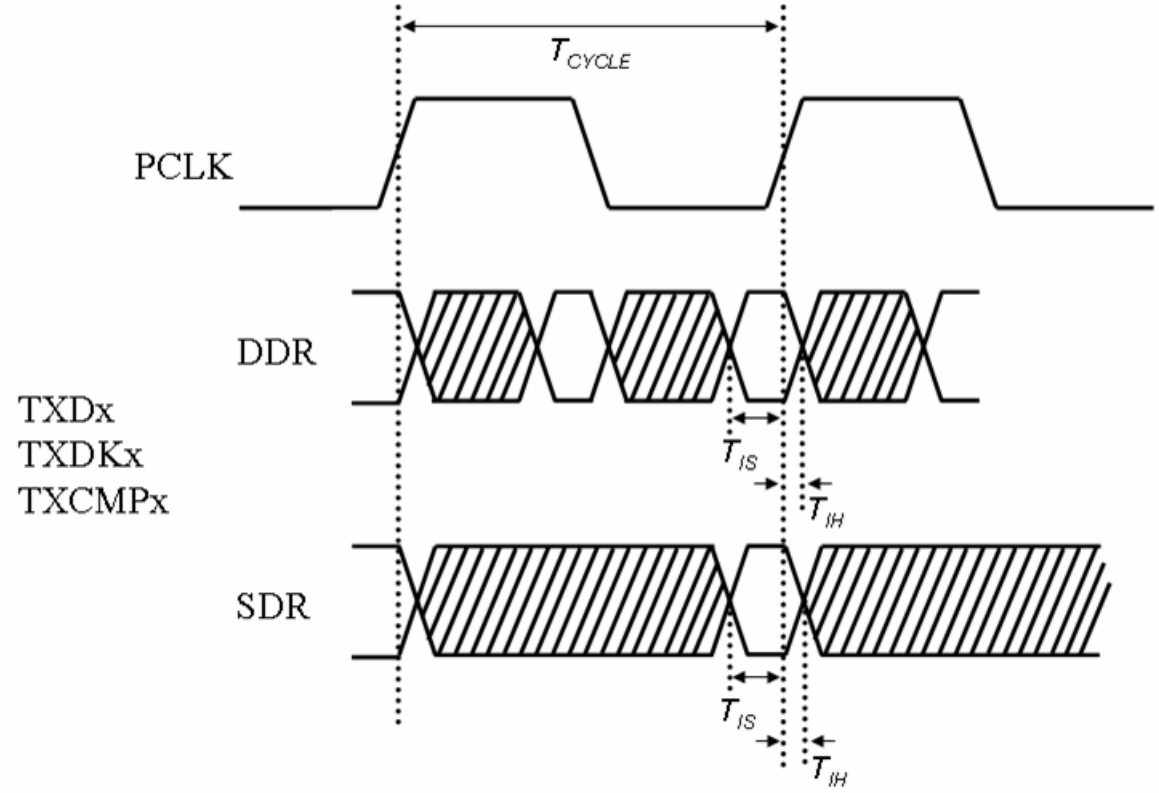

Figure 8.1 – Definition of Input Setup and Hold Time

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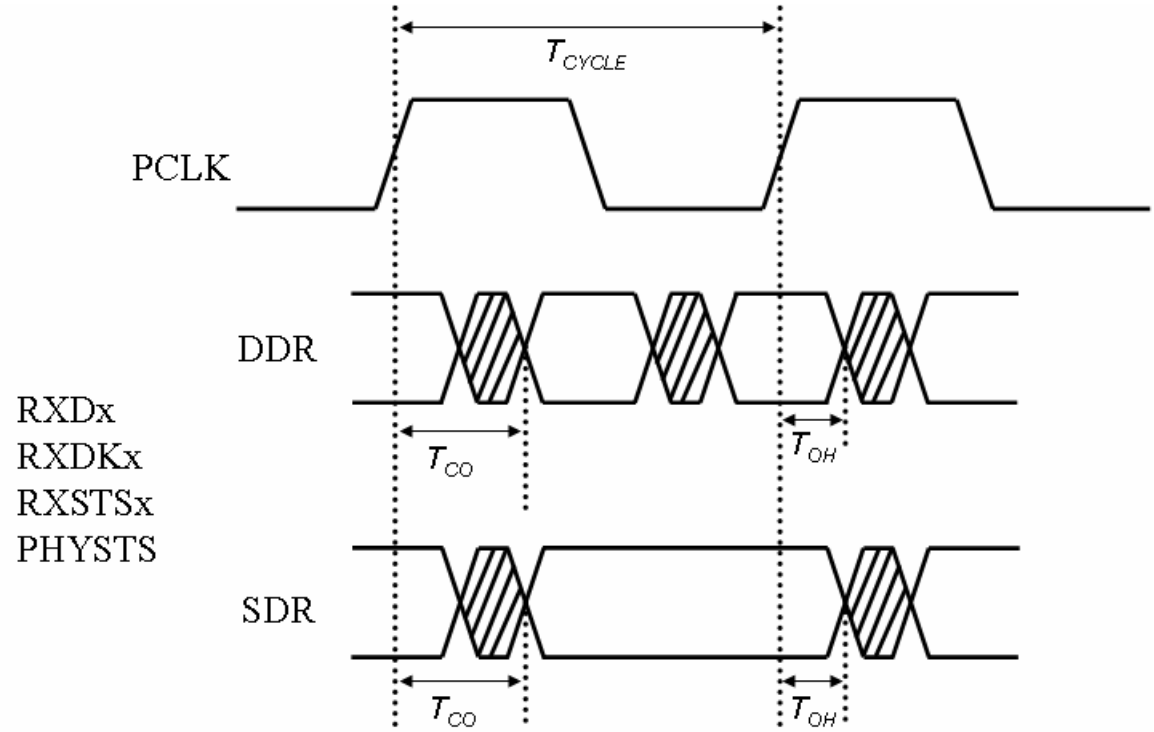

Figure 8.2 – Definition of Output Timing

Table 8.1 – Input Setup, Hold Time and Output Timing for 8-bit SDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{CYCLE}	PCLK cycle time	3.99	4	4.01	ns
Duty-$_H$	Duty cycle for PCLK high	35	-	50	%
T_{IS}	Input setup time requirement [1]	0.8	-	-	ns
T_{IH}	Input hold time requirement [1]	1	-	-	ns
T_{CO}	Clock to output delay [2]	-	-	3.2	ns
T_{OH}	Output hold time [2]	1	-	-	ns

Note:

1. Based on data rise time=1.9ns, fall time=1.3ns, and the slew rate is based on 20%~80% measuring.
2. The test load is 10 pf.
3. All setup, hold and Tco numbers include PCLK jitter and SSO, which is about +/- 250ps.

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Table 8.2 – Input Setup, Hold Time and Output Timing for 8-bit DDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{CYCLE}	PCLK cycle time	7.98	8	8.02	ns
Duty-$_H$	Duty cycle for PCLK high	48	-	50	%
T_{IS}	Input setup time	-	-	1.4	ns
T_{IH}	Input hold time	0.5	-	-	ns
T_{CO}	Clock to output delay	-	1.5	1.6	ns
T_{OH}	Output hold time	0.8	1	-	ns

Note:

This table is based on design target, correlation data will be posted later.

Table 8.3 – Input Setup, Hold Time and Output Timing for 16-bit Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{CYCLE}	PCLK cycle time	7.98	8	8.02	ns
Duty-$_H$	Duty cycle for PCLK high	48	-	50	%
T_{IS}	Input setup time	-	-	1.4	ns
T_{IH}	Input hold time	0.5	-	-	ns
T_{CO}	Clock to output delay	-	5.3	5.6	ns
T_{OH}	Output hold time	4.3	4.7	-	ns

Note:

This table is based on design target, correlation data will be posted later.

Table 8.4 – Input Setup, Hold Time and Output Timing for 10-bit SDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{CYCLE}	PCLK cycle time	3.99	4	4.01	ns
Duty-$_H$	Duty cycle for PCLK high	35	-	50	%
T_{IS}	Input setup time	-	-	1	ns
T_{IH}	Input hold time	1	-	-	ns
T_{CO}	Clock to output delay	-	4	4.2	ns
T_{OH}	Output hold time	3.4	3.7	-	ns

Note:

This table is based on design target, correlation data will be posted later.

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Table 8.5 – Input Setup, Hold Time and Output Timing for 10-bit DDR Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{CYCLE}	PCLK cycle time	7.98	8	8.02	ns
Duty-$_H$	Duty cycle for PCLK high	48	-	50	%
T_{IS}	Input setup time	-	-	1.4	ns
T_{IH}	Input hold time	0.5	-	-	ns
T_{CO}	Clock to output delay	-	4.1	4.3	ns
T_{OH}	Output hold time	3.5	3.7	-	ns

Note:

This table is based on design target, correlation data will be posted later.

8.2 Reference Timing Information

Table 8.6 – Reference Timing Information

Symbol	Parameter	Min	Typ	Max	Unit
T_{RECDET}	Time for receiver detection	-	10	-	us
$T_{PHYSTS-RESET}$	Timing from de-asserting RST_N to the falling edge of PHYSTS	-	16.7	-	us
T_{RESET}	Reset Assertion Time to GL9714	10	-	-	us

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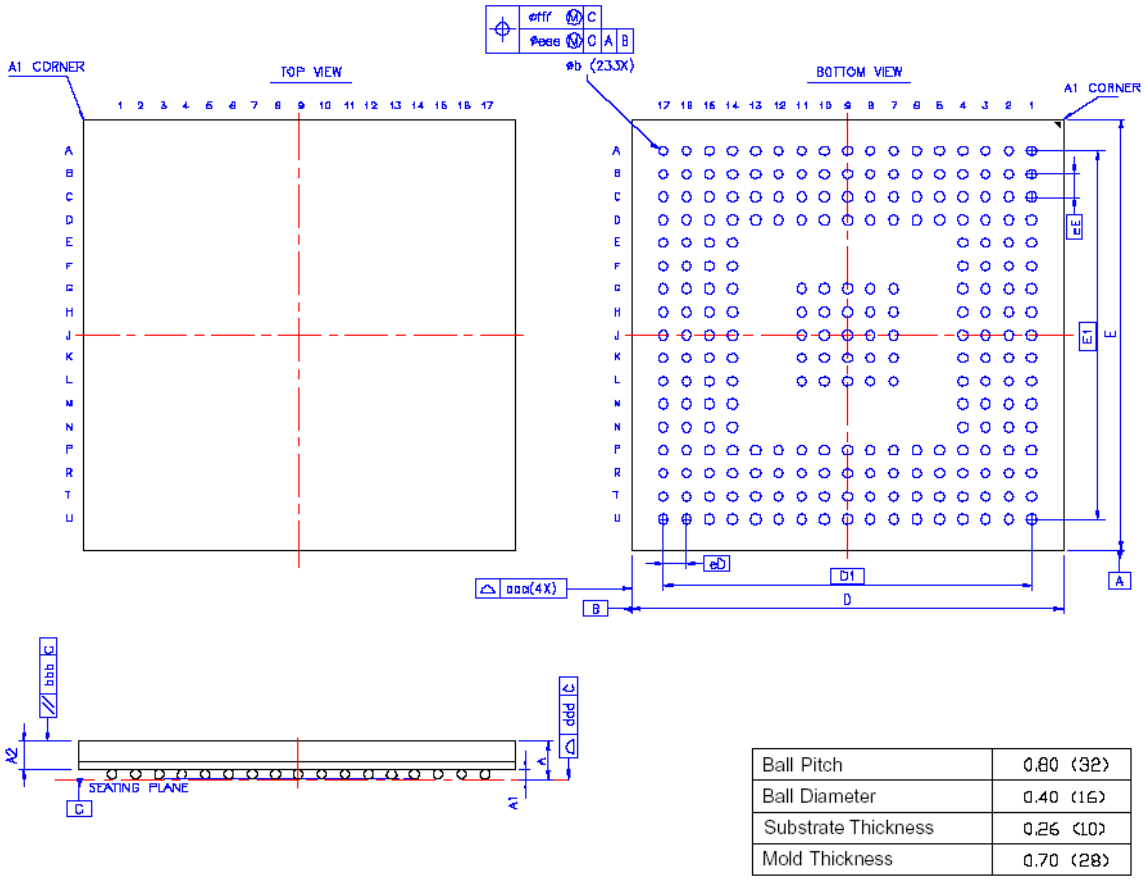
CHAPTER 9 PACKAGE DIMENSION

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.40 (55)
A1	0.27 (11)		0.37 (15)
A2	0.96 (38) REF		
b	0.37 (15)		0.47 (19)
D	14.95 (589)	15.00 (591)	15.05 (593)
E	14.95 (589)	15.00 (591)	15.05 (593)
eD	0.80 (32) BSC		
D1	12.80 (504) BSC		
eE	0.80 (32) BSC		
E1	12.80 (504) BSC		
aaa	0.15 (6)		
bbb	0.20 (8)		
ddd	0.12 (5)		
eee	0.15 (6)		
fff	0.08 (3)		

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.



Ball Pitch	0.80 (32)
Ball Diameter	0.40 (16)
Substrate Thickness	0.26 (10)
Mold Thickness	0.70 (28)

Figure 9.1 - GL9714 233 Pin LFBGA Package

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CHAPTER 10 ORDERING INFORMATION

Table 10.1 - Ordering Information

Part Number	Package	Green	Version	Status
GL9714-TgGxx	233-pin LFBGA	Green Package	xx	Engineering Sample

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