MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX629

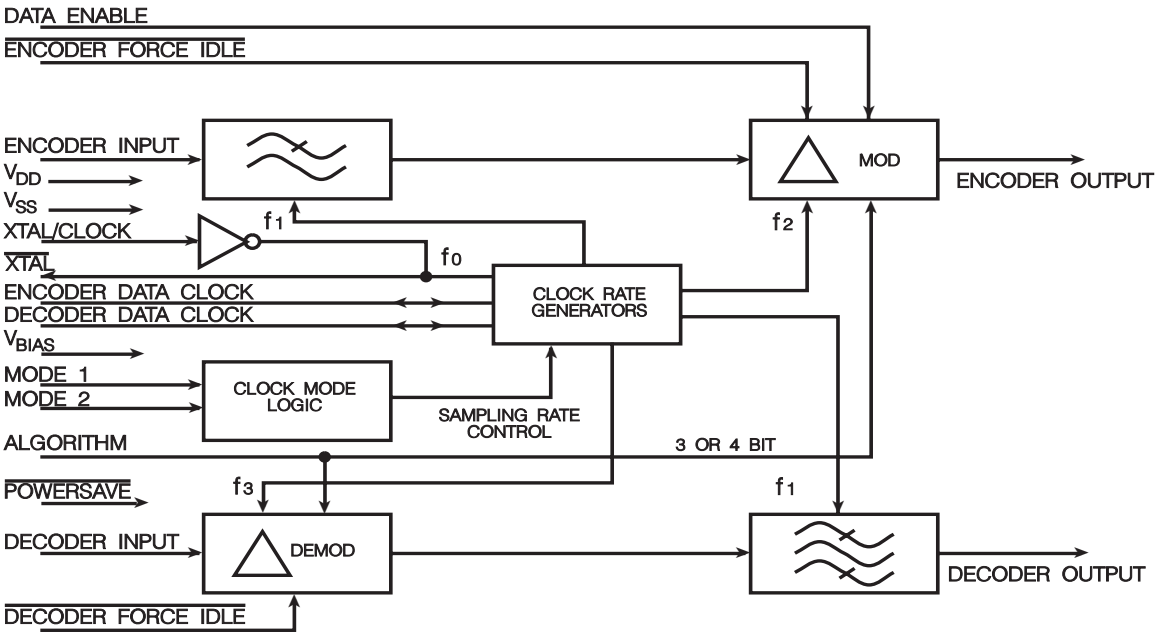
DELTA MODULATION CODEC meets Mil-Std-188-113

Features

- **Meets Mil-Std-188-113**
- **Single Chip Full Duplex CVSD CODEC**
- **On-chip Input and Output Filters**
- **Programmable Sampling Clocks**
- **3- or 4-bit Companding Algorithm**
- **Powersave Capabilities**
- **Low Power, 5.0V Operation**

Applications

- **Military Communications**
- **Multiplexers, Switches, & Phones**



The MX629 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in military communications systems. This device is suitable for applications in military delta multiplexers, switches, and phones. The MX629 is designed to meet Mil-Std-188-113 specifications.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32, or 64kbps from an internal clock generator or externally injected in the 8 to 64kbps range. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle capabilities are provided forcing 10101010…pattern in encode and a $V_{DD}/2$ bias in decode. The companding circuit may be operated with an externally selectable 3- or 4-bit algorithm. The device may be placed in standby mode by selecting Powersave. A reference 1.024MHz oscillator uses an external clock or crystal.

The MX629 operates with a supply voltage of 5.0V and is available in the following packages: 24-pin PLCC (MX629LH), 22-pin CERDIP (MX629J), and 22-pin PDIP (MX629P).

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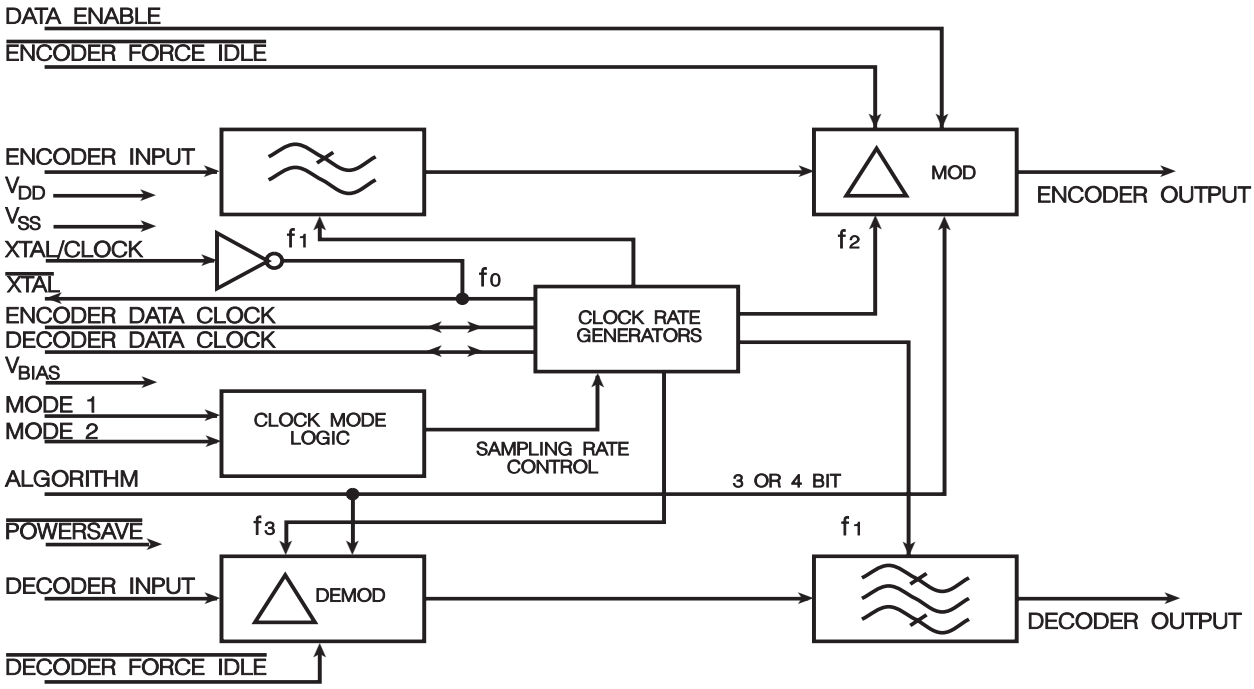

Figure 1: Block Diagram

2 Signal List

J/P	LH	Name	Signal	Description
1	1	Xtal/Clock	input	Input to the clock oscillator inverter. A 1.024MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 2.
	2	N/C		No Connection
2	3	$\overline{\text{Xtal}}$	output	The 1.024 MHz output of the clock oscillator inverter.
3	4	N/C		No Connection
4	5	Encoder Data Clock	input/ output	A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon Clock Mode 1, 2 inputs and Xtal frequency (see Clock Mode pins).
5	6	Encoder Output	output	The encoder digital output. This is a three-state output whose condition is set by the Data Enable and $\overline{\text{Powersave}}$ inputs. See Table 2.
6	7	$\overline{\text{Encoder Force Idle}}$		When this pin is at a logical “0” the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical “1” the encoder encodes as normal. Internal 1MΩ pullup.
7	8	Data Enable	input	Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1 MΩ pullup.
8	9	N/C		No Connection
9	10	V_{BIAS}		Normally at $V_{DD}/2$ bias, this pin should be externally decoupled by capacitor C4. Internally pulled to V_{SS} when “$\overline{\text{Powersave}}$” is a logical “0”.
10	11	Encoder Input	input	The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 2.
11	12	V_{SS}	power	Negative Supply
12	13	N/C		No Connection
13	14	Decoder Output	output	The recovered analog signal is output at this pin. It is the buffered output of a lowpass filter and requires external components. During “Powersave” this output is open circuit.
14	15	N/C		No Connection
15	16	$\overline{\text{Powersave}}$		A logic “0” at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical “1”, the codec operates normally. Internal 1 MΩ pullup.
	17	N/C		No Connection
16	18	$\overline{\text{Decoder Force Idle}}$		A logic “0” at this pin gates a 0101... pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is a logical “1” the decoder operates as normal. Internal 1MΩ pullup.
17	19	Decoder Input		The received digital signal input. Internal 1 MΩ pullup.
18	20	Decoder Data Clock	input/ output	A logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1,2 inputs. See Clock Mode pins.
19	21	Algorithm		A logic “1” at this pin sets this device for a 3-bit companding algorithm. A logical “0” sets a 4-bit companding algorithm. Internal 1 MΩ pullup.

J/P	LH	Name	Signal	Description
20	22	Clock Mode 2		Clock rates refer to f = 1024MHz Xtal/Clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Internal 1MΩ pullups. See Table 3.
21	23	Clock Mode 1		
22	24	V_{DD}	power	Positive Supply. A single 5.0V supply is required.

Table 1: Signal List

Data Enable	Powersave	Encoder Output
1	1	Enable
0	1	High Z (open circuit)
1	0	V_{SS}

Table 2: Encoder Output

Clock Mode 1	Clock Mode 2	Facility
0	0	External Clocks
0	1	Internal, 64kbps = f/16
1	0	Internal, 32kbps = f/32
1	1	Internal, 16kbps = f/64

Table 3: Clock Mode

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3 External Components

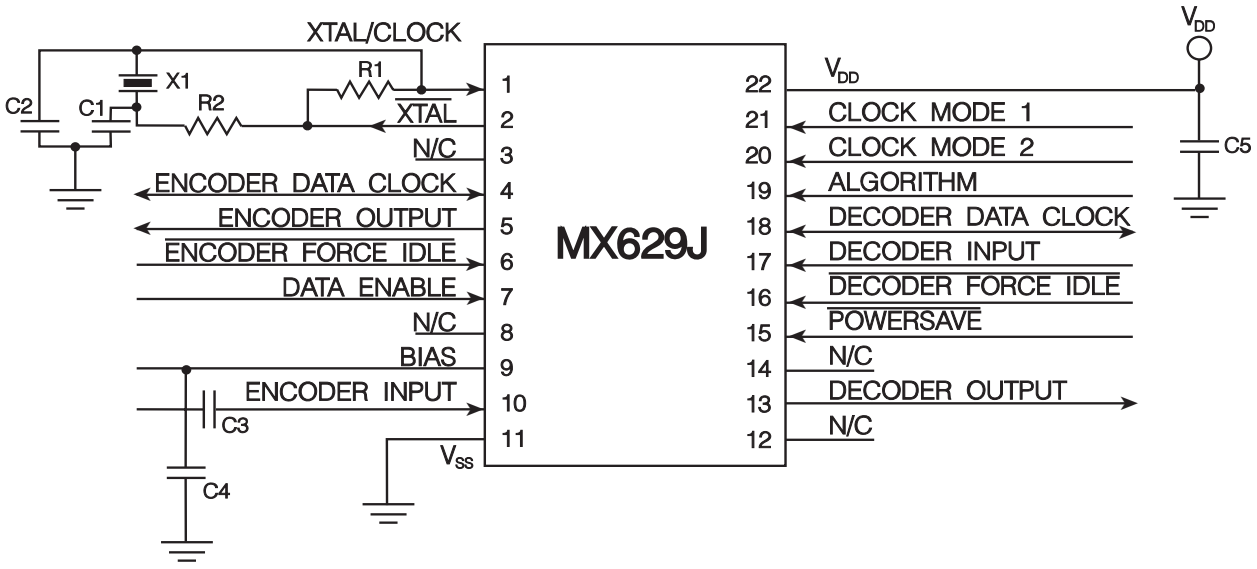

Figure 2: Recommended External Components for Typical Application

R1	Note 1	1MΩ	±10%
R2	Note 2	Selectable	
C1	Note 3	33pF	±20%
C2	Note 3	68pF	±20%

C3	Note 4	1.0µF	±20%
C4	Note 5	1.0µF	±20%
C5	Note 6	1.0µF	±20%
X1	Note 7, 8	1.024MHz	

Table 4: Recommended External Components for Typical Application

Notes:

1. Oscillator inverter bias resister.
2. Xtal Drive limiting resistor.
3. Xtal circuit load capacitor.
4. Encoder input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output idle channel noise levels will improve with even lower source impedance.
5. Bias decoupling capacitor
6. V_{DD} decoupling capacitor
7. A 1.024MHz Xtal/Clock input will yield exactly 16/32/64kbps data clock rates. Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note.
8. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, please consult you crystal manufacturer.

4 General Description

The MX629 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in military communications systems. This device is suitable for applications in military delta multiplexers, switches and phones. The MX629 is designed to meet Mil-Std-188-113 specifications.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32, or 64kbps from an internal clock generator or externally injected in the 8 to 64kbps range. The sampling clock frequency is output for the synchronization of external circuits.

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5 Application

Due to the very low levels of a signal idle channel noise specified for military applications, a noisy or badly regulated power supply could cause instability, putting the overall system performance out of specification. Adherence to the points listed below will assist in minimizing this problem.

1. Care should be taken in the design and layout of the printed circuit board.
2. All external components (as recommended in Figure 2) should be kept close to the package.
3. Tracks should be kept short, particularly the Encoder Input capacitor and the V_{BIAS} capacitor.
4. Xtal/Clock tracks should be kept well away from analog inputs and outputs.
5. Inputs and outputs should be screened whenever possible.
6. A 'ground plane' connected to V_{SS} will assist in eliminating external pick-up on the input and output pins.
7. It is recommended that the power supply rails have less that $1mV_{RMS}$ of noise allowed.
8. The source impedance to the Encoder Input pin must be less that 100W; output idle channel, noise levels will improve with even power source impedances.

5.1 CODEC Integration

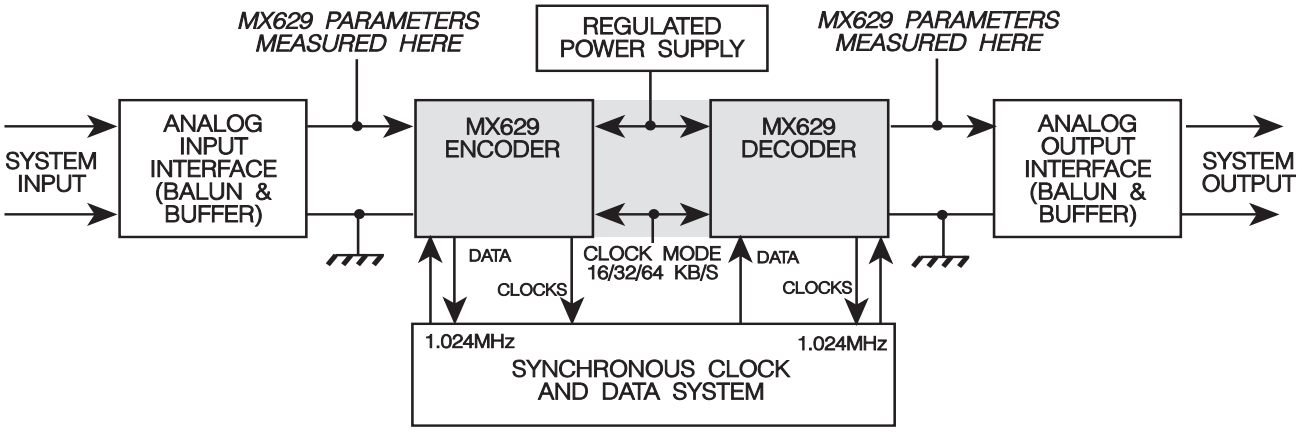


Figure 3: System Configuration using the MX629

5.2 Digital to Analog Performance

Sample Rate	Bit Sequence at Decoder Input	'Run of Threes' (%)	Output level (dBm0)
16kbps	11011011010010010010	0	-29.2±2
32kbps	11011011010101001001001001001010101011011O	0	-30.0±2
16kbps	1111101101000010010	30	0±1
32kbps	11111101101010100001000000100101010111O	30	0±1

Table 5: Bit Sequence Test and Results

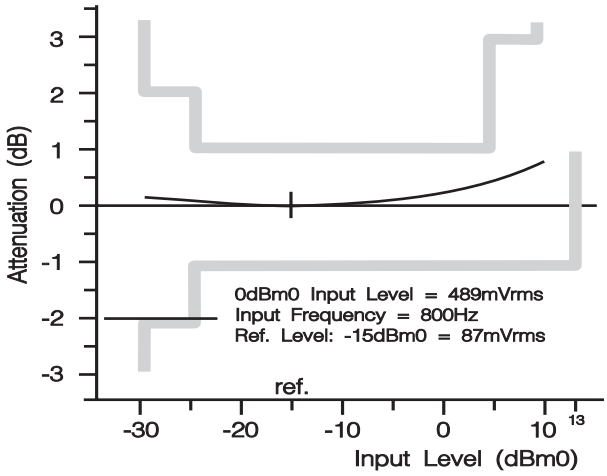


Figure 4: Gain vs. Input Level (16kbps)

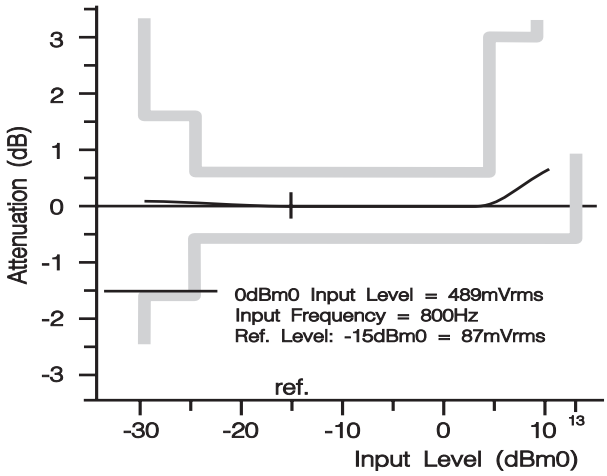


Figure 5: Gain vs. Input Level (32kbps)

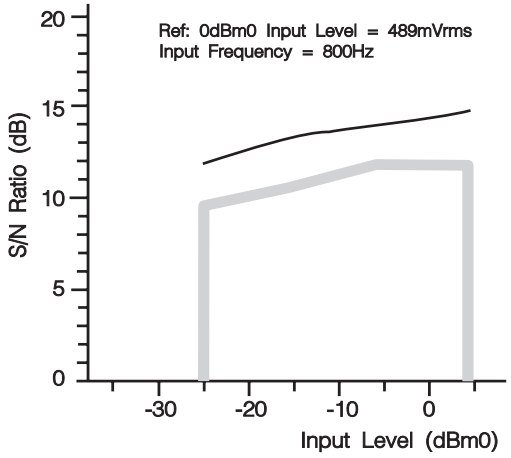


Figure 6: S/N vs. Input Level (16kbps)

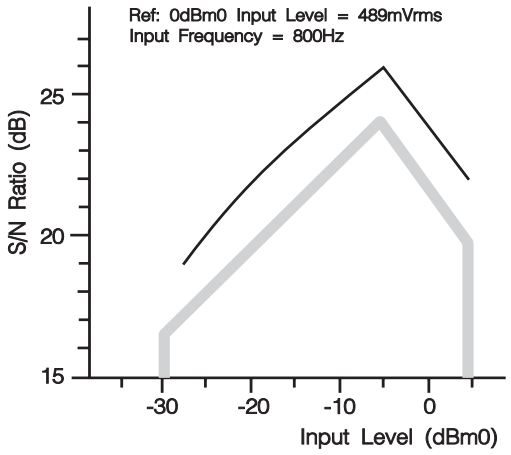


Figure 7: S/N vs. Input Level (32kbps)

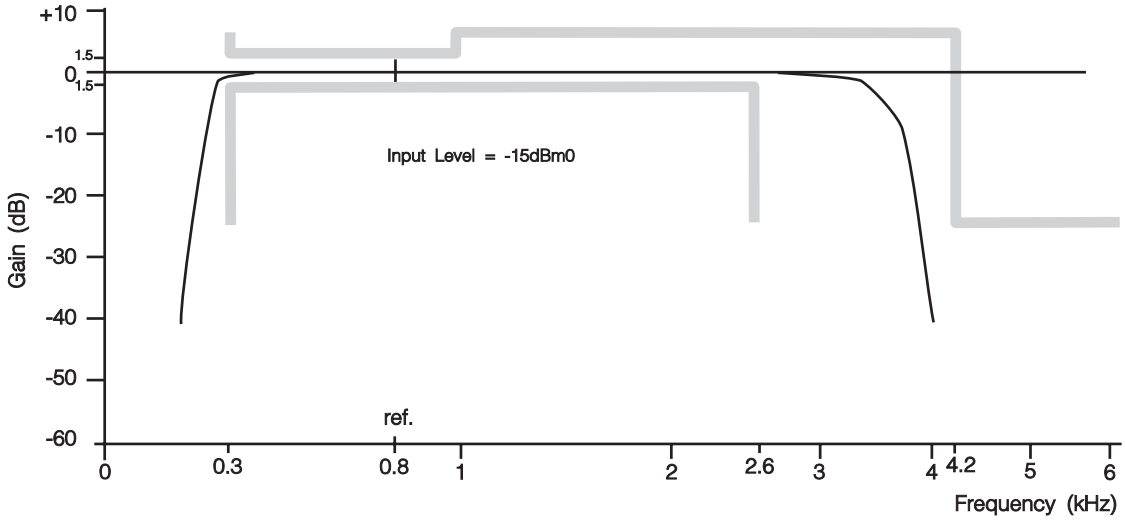


Figure 8: Attenuation distrotion vs. Frequency (16kbps)

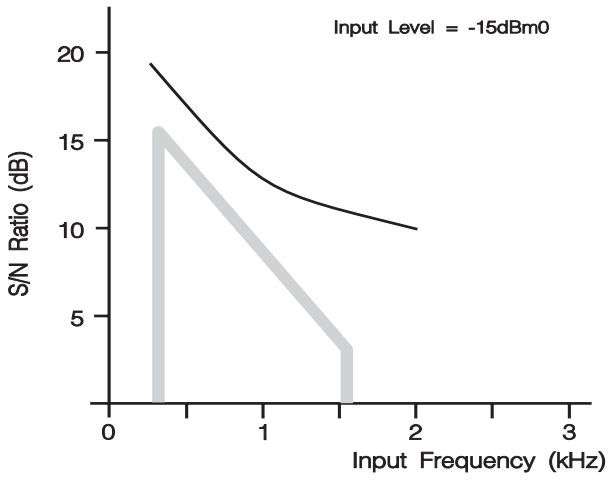


Figure 9: S/N vs. Input Frequency (16kbps)

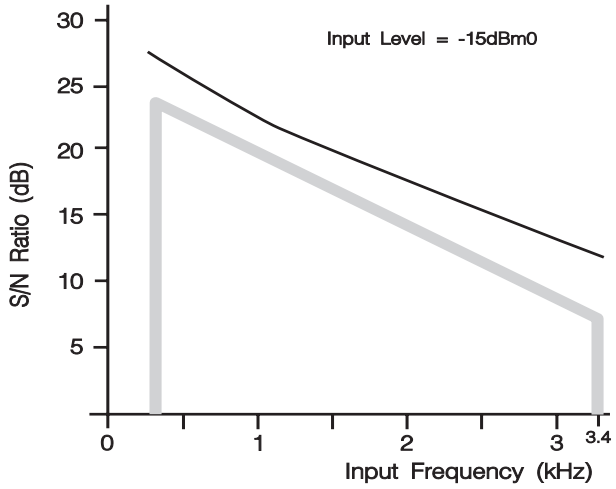


Figure 10: S/N vs. Input Frequency (32kbps)

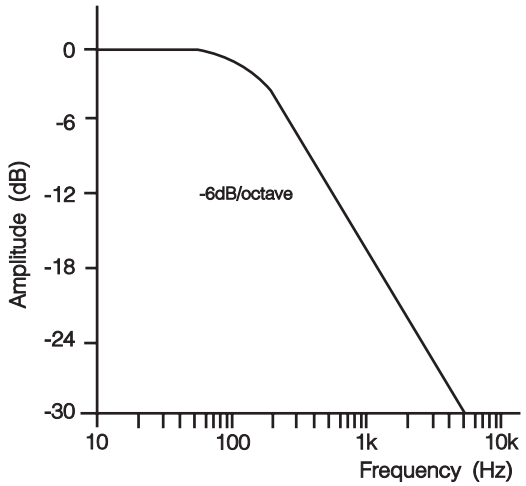


Figure 11: Principal Integrator Response

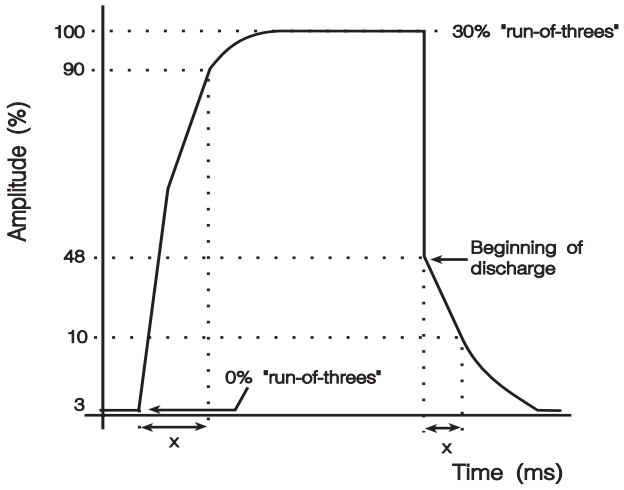


Figure 12: Compand Envelope

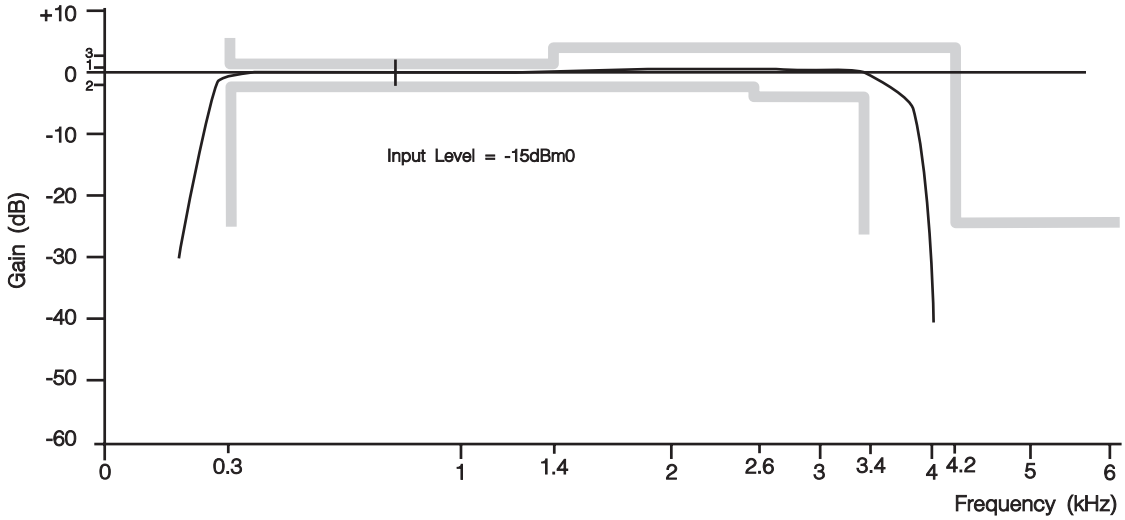


Figure 13: Attenuation Distortion vs. Frequency (32kbps)

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
any other pin	-20	20	mA
J / P / LH Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C	-	800	mW
Derating above 25°C	-	10	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ.	Max.	Units
Supply (V_{DD} - V_{SS})	4.5	5.0	5.5	V
Operating Temperature	-40		85	°C
Xtal Frequency	500	1.024	1500	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 5.0V at T_{AMB} = 25°C, Audio Test Frequency = 820Hz Xtal/Clock f_0 = 1.024MHz
3-bit Compand Algorithm, Sample Clock Rate = 32kbps, Audio level 0dB ref (0 dBm0) = 489mV_{RMS}.

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)			5.5		mA
Supply Current (Powersave)			400		μA
Input logic '1'	8	3.5			V
Input Logic '0'	8			1.5	V
Output Logic '1'		4.0			V
Output Logic '0'				1.0	V
Digital input Impedance					
Logic I/O pins		1.0	10		MΩ
Logic Input pins, Pullup Resistor	2	300			kΩ
Digital output impedance				4	kΩ
Analog Input Impedance	4		1		kΩ
Analog Output Impedance	7			800	Ω
Three State Output Leakage		-4		4	μA
Insertion Loss	3	-2		2	dB
Dynamic Values	1,9				
Encoder					
Analog signal Input levels	5, 9	-35		12	dBmO
Principal Integrator Frequency		127	159	212	Hz
Encoder Passband			3400		Hz
Compand Time Constant		4.0	5.0	6.0	ms
Decoder					
Analog Signal Output Levels	5, 9	-35		12	dBmO
Decoder Passband		300		3400	Hz
Encoder Decoder (Full Codec)					
Compression Ration (Cd = 0.3 to Cd = 0.0)			16:1		
Passband		300		3400	Hz
Stopband		4.2			KHz
Stopband Attenuation					
4200Hz to 6000Hz		25			dB
>6000Hz			60		dB
Passband Gain			0		dB
Passband Ripple		-3		3	dB
300Hz – 1400Hz		-1		1	dB
1400Hz – 2600Hz		-1		1	dB
2600Hz –3400Hz		-2		3	dB
Output Noise (Input Short Circuit)	9		-55		dBmO
Perfect Idle Channel Noise					
(Encode Forced)	9		-57		dBmO

	Notes	Min.	Typ.	Max.	Units
Group Delay Distrotion	4				
(1000Hz-2600Hz)	6			450	μs
(600Hz-2800Hz)	6			750	μs
(500Hz-3000Hz)	6			1.5	ms
Xtal/clock Frequency			1024		kHz

Notes:

1. Dynamic characteristics are specified at 5.0V unless otherwise specified.
2. All logic inputs except Encoder and Decoder Data clocks
3. For and encoder/Decoder combination, Insertion loss contributed by a single component is half this figure.
4. Driven with a source impedance of <100Ω.
5. Recommended values – See Figures 4, 5, 6, and 7.
6. Group Delay Distortion for the full codec is relative to the delay with and 820Hz, -20dB signal at the encoder input
7. An Emitter Follower output stage.
8. 4V = 80%V_{DD}, 3.5V = 70%V_{DD}, 1.5V = 30%V_{DD}, 1V = 20%V_{DD}
9. Analog Voltage Levels used: 0dBmO = 489mV_{RMS} = -4dBm = 0dB. –15dBmO = 87mV_{RMS}. –20dBmO = 49mV_{RMS} = -24dBm.

6.1.4 TIMING

Serial Bus Timings (See Figure 14)		Min.	Typ.	Max.	Units
t_{CH}	Clock 1 pulse width	1.0			μs
t_{CL}	Clock 0 pulse width	1.0			μs
t_{IR}	Clock rise time	0	100		ns
t_{IF}	Clock fall time		100		ns
t_{SU}	Data set-up time			450	ns
t_H	Data hold time	600			ns
t_{SU} +t_H	Data true time		1.5		μs
t_{PCO}	Clock to output delay time		750		ns
t_{DR}	Data rise time		100		ns
t_{DF}	Data fall time		100		ns
Xtal input frequency = 1.024MHz					

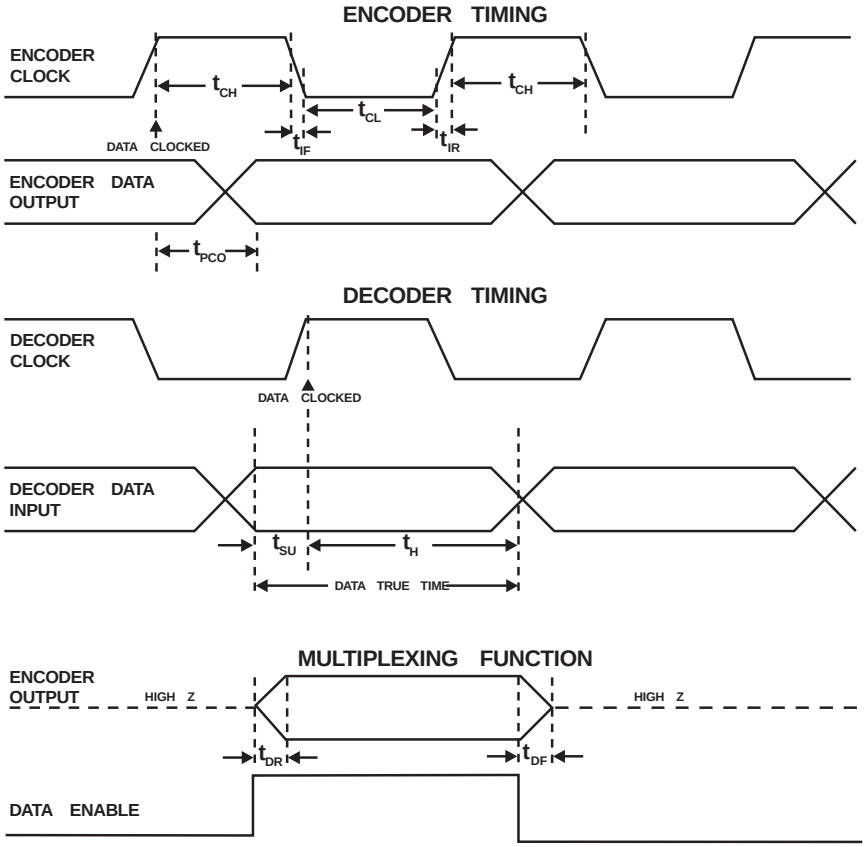
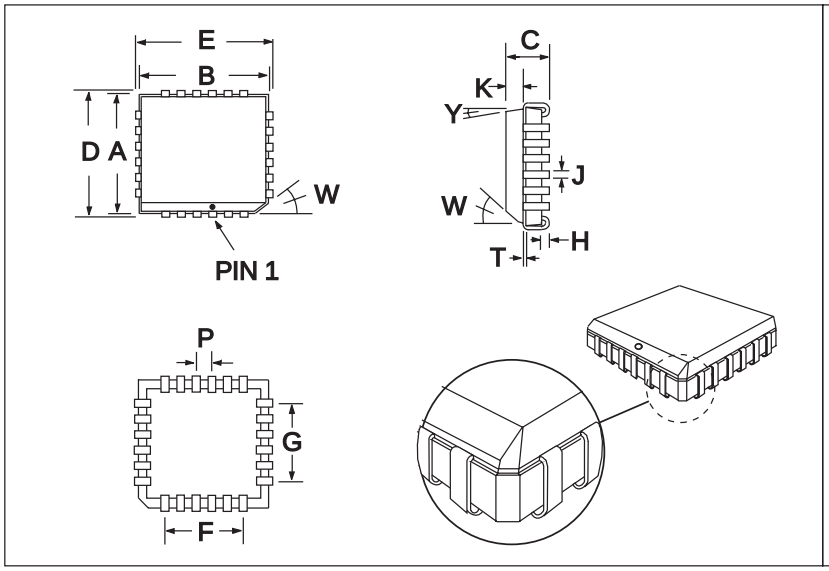


Figure 14: CODEC Timing

6.2 Packaging

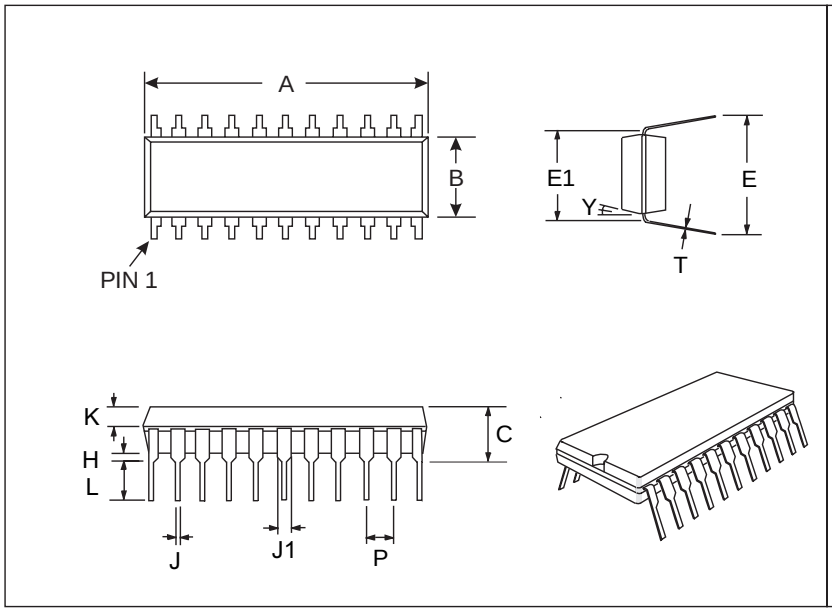


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 24-pin PLCC (LH) Mechanical Outline: *Order as part no. MX629LH*

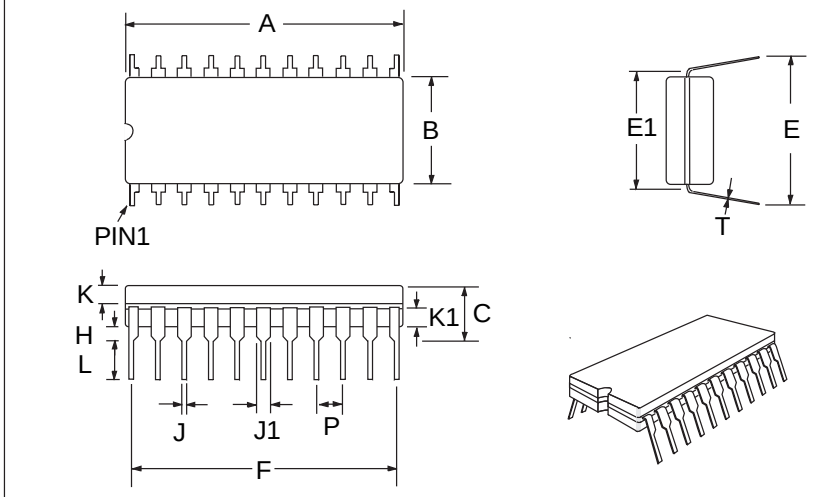


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.080 (27.43)		1.100 (27.94)
B	0.330 (8.38)		0.360 (9.14)
C		0.185 (4.70)	
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.91)		0.420 (10.67)
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K		0.066 (1.68)	
L		0.128 (3.25)	
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 22-pin PDIP (P) Mechanical Outline: *Order as part no. MX629P*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.060 (26.92)		1.080 (27.43)
B	0.376 (9.55)		0.384 (9.75)
C	0.165 (4.19)		0.230 (5.84)
E	0.466 (11.84)		0.515 (13.08)
E1	0.408 (10.36)		0.418 (10.62)
F		1.000 (25.40)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.40)	
K	0.058 (1.47)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 17: 22-pin CERDIP (J) Mechanical Outline: *Order as part no. MX629J*