ANALOG DEVICES

Dual Precision JFET High Speed Operational Amplifier

ANALOG DEVICES INC

OP-249

1.1 Scope.

This specification covers the detail requirement for a dual precision JFET input operational amplifier. It is highly recommended that this data sheet be used as a baseline for new military or aerospace specification control drawings.

1.2 Part Number.

The complete part numbers per Table 1 of this specification is as follows:

Device	Part Number	Package
−1	OP-249AJ/883	J
−1	OP-249AZ/883	Z
−1	OP-249ARC/883	RC

1.2.3 Case Outline.

Letter	Case Outline (Lead Finish Per MIL-M-38510)
J	8-Lead Metal Can (TO-99)
Z	8-Lead Ceramic Dual-in-Line Package (Cerdip)
RC	20-Contact Hermetic Leadless Chip Carrier (LCC)

1.3 Absolute Maximum Ratings.* (T_A = +25°C unless otherwise noted)

Supply Voltage ..... ±18 V
Differential Input Voltage ..... Supply Voltage
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering 60 sec) ..... +300°C
Maximum Junction Temperature (T_J) ..... +175°C

NOTE
*CAUTION: a. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability. b. Remove power before inserting or removing units from their sockets.

1.5 Thermal Characteristics.[1]

Thermal Resistance θ_{JC} = 16°C/W max for J Package
θ_{JA} = 145°C/W max for J Package
θ_{JC} = 12°C/W max for Z Package
θ_{JA} = 134°C/W max for Z Package
θ_{JC} = 32°C/W max for RC Package
θ_{JA} = 88°C/W max for RC Package

NOTE
[1]θ_{JA} is specified for device in socket for cerdip and mounted to PC board for LCC.

OP-249—SPECIFICATIONS

Table 1.

Test	Symbol	Device Types	Limits Min	Limits Max	Group A Subgroups	Test Condition[1]	Units
Input Offset Voltage	V_{OS}	−1		0.5	1	T_A = +25°C	mV
				1.0	2, 3	T_A = −55°C, +125°C	
Average Input Offset Drift	TCV_{OS}	−1		5	8	T_A = −55°C, +125°C	µV/°C
Input Offset Current	I_{OS}	−1		25	1	T_A = +25°C	pA
				4	3	T_A = +125°C	nA
Input Bias Current	I_B	−1		75	1	T_A = +25°C	pA
				20	3	T_A = +125°C	nA
Large Signal Voltage Gain	A_{VO}	−1	1000		4	V_O = ±10 V, $R_L \geq 2$ kΩ T_A = +25°C	V/mV
			500		5, 6	V_O = ±10 V, $R_L \geq 2$ kΩ T_A = −25°C, +125°C	
Output Voltage Swing	V_O	−1	±12		4	$R_L \geq 2$ kΩ, T_A = +25°C	V
			±12		5, 6	$R_L \geq 2$ kΩ; T_A = −55°C, +125°C	
Output Short Circuit Limit	I_{SC}	−1	±20	±50	1	V_O = GND, T_A = +25°C	mA
			±10	±60	2, 3	V_O = GND; T_A = −55°C, +125°C	
Supply Current	I_{SY}	−1		7	1	V_O = 0 V, No Load, T_A = +25°C	mA
				7	2, 3	V_O = 0 V, No Load; T_A = −55°C, +125°C	
Slew Rate	SR	−1	18		7	A_{VCL} = +1, R_L = 2 kΩ C_L = 50 pF, T_A = +25°C	V/µs
Common-Mode Rejection Ratio	CMRR	−1	80		1	V_{CM} = IVR = ±11 V, T_A = +25°C	dB
			76		2, 3	V_{CM} = IVR = ±11 V; T_A = −55°C, +125°C	
Power Supply Rejection	PSR	−1		31.6	1	V_S = ±4.5 V to ±18 V, T_A = +25°C	µV/V
				50.0	2, 3	V_S = ±4.5 V to ±18 V; T_A = −55°C, +125°C	
Input Voltage Range[2]	IVR	−1	±11		1	T_A = +25°C	V
			±11		2, 3	T_A = −55°C, +125°C	
Settling Time	t_S	−1		1.2	9	10 V Step, 0.01%, T_A = +25°C	µs

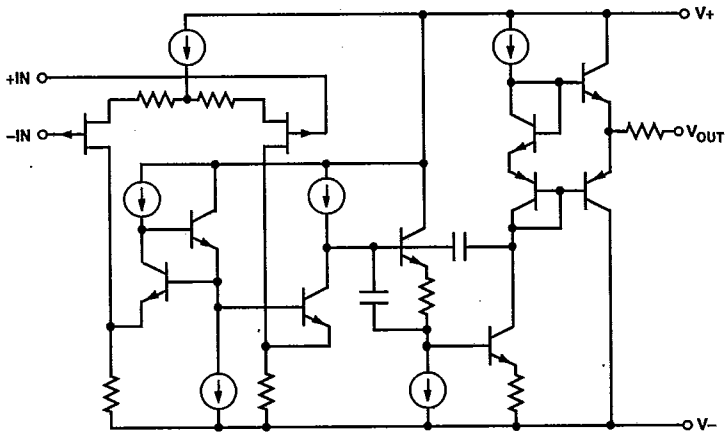
NOTES
[1]V_S = ±15 V, V_{CM} = 0 V, unless otherwise specified.
[2]Input voltage range (IVR) is guaranteed by common-mode rejection ratio (CMRR) test.

Table 2. Electrical Test Requirements

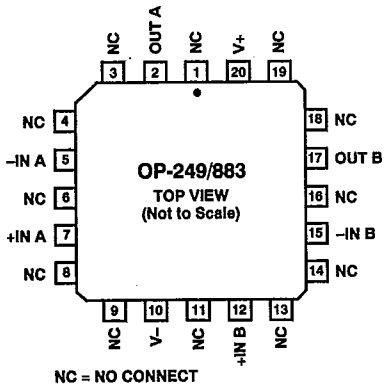
MIL-STD-883 Test Requirements	Group A Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1,* 2, 3, 4, 5, 6
Group A Test	1, 2, 3, 4, 5, 6, 7, 8, 9

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA. V_{OS} is excluded from PDA.

3.2.1. Functional Block Diagram and Terminal Assignments.

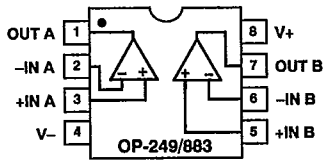


20-Position LCC
(RC Suffix)

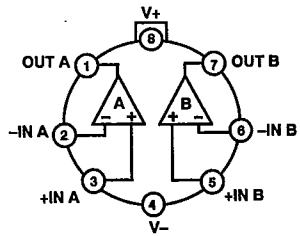


NC = NO CONNECT

8-Pin Ceramic DIP
(Z Suffix)



TO-99
(J Suffix)



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (C).