# PDSP16340

## POLAR TO CARTESIAN CONVERTER

*(Supersedes version in December 1993 Digital Video & Digital Signal Processing IC Handbook, HB3923-1)*

The PDSP16340 can be configured to perform either a coordinate conversion function, or simply to provide a sine / cosine look-up table. When employed as a coordinate conversion processor, the device converts data from 16 bit polar coordinates (R,Ø) into 16 bit cartesian coordinates (Real, Imaginary). The translation is illustrated in Fig. 1, and uses the formula:-

$Xr = R \cos(Ø)$
$Xi = R \sin(Ø)$

In look-up table mode, the user enters 16 bit phase data, and the chip outputs the corresponding sine and cosine values. A typical application is shown in Fig. 5.

The PDSP16340 is pipelined to process a continuous stream of data at 20 MHz, and outputs a new (16 + 16) bit result every clock cycle. The RANGE control signal allows the user to select the input range most appropriate to the system. Data is produced in Two's Complement Fractional format.

### APPLICATIONS

- Digital Signal Processing
- Radar Systems
- Sonar Systems
- Robotics
- Medical Imaging

### FEATURES

- Provides R cos(Ø) and R sin(Ø) in 16 bit streams using a CORDIC processor
- Look-up table equivalent to 64k by 32 bit ROM
- 20MHz clock rate
- Tri-state outputs and independent data enables
- 84 Pin PGA or 132 pin QFP

### ASSOCIATED PRODUCTS

| | |
|---|---|
| **PDSP16330** | Pythagoras Processor |
| **PDSP16256** | Programmable FIR Filter |
| **PDSP16510** | FFT Processor |
| **PDSP16350** | I/Q Splitter and NCO |
| **PDSP16116** | 16 Bit Complex Multiplier |
| **PDSP16318** | Complex Accumulator |

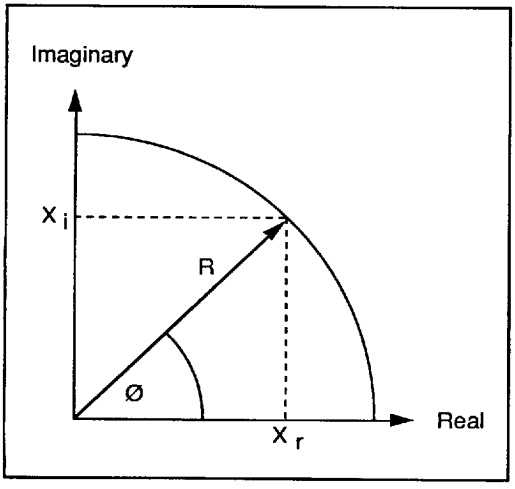



*Fig. 1. Cartesian to Polar Coordinates*

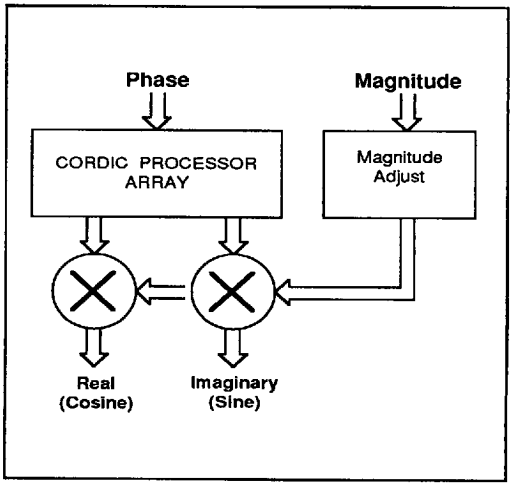



*Fig. 2. Simplified Block Diagram*

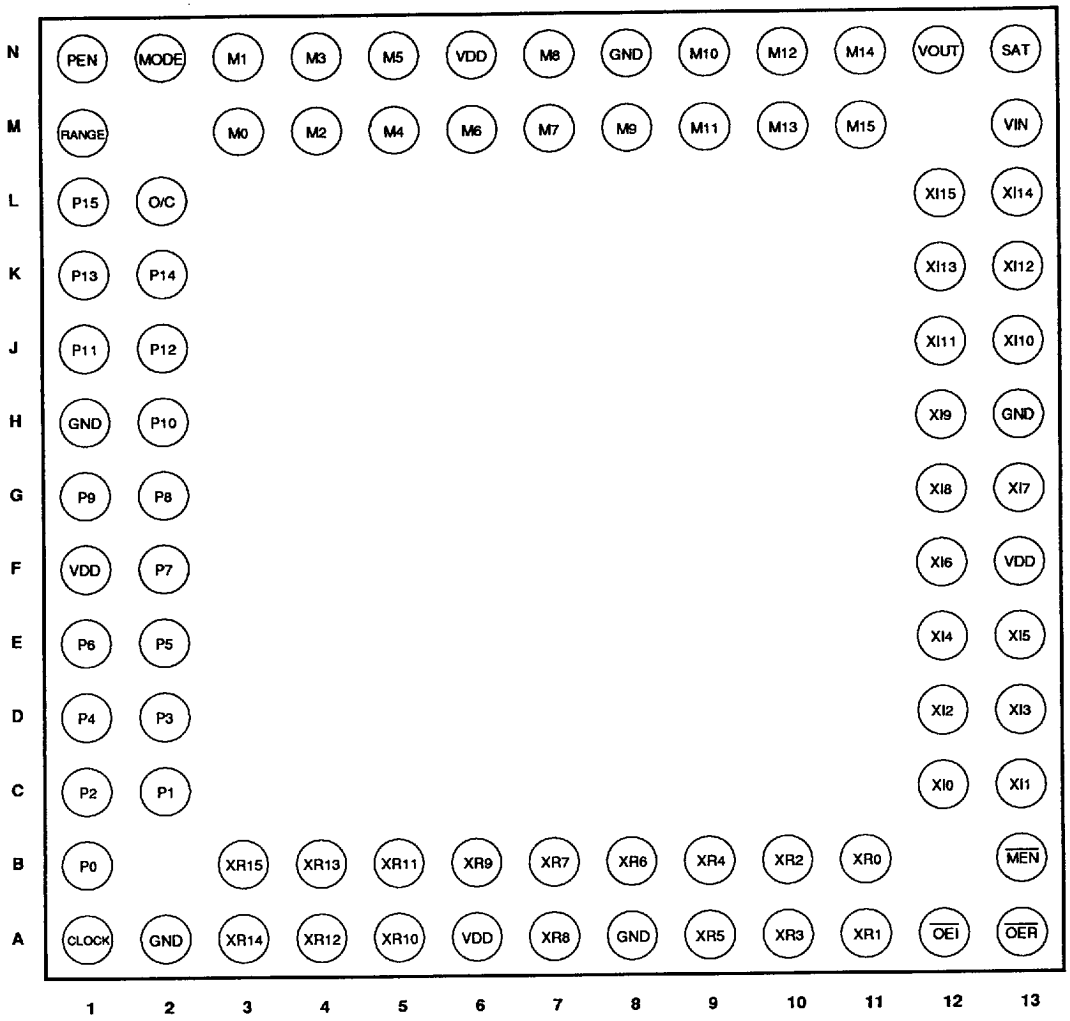



*Fig. 3A Device Pinout - Bottom View (84 pin PGA - AC84)*

| GC | SIG | GC | SIG | GC | SIG | GC | SIG |
|---|---|---|---|---|---|---|---|
| 1 | N/C | 34 | N/C | 67 | GND | 100 | GND |
| 2 | $\overline{MEN}$ | 35 | VOUT | 68 | RANGE | 101 | VDD |
| 3 | N/C | 36 | M15 | 69 | N/C | 102 | GND |
| 4 | XI0 | 37 | GND | 70 | N/C | 103 | N/C |
| 5 | XI1 | 38 | VDD | 71 | P15 | 104 | XR15 |
| 6 | XI2 | 39 | M14 | 72 | GND | 105 | XR14 |
| 7 | GND | 40 | N/C | 73 | VDD | 106 | N/C |
| 8 | VDD | 41 | M13 | 74 | P14 | 107 | XR13 |
| 9 | XI3 | 42 | M12 | 75 | P13 | 108 | XR12 |
| 10 | XI4 | 43 | N/C | 76 | P12 | 109 | N/C |
| 11 | N/C | 44 | M11 | 77 | N/C | 110 | XR11 |
| 12 | XI5 | 45 | M10 | 78 | P11 | 111 | N/C |
| 13 | XI6 | 46 | N/C | 79 | P10 | 112 | XR10 |
| 14 | N/C | 47 | M9 | 80 | N/C | 113 | XR9 |
| 15 | XI7 | 48 | GND | 81 | P9 | 114 | VDD |
| 16 | XI8 | 49 | VDD | 82 | GND | 115 | GND |
| 17 | VDD | 50 | M8 | 83 | VDD | 116 | XR8 |
| 18 | GND | 51 | M7 | 84 | P8 | 117 | XR7 |
| 19 | XI9 | 52 | M6 | 85 | P7 | 118 | N/C |
| 20 | N/C | 53 | M5 | 86 | P6 | 119 | XR6 |
| 21 | XI10 | 54 | VDD | 87 | N/C | 120 | XR5 |
| 22 | XI11 | 55 | M4 | 88 | P5 | 121 | N/C |
| 23 | N/C | 56 | VDD | 89 | N/C | 122 | XR4 |
| 24 | XI12 | 57 | M3 | 90 | P4 | 123 | N/C |
| 25 | XI13 | 58 | GND | 91 | P3 | 124 | XR3 |
| 26 | XI14 | 59 | M2 | 92 | VDD | 125 | XR2 |
| 27 | VDD | 60 | M1 | 93 | GND | 126 | N/C |
| 28 | GND | 61 | GND | 94 | P2 | 127 | XR1 |
| 29 | XI15 | 62 | VDD | 95 | P1 | 128 | VDD |
| 30 | VIN | 63 | M0 | 96 | N/C | 129 | GND |
| 31 | N/C | 64 | MODE | 97 | P0 | 130 | XR0 |
| 32 | N/C | 65 | $\overline{PEN}$ | 98 | N/C | 131 | $\overline{OE1}$ |
| 33 | SAT | 66 | VDD | 99 | CLK | 132 | $\overline{OE2}$ |

*Fig.3B Pin out Table (132 pin ceramic QFP - GC132)*

| SIGNAL | DESCRIPTION |
|---|---|
| M15:0 | 16 bit 2's complement data representing the magnitude of the phase angle. Data is loaded into the input register on the rising edge of CLK. These inputs are not used in look-up table mode, however, they should be tied high or low for electrical, rather than logical, reasons. M15 is the MSB. |
| P15:0 | 16 bit data representing the phase angle. Data is loaded into the input register on the rising edge of CLK. P15 is the MSB. |
| XR15:0 | 16 bit 2's complement real data output, or cosine output in the table look-up mode. Data is passed to the XR outputs on the rising edge of CLK. |
| XI15:0 | 16 bit 2's complement imaginary data output, or sine output in the table look-up mode. Data is passed to the XI outputs on the rising edge of CLK. |
| RANGE | Magnitude range select. When this pin is high, the MSB of the M input bus (also the sign bit) will represent $2^1$. When low, it will represent $2^0$ |
| SAT | Input data saturated flag. This output goes high to indicate that input data of magnitude greater than SQRT(2) has been saturated to SQRT(2). It is internally delayed such that it appears at the output at the same time as the data which resulted from the saturated input value. |
| $\overline{\text{MEN}}$ | Clock enable for the magnitude input port. When low new data may be latched in the input register; when high the register remains in its previous state. |
| $\overline{\text{PEN}}$ | Clock enable for the phase input port. When low new data may be latched in the input register: when high the register remains in its previous state. |
| $\overline{\text{OER}}$ | Output enable for the XR output port. When high the XR output is forced into a high impedance state. |
| $\overline{\text{OEI}}$ | Output enable for the XI output port. When high the XI output is forced into a high impedance state. |
| VIN | Valid data input flag. This input is connected to VOUT via a pipeline delay which matches the data path pipeline delay. Hence, if VIN is set high when valid data is input, then VOUT will go high when valid results are output. It performs no internal control function. |
| VOUT | Valid data output flag which is a delayed version of VIN as explained above. |
| MODE | When high, this input configures the chip into look-up table mode in which the M inputs are redundant and internally replaced by a unity magnitude. When low, the chip is configured in coordinate conversion mode. |
| CLK | Common clock to all internal registers. |
| VDD | Four +5V power pins. All power supply pins must be connected. |
| GND | Four ground pins. All pins must be connected. |

*Table 1. Signal description*

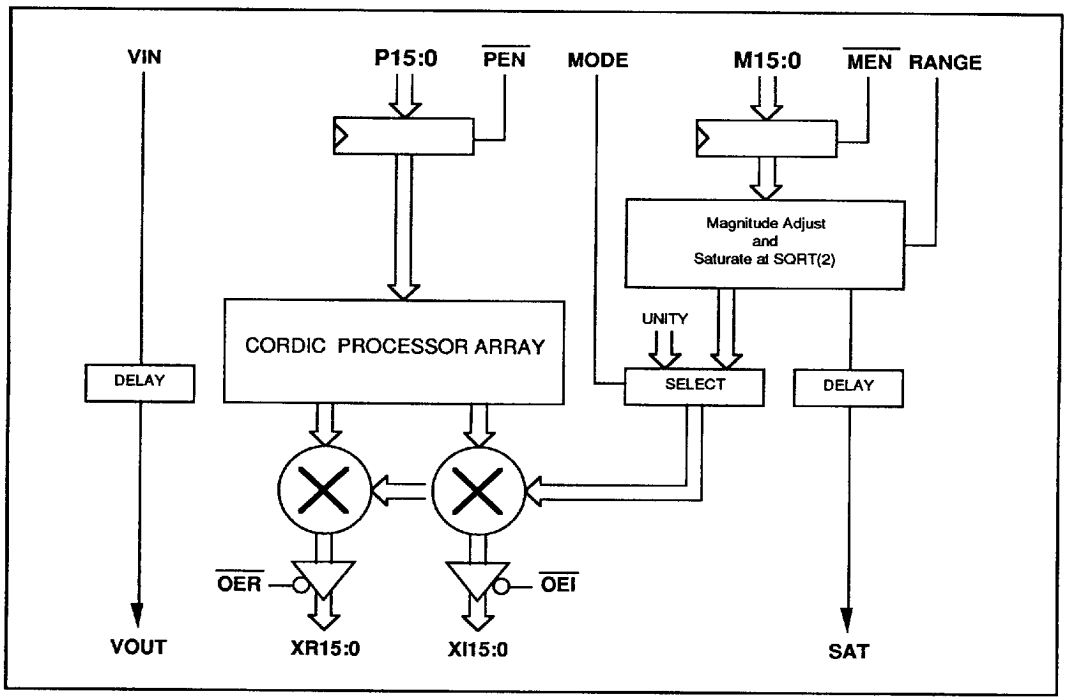



*Fig. 4. Internal Block Diagram*

## OPERATION

The functional blocks used within the device are illustrated by Fig. 4. Both input data and output data are fully registered to allow the device to be easily incorporated into data flow DSP systems. The sine and cosine values are actually calculated in a 26 stage pipelined arithmetic processor, and are accurate to 16 bits. This technique allows high data throughputs, and requires less die area than the equivalent ROM.

The PDSP16340 has two modes of operation, which are selected by the logical state of the MODE input pin. This pin should be tied high or low to suite the particular application.

### Look-up Mode

In the Table Look-up mode the MODE pin is tied high, and the device is used to provide simultaneous sine and cosine values at rates up to the maximum clock frequency. A new phase value is clocked into the Phase Port (P15:0) on each cycle, and the corresponding sine and cosine values appear at the XI and XR ports 29 clock cycles later. In this operating mode the MAGNITUDE inputs, the $\overline{\text{MEN}}$, and the RANGE inputs are logically redundant. They must, however, be tied either high or low for electrical reasons. If the Phase Port is disabled by pulling $\overline{\text{PEN}}$ high, then the look-up table will continue to provide the sine and cosine outputs corresponding to the value of P15:0 present during the active clock edge before the $\overline{\text{PEN}}$ level change.

Fig. 5. illustrates a typical FFT arrangement with the PDSP16340 providing sine and cosine 'twiddle' factors for use by the butterfly processor. Use of the PDSP16520 Quad Port RAM, and the PDSP16116/318 complex arithmetic element, allows butterfly calculations to be performed at rates up to 20 MHz.

### Coordinate Conversion

In the Coordinate Conversion Processor mode the MODE pin is tied low, and the PDSP16340 converts data from polar format into the corresponding real and imaginary Cartesian co-ordinates. The coordinate conversion operation is equivalent to the inverse of the function performed by the PDSP16330 Pythagoras Processor. The device produces simultaneous sine and cosine values from the incoming phase angle, and then multiplies these results with the appropriate magnitude value. The $\overline{\text{MEN}}$ input allows the value in the input latch to be retained in a similar manner to the use of the $\overline{\text{PEN}}$ control.

The RANGE control allows the device to accept magnitude data in the range of, either, -1 to within one LSB of +1, or from -2 to within one LSB of +2. The smaller range option allows maximum accuracy to be preserved, if fractional inputs are expected. The latter option enables the theoretical maximum polar magnitude of SQRT(2) to be accommodated. A negative magnitude introduces a 180° phase shift.

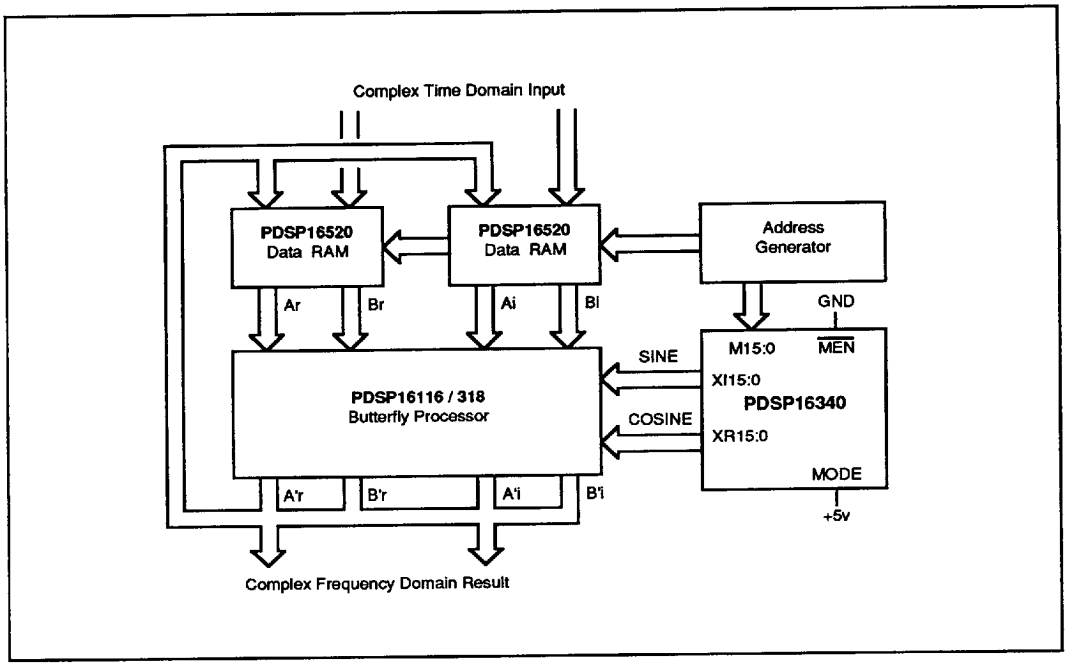



*Fig. 5. Sin / Cos generator for 20 MHz FFT System*

The device will replace all incoming values above the square root of two with the maximum value. The SAT output indicates when this replacement has internally occurred. The flag is delayed such that it is valid at the same time as the output data which was calculated from the saturated input.

## DATA FORMATS

When the device is configured in the co-ordinate conversion mode (MODE pin is low), the magnitude (M) input bus can have one of the following data formats:

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WEIGHTING RANGE = 1 | S | $2^{0}$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ |
| RANGE = 0 | S | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |

The sign bit is provided to maintain compatibility with normal arithmetic procedures, but in most applications the value will always be positive. The sign bit could then be tied low, and the lower fifteen bits used to define the input. If a negative value is used this will introduce a 180° phase shift. When the MODE pin is high the state of the RANGE pin is irrelevant, and the magnitude is internally defined to be unity.

The PHASE port has the following data format:

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WEIGHTING in Π radians | $2^{0}$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |

Thus, for example :

+90° (= -270°) = 0100000000000000
-180° (= +180°) = 1000000000000000
-90° (= +270°) = 1100000000000000

The 16 bit radius value is multiplied with the 16 bit internally generated sine and cosine values, to produce a 16 bit result. The RANGE input controls the format of the output data as given below:

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WEIGHTING RANGE = 1 | S | $2^{0}$ | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ |
| RANGE = 0 OR MODE = 1 | S | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| | |
|---|---|
| Supply voltage Vcc | -0.5V to 7.0V |
| Input voltage $V_{IN}$ | -0.5V to Vcc + 0.5V |
| Output voltage $V_{OUT}$ | -0.5V to Vcc + 0.5V |
| Clamp diode current per pin $I_K$ (see note 2) | 18mA |
| Static discharge voltage (HMB) | 500V |
| Storage temperature $T_S$ | -65°C to 150°C |
| Ambient temperature with power applied $T_{AMB}$ | |
| Military | -55°C to +125°C |
| Industrial | -40°C to 85°C |
| Junction temperature | 150°C |
| Package power dissipation | 3500mW |
| Thermal resistances | |
| Junction to Case $Ø_{JC}$ | 5°C/W |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Vcc = Max. Outputs Unloaded, Clock Freq = Max.
5. CMOS levels are defined as
   $V_{IH}$ = Vcc - 0.5v
   $V_{IL}$ = +0.5v
6. Current is defined as negative into the device.
7. $Ø_{JC}$ data assumes that heat is extracted from the top face of the package.

## ELECTRICAL CHARACTERISTICS

### Operating Conditions (unless otherwise stated)

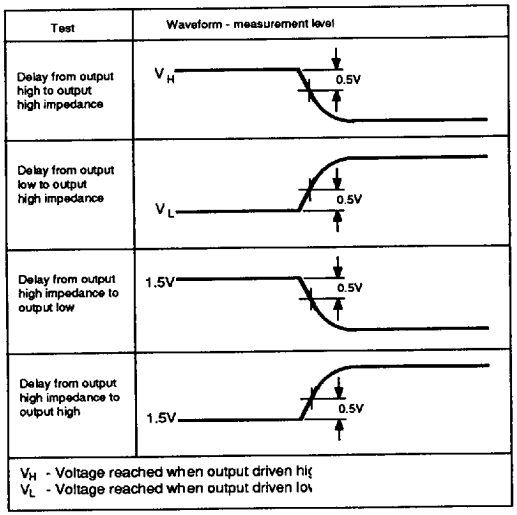
Commercial: $T_{AMB}$ = -0°C to +70°C $T_{J(MAX)}$ = 95°C $V_{CC}$ = 5.0V±5% Ground = 0V
Industrial: $T_{AMB}$ = -40°C to +85°C $T_{J(MAX)}$ = 110°C $V_{CC}$ = 5.0V±10% Ground = 0V
Military: $T_{AMB}$ = -55°C to +125°C $T_{J(MAX)}$ = 150°C $V_{CC}$ = 5.0V±10% Ground = 0V

### Static Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output high voltage | $V_{OH}$ | 2.4 | | - | V | $I_{OH}$ = 4mA |
| Output low voltage | $V_{OL}$ | - | | 0.4 | V | $I_{OL}$ = -4mA |
| Input high voltage | $V_{IH}$ | 3.0 | | - | V | |
| Input low voltage | $V_{IL}$ | - | | 0.8 | V | |
| Input leakage current | $I_{IN}$ | -10 | | +10 | µA | GND < $V_{IN}$ < $V_{CC}$ |
| Input capacitance | $C_{IN}$ | | 10 | | pF | |
| Output leakage current | $I_{OZ}$ | -50 | | +50 | µA | GND < $V_{OUT}$ < $V_{CC}$ |
| Output S/C current | $I_{SC}$ | 10 | | 250 | mA | $V_{CC}$ = Max |

### Switching Characteristics

| Characteristic | Industrial | | | Military | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| M15:0 or P15:0 setup to clock rising edge | 15 | | - | 15 | | - | ns | |
| M15:0 or P15:0 hold after clock rising edge | 4 | | - | 4 | | - | ns | |
| $\overline{MEN}$ or $\overline{PEN}$ setup to clock rising edge | 20 | | - | 20 | | - | ns | |
| $\overline{MEN}$ or $\overline{PEN}$ hold after clock rising edge | 0 | | - | 0 | | - | ns | |
| RANGE setup to clock rising edge | 15 | | - | 15 | | - | ns | |
| RANGE hold after clock rising edge | 8 | | - | 8 | | - | ns | |
| Clock rising edge to all outputs valid | 5 | | 30 | 5 | | 30 | ns | 30pF |
| Clock freq | DC | | 20 | DC | | 20 | MHz | |
| Clock High Time | 15 | | - | 15 | | - | ns | |
| Clock Low Time | 20 | | - | 20 | | - | ns | |
| $\overline{OER}$,$\overline{OEI}$ low to data valid | - | | 20 | - | | 20 | ns | see Fig. 6 |
| $\overline{OER}$,$\overline{OEI}$ high to data high impedance | - | | 20 | - | | 20 | ns | see Fig. 6 |
| Pipeline delay VIN to VOUT | 28 | | 28 | 28 | | 28 | CLKs | |
| Vcc Current (CMOS inputs) | - | | 430 | - | | 450 | mA | see Note 4 |
| Vcc Current (TTL inputs) | - | | 460 | - | | 500 | mA | see Note 4 |



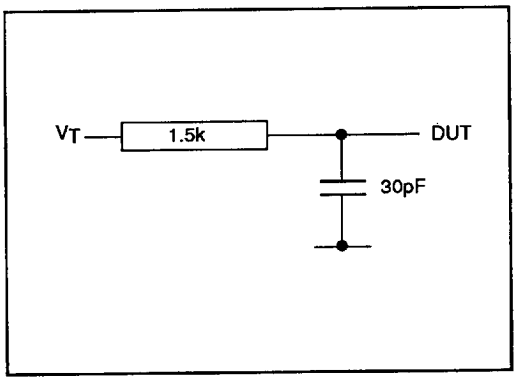




*Fig. 6 Tri-state delay measurement load.*

## ORDERING INFORMATION

**Commercial (0°C to +70°C)**
PDSP16340 / C0 / AC (20MHz - PGA)
PDSP16340 / C0 / GC (20MHz - QFP)

**Industrial (-40°C to +85°C)**
PDSP16340 / B0 / AC (20MHz - PGA)
PDSP16340 / B0 / GC (20MHz - QFP)

**Military (-55°C to +125°C)**
PDSP16340 / A0 / AC (20MHz - PGA)
PDSP16340 / A0 / GC (20MHz - QFP)

Call for availability of High Rel parts and MIL 883C screening.