Quad ISDN 2B1Q Echocanceller Digital Front End

DFE-Q V2.1

PEF 24911 Version 2.1

This Delta Sheet lists the add-on features and differences between the DFE-Q V2.1 and the DFE-Q V1.3.

1 Power Supply

The DFE-Q V2.1 requires a +3.3 V ±0.3 V power supply. The inputs and outputs remain 5 V TTL compatible.

Table 1 Power Consumption

Mode	Typ. values	Max. values	Unit	Test conditions
Power-up all Channels	85	100	mA	3.3 V, open outputs, inputs at V_{DD} /V_{SS}
Power-down	35	t.b.d.	mA	3.3 V, open outputs, inputs at V_{DD} /V_{SS}

All measurements of the power consumption are performed with random 2B+D data in active states, 3.3 V (0° C - 70° C)

PEF 24911 Revision History:	**2000-12-01**	DS 6
Previous Version:	09.00	DS 5
Major changes since last revision: MTO Function removed State Diagram updated		
Previous Version:	06.00	DS 4
Major changes since revision 05.99: Typical values of Power Consumption added Delay for Recognition of C/I code changed 2nd time MON 8 Messages in State ’Reset’		

2 Pinning

Table 2 lists the changes that were made concerning the pinning, **Table 3** specifies new pin functions that were introduced with version 2.1.

Table 2 Pinning Changes

Pin No.	V2.1	V1.3	Comment
32	PUP	N.C.	additional push-pull mode for pin DOUT eases interface adaptation
36	n.c.	DSYNC	obsolete
55	SLOT0	SLOT	renamed
45	SLOT1	N.C.	increased max data rate (4 MBit/s) requires an additional SLOT pin
53	LT	LT	dedicated LT mode pin is obsolete
56	SSP	TSP	dedicated pin for ’Send Single Pulses’ test mode
58	PBX	PBX	function removed
62	DT	TP	dedicated pin for ’Data Through’ test mode
63	TRST	TP1	BScan power-on-reset is replaced by a dedicated reset line

Table 3 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
32	PUP	I (PD)	Push Pull Mode in push pull mode ’0’ and ’1’ is actively driven during an occupied time-slot, outside the active time-slots DOUT is high impedance (tristate) ’1’= configures DOUT as push/pull output ’0’= configures DOUT as open drain output
55	SLOT0	I	IOM®-2 Channel Slot Selection 0 assigns IOM®-2 channels in blocks of 4 SLOT1, 0: ’00’= IOM®-2 channels 0 to 3 ’01’= IOM®-2 channels 4 to 7 ’10’= IOM®-2 channels 8 to 11 ’11’= IOM®-2 channels 12 to 15
45	SLOT1	I (PD)	IOM®-2 Channel Slot Selection 1 assigns IOM®-2 channels in blocks of 4
53	LT	I	reserved, clamp to one
56	SSP	I	Send Single Pulses (SSP) Test Mode enables/disables SSP test mode ’1’= SSP test mode enabled, alternating +/-3 pulses are issued at the four line ports in 1.5 ms intervals ’0’= SSP test mode disabled
58	PBX	I	reserved, clamp to zero

Table 3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
62	DT	I	Data Through (DT) Test Mode enables/disables DT test mode '1'= DT test mode enabled, the U-transceiver is forced on all line ports to enter the 'Transparent' state '0'= DT test mode disabled
63	TRST	I (PU)	JTAG Boundary Scan Disable resets the TAP controller state machine (asynchronous reset), internal pullup '1'= reset inactive '0'= reset active

PU:Pull Up

PD:Pull Down

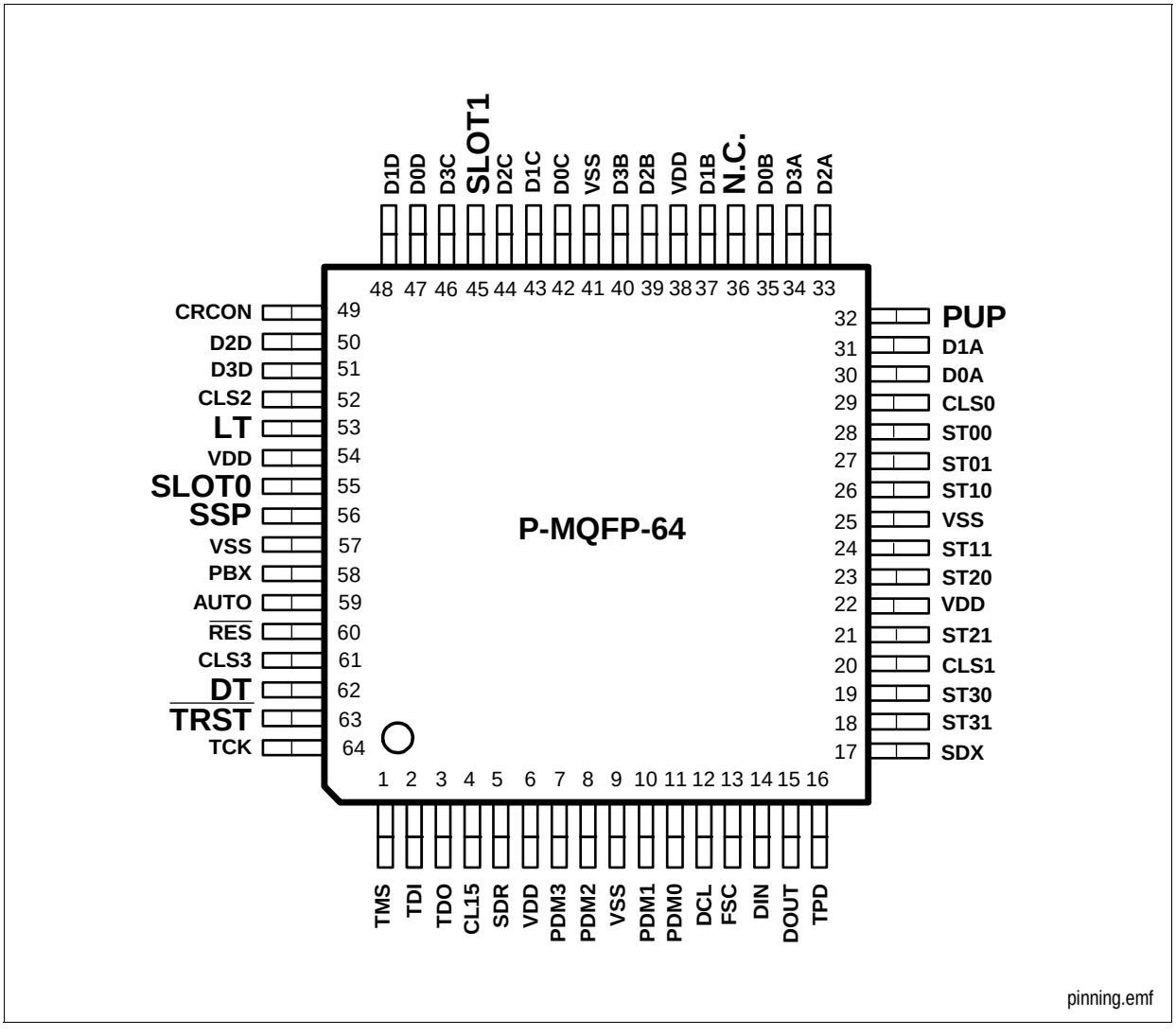

Figure 1 Pin Diagram of the DFE-Q V2.1

3 Max. Data Rate On IOM®-2 Doubled

With version 2.1 the maximum data rate on IOM®-2 is doubled from 2 MBit/s to 4MBit/s. The 4MBit/s mode corresponds to a DCL frequency of 8192 kHz.

4 MON-12 Protocol

MON-12 commands feature via the IOM®-2 Monitor channel direct access to the device internal register map. The MON-12 protocol works in the manner of a serial microprocessor interface.

New functions such as digital local loopbacks, BER measurement etc. are only accessible via MON-12 commands. Functions that were so far provided via MON-8 commands, e.g. FEBE/NEBE counter status retrieval, can be accessed as well via the MON-12 protocol. For a detailed description of the register set please refer to the data sheet of the DFE-Q V2.1

5 Bit Error Rate Measurement

For bit error rate monitoring the DFE-Q V2.1 features an 16-bit Bit Error Rate counter (BERC) per line. As soon as the BER function is enabled zeros are sent in the selected channels and incoming ones are counted until the BER function has been disabled again by the user.

6 Advanced Filter Options for MON-0 and MON-2 Messages

Additionally to the existing mode pins, AUTO and CRCON, the internal MFILT register provides a wide range of filter options for the passing on of MON-0 and MON-2 messages. The new MON-12 protocol gives access to the MFILT register. The following options are provided,

– MON-0:	Transparent, On Change, TLL	in transparent mode
	TLL (Triple-Last-Look)	in automode
– MON-2:	On Change, TLL, CRC, CRC & TLL	vs. IOM®-2
	On Change, TLL, CRC, CRC & TLL	vs. State Machine

7 Digital Local Loops

Besides the remote loopback stimulation and the local analog loopback (C/I= ARL) the DFE-Q V2.1 features digital local loopbacks via its internal register set. The local loopbacks that are additionally provided by the LOOP register are shown in **Figure 2**. The local loops can be activated at any time independent of the current activation status using the MON-12 protocol.

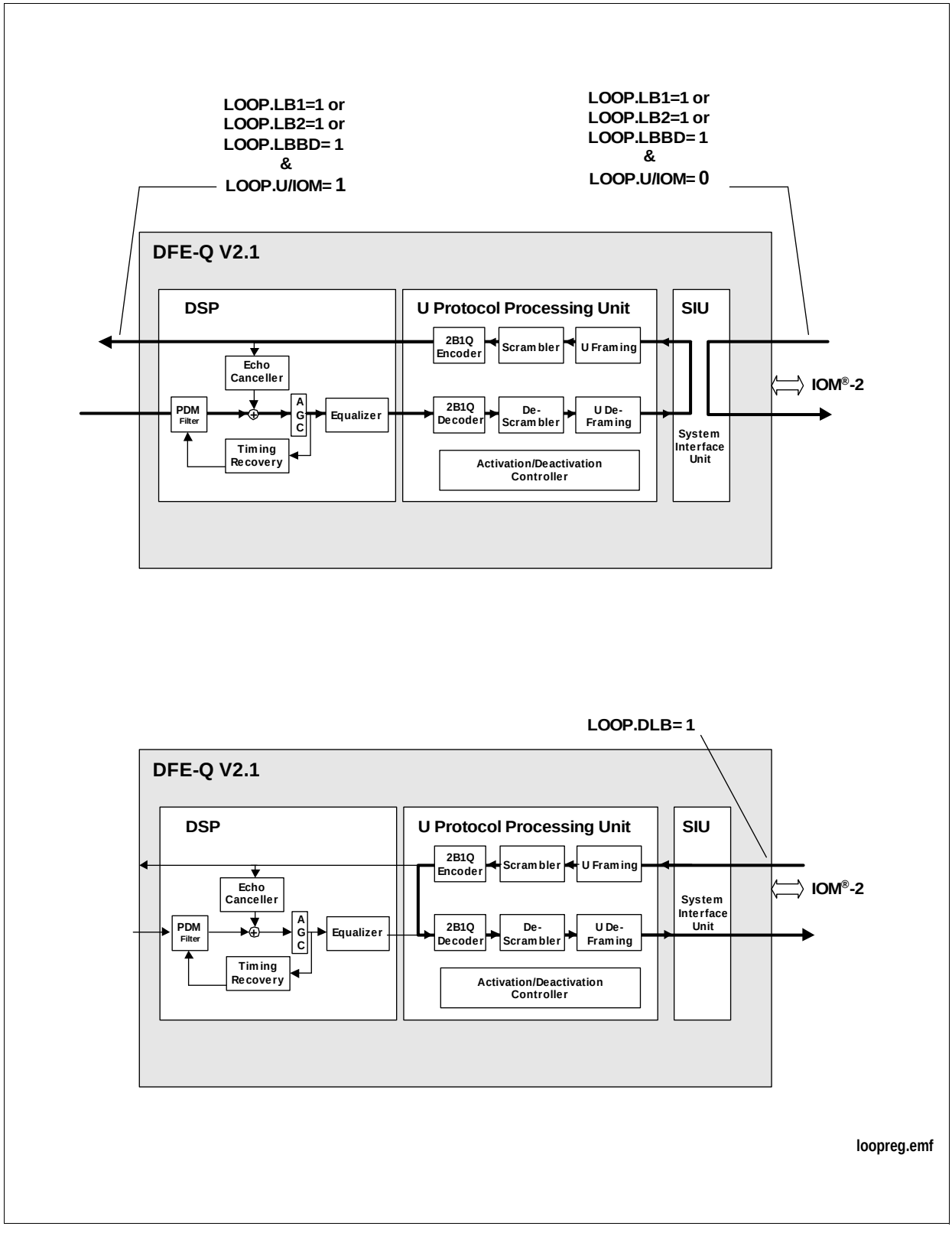

Figure 2 Loopbacks Featured by Register LOOP

8 D-Channel Arbitration

D-channel arbitration is not supported by version 2.1.

9 C/I code ’LTD’ omitted

The C/I command ’LTD’ is no more supported, since the LTD function corresponds to that of C/I ’RES’. Upon C/I ’RES’ the DFE-Q V2.1 stops transmitting signals on U and ignores wake-up signals.

On contrast to the DFE-Q V1.x the relay driver and status pins are not affected by the software reset C/I ’RES’ in version 2.1. The relay driver and status pins are only reset by a hardware reset.

10 State Machine

Some minor changes were made regarding the state machine. The improvements are summarized and listed in **Table 4**. See also the state diagrams in **Figure 3** (V2.1) and **Figure 4** (V1.3).

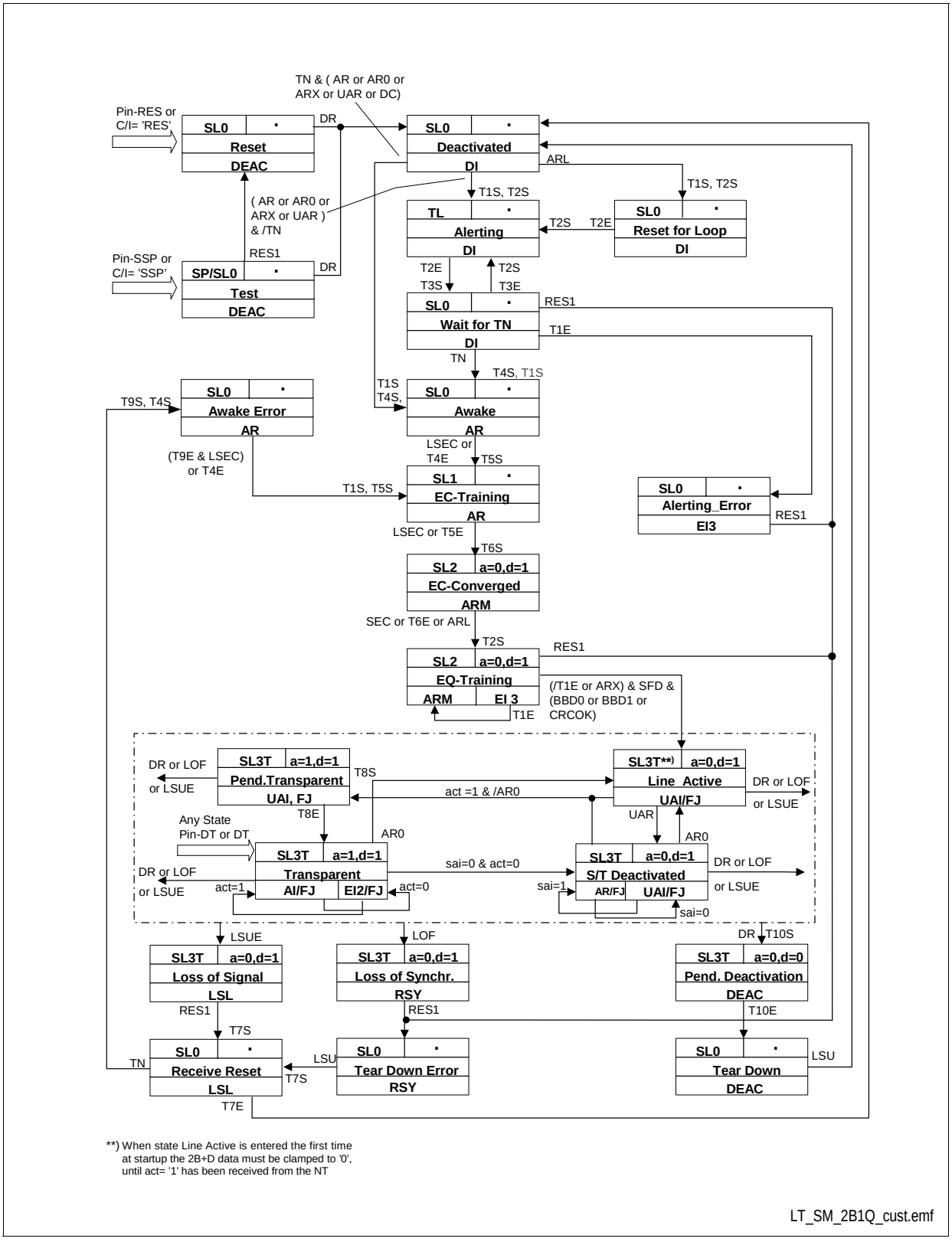

Figure 3 State Diagram of V2.1

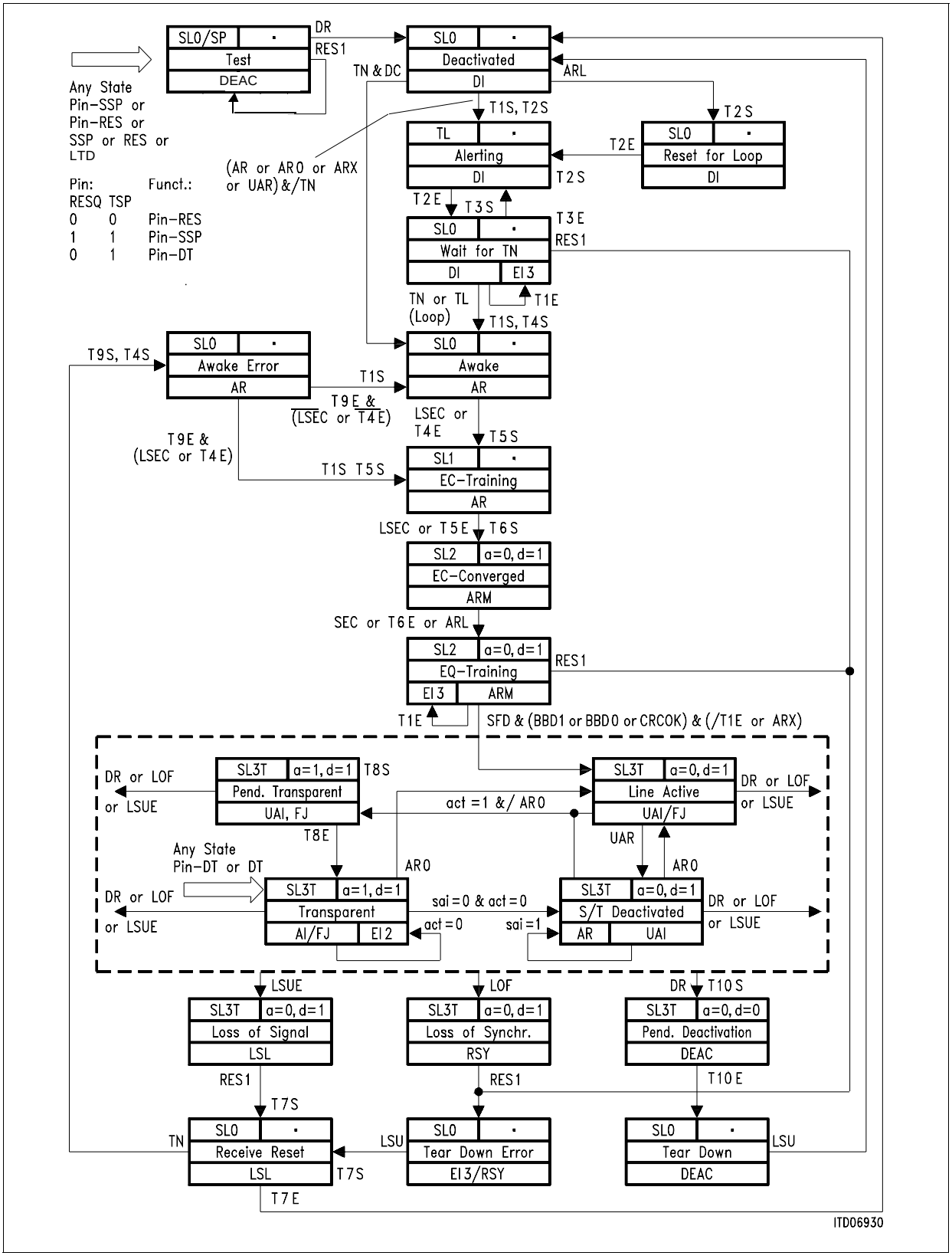

Figure 4 State Diagram of V1.3

Table 4 Differences to LT-SM of DFE-Q V1.3

No.	V1.3 State/ Signal	Change in V2.1	Comment
1.	'Test' State	split into two states - Reset State - Test State	defined reset and test states
2.		state 'Alerting Error'	introduced for a clear separation of the normal operation state from the error condition state (which will result in a deactivation)
3.	state 'Transparent'	C/I code output in state 'Transparent' dependent on received act bit	
4.	state 'S/T Deactivated'	C/I code output in state 'S/T Deactivated' dependent on sai bit status	
5.	C/I code LTD	C/I code 'LTD' is omitted	function corresponds to that of C/I 'RES'
6.	C/I code INT	C/I code 'INT' is not supported	INT was listed in former documents of V1.x due to an editorial fault

11 RITL/WLL Functions

RITL/WLL functions are not supported by the DFE-Q version 2.1.

12 Retrieving Coefficients

MON-8 commands with bit r=1, that were defined for former versions, are no more supported.

13 Boundary Scan Instruction Set

The Boundary-Scan instructions ’CLAMP’ and ’HIGHZ’ are introduced in version 2.1. The instruction ’SSP’ and ’DT’ are omitted since these test functions can be triggered either by the pins SSP and DT or - channel selective - by the C/I codes SSP and DT.

CLAMP allows the state of the signals included in the boundary scan driven from the PEB 24911 to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. These output signals driven from the DFE-Q V2.1 will not change while CLAMP is selected.

HIGHZ sets all output pins included to the boundary scan path into a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by the DFE-Q V2.1 outputs without incurring the risk of damage to the DFE-Q V2.1.

Table 5 TAP Controller Instructions

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing
0011	IDCODE	Reading ID code
0100	CLAMP	Reading outputs
0101	HIGHZ	Z-State of all boundary scan output pins
1111	BYPASS	Bypass operation

14 Version Update of the Boundary Scan IDCODE Register

Version	Device Code	Manufacturer Code		Output
0001	0000 0000 0111 0010	0000 1000 001	1	--> TDO

15 MON-8 AID Version Identification

On receiving the MON-8 Command RID the DFE-Q responds with the MONITOR message AID coded 8006_H .

This code is unique for version 2.1 with respect to other DFE-Q versions

16 Recognition delay of C/I code changes

The DFE-Q V2.1 has implemented a new architecture for low power consumption. Furthermore it is developed for complete compatibility in MONITOR and C/I messages. The new architecture , however, leads to changes in response times compared to former versions, that could affect the compatibility to software with rigid time-out settings.

The evaluation of changes of the incoming C/I-code takes longer than in former versions of the PEB 24911:

- Recognition of changes to unconditional commands (I.e.: to RES, SSP, and DT) takes up to 2,5 msec instead of 0.25 msec in former versions
- In the C/I channel in states ’Test’ and ’Reset’ recognition of changes can also take up to 2,5 msec instead of 0.25 msec in former versions
- In states other than ’Reset’ or ’Test’ recognition of changes to all other conditional commands takes up to 0,5 ms instead of 0.25 msec in former versions

The C/I codes shall be repeated at least the times above, before the C/I code may be changed. Surveillance timers have to be set to values beyond the named times.

17 MON-8 messages in State ’Reset’

The issuing of MON-8 messages has been improved in state ’Reset’

If the state ’Reset’ is entered due to a hardware reset (pin $\overline{\text{RES}}$=0) the device will issue a MON-8 message AST afterwards if one of the pins STxy is high to communicate this status to the system software.

The usage of MON-8 commands is not blocked during a Software Reset, i.e. the C/I-command RES is applied. Even while the SW-reset is activated, the relay driver pins can be programmed by the MON-8 message SETD, and the status pins can be read with RST messages or will autonomously communicate changes of the status. The device will also answer on a RID-command with a AID-message.

18 C/I-channel indication in Hardware Reset

As long as pin $\overline{\text{RES}}$ is low, the issued C/I-code is DI (1111_b) instead of DEAC (0001_b) for all channels. After putting $\overline{\text{RES}}$ to high the C/I-codes change to DEAC.