CMOS INPUT/OUTPUT EXPANDER (TLCS-48C)

TMP82C43P

1. GENERAL DESCRIPTION AND FEATURES

The TMP82C43P is an input/output expander designed specifically to provide a low cost means of I/O expansion for the TLCS-48C family.

The I/O ports of the TMP82C43P serve as a direct extension of the resident I/O facilities of the TLCS-48C microcomputers and are accessed by their own MOVD, ANLD and ORLD instructions.

FEATURES

- CMOS LSI for low power dissipation
- Simple interface to TLCS-48C microcomputers
- Four 4-bit I/O ports
- Single 5V supply
- High output drive
- PIN compatible with intel's 8243
- Extended operation temperature range −40°C to 85°C

2. PIN CONNECTION AND PIN FUNCTIONS

2.1 Pin Connection (Top View)

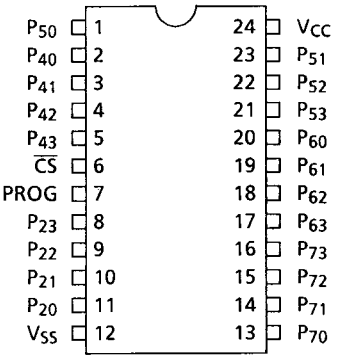


Figure 2.1 DIP Pin Connections

2.2 BLock Diagram

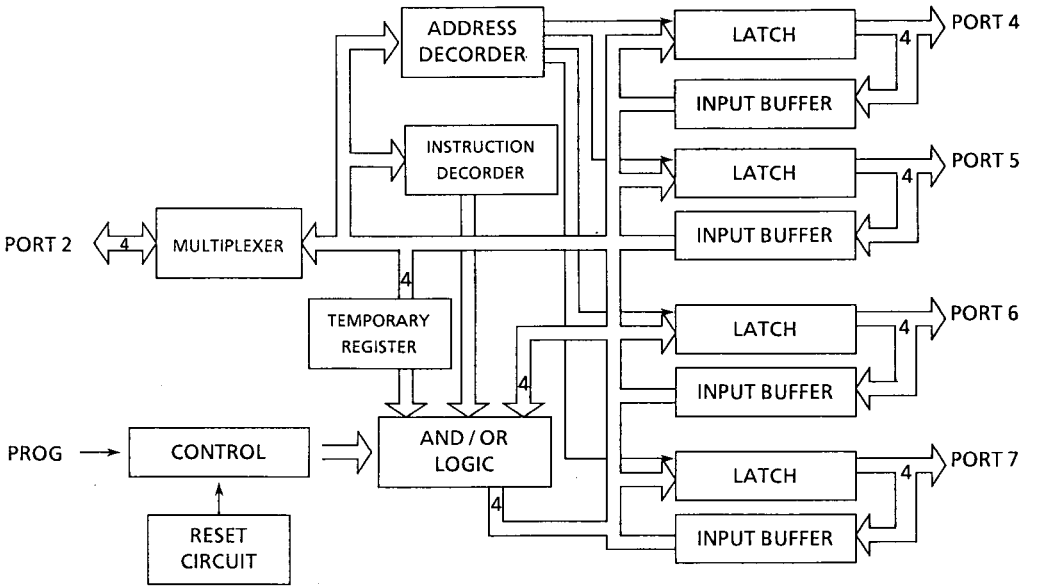


Figure 2.2 Block Diagram

2.3 Pin Names And Pin Description

PROG (Input)

Clock input. A high to low transistion on PROG signifies that address and control are available on P_{20-23}, and a low to high transition signifies that data is available on P_{20-23}.

$\overline{CS}$ (Input)

Chip Select Input. A high on $\overline{CS}$ inhibits any change of output or internal status.

P_{20-23} (Input/Output, 3-state)

Four (4) bit bi-directional port contains the address and control bits on a high to low transition of PROG. During a low to high transition it, contains the data for a selected output port if a write operation, or the data from a selected port before the low to high transition if a read operation.

P_{40-43}, P_{50-53}, P_{60-63}, P_{70-73} (Input/Output, 3-state)

Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write) or a 3-state (after read). Data on pins P_{20-23} may be directly written, ANDed or ORed with previous data.

V_{CC} (Power)

+5 volt supply

V_{SS} (Power)

0 volt supply

3. FUNCTIONAL DESCRIPTION

3.1 General Operation

The TMP82C43P contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports.

- Transfer accumulator to port
- Transfer port to accumulator
- AND accumulator to port
- OR accumulator to port

All communication between the microcomputer (TMP80C49A) and the TMP82C43P occurs over Port 2 (P_{20-23}) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles.

A high to low transition of the PROG line indicates that address is present while a low to high transition indicates the presence of data. Additional TMP82C43P may be added to the 4-bit bus and chip select signal using additional output lines from the microcomputer.

3.2 Power On Initialization

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1V.

P21	P20	ADDRESS CODE	P23	P22	INSTRUCTION CODE
0	0	PORT 4	0	0	Read
0	1	PORT 5	0	1	Write
1	0	PORT 6	1	0	ORLD
1	1	PORT 7	1	1	ANLD

3.3 Write Modes

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi, A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi, A takes new data AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

3.4 Read Mode

The device has one read mode. The operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are 3-stated, and the input buffers switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the 3-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode).

If modes are changed during operation, the first read following a write should be ignored ; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the TMP82C43P output. A read of any port will leave that port in a high impedance state.

4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

SYMBOL	ITEM	RATING
V_{CC}	V_{CC} Supply Voltage with Respect to GND	− 0.5V to + 7.0V
V_{IN}	Input Voltage with Respect to GND	− 0.5V to V_{CC} + 0.5V
P_D	Power Disspation	250mW
T_{SOLDER}	Soldering Temperature (soldering Time 10 sec.)	260°C
T_{STG}	Storage Temperature	− 65°C to + 150°C
T_{OPR}	Operating Temperature	− 40°C to + 85°C

4.2 D.C. Characteristics (I)

T_{OPR} = − 40°C to 85°C, V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage		− 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.2	—	V_{CC}	V
V_{OL1}	Output Low Voltage Ports 4-7	I_{OL} = 5mA	—	—	0.45	V
V_{OL2}	Output Low Voltage Port 7	I_{OL} = 20mA	—	—	1.0	V
V_{OL3}	Output Low Voltage Port 2	I_{OL} = 0.8mA	—	—	0.45	V
V_{OH11}	Output High Voltage Ports 4-7	I_{OH} = − 1.2mA	2.4	—	—	V
V_{OH21}	Output High Voltage Port 2	I_{OH} = − 0.6mA	2.4	—	—	V
V_{OH12}	Output High Voltage Ports 4-7	I_{OH} = − 0.6mA	V_{CC} − 0.8	—	—	V
V_{OH22}	Output High Voltage Port 2	I_{OH} = − 0.3mA	V_{CC} − 0.8	—	—	V
I_{IL1}	Input Leakage Port 4-7	$V_{SS} \leqq V_{IN} \leqq V_{CC}$	—	—	± 10	μA
I_{IL2}	Input Leakage Port 2, $\overline{CS}$, PROG	$V_{SS} \leqq V_{IN} \leqq V_{CC}$	—	—	± 10	μA
I_{CC1}	Power Supply Current (1)	V_{CC} = 5V, V_{IL} = 0.2V, V_{IH} = V_{CC}-0.2V, PROG PERIOD = 5μS	—	—	2	mA
I_{CC2}	Power Supply Current (2)	V_{CC} = 5V, V_{IL} = 0.2V, V_{IH} = V_{CC}-0.2V, PROG = V_{CC}-0.2V,	—	—	10	μA
I_{OL}	Sum of all I_{OL} of 16 Outputs	5mA Each pin	—	—	80	mA

4.3 D.C. Characteristics (II)

T_{OPR} = −40°C to 85°C, V_{CC} = 5V ± 20%, V_{SS} = 0V

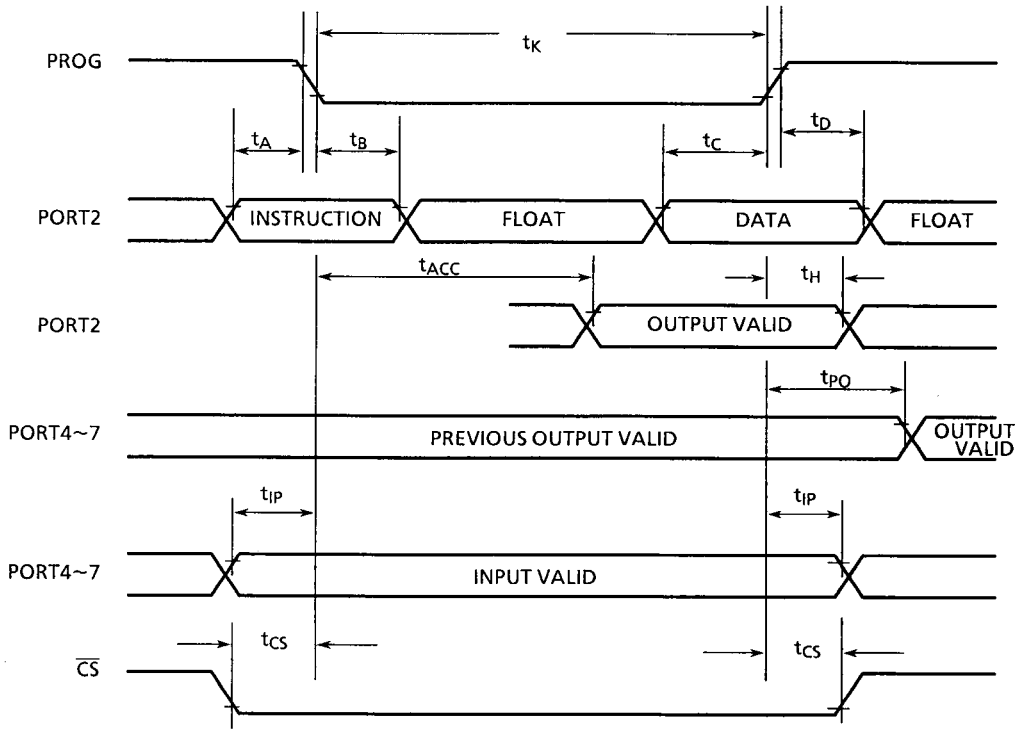
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage	$4.0 \leqq V_{CC} \leqq 4.5V$	−0.5	—	$0.15V_{CC}$	V
V_{IH}	Input High Voltage	$5.5 \leqq V_{CC} \leqq 6.0V$	$0.5V_{CC}$	—	V_{CC}	V
V_{OL1}	Output Low Voltage Ports 4-7	I_{OL} = 4mA	—	—	0.45	V
V_{OL2}	Output Low Voltage Port 7	I_{OL} = 15mA	—	—	1.0	V
V_{OL3}	Output Low Voltage Port 2	I_{OL} = 0.6mA	—	—	0.45	V
V_{OH12}	Output High Voltage Ports 4-7	I_{OH} = −200μA	V_{CC} − 0.8	—	—	V
V_{OH22}	Output High Voltage Port 2	I_{OH} = −100μA	V_{CC} − 0.8	—	—	V
I_{OL}	Sum of all I_{OL} of 16 outputs	4mA Each Pin	—	—	64	mA

4.4 A.C. characteristics

T_{OPR} = −40°C to 80°C, V_{CC} = 5V ± 20%, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
t_A	Code Valid Before PROG	C_L = 80pF	100	—	—	ns
t_B	Code Valid After PROG	C_L = 20pF	60	—	—	ns
t_C	Data Valid Before PROG	C_L = 80pF	200	—	—	ns
t_D	Data Valid After PROG	C_L = 20pF	20	—	—	ns
t_H	Floating After PROG	C_L = 20pF	0	—	150	ns
t_K	PROG Negative Pulse Width		700	—	—	ns
t_{CS}	$\overline{CS}$ Valid Before/After PROG		50	—	—	ns
t_{PO}	Ports 4-7 Valid After PROG	C_L = 100pF	—	—	700	ns
t_{IP}	Ports 4-7 Valid Before/After PROG		100	—	—	ns
t_{ACC}	Port 2 Valid After PROG	C_L = 80pF	—	—	650	ns

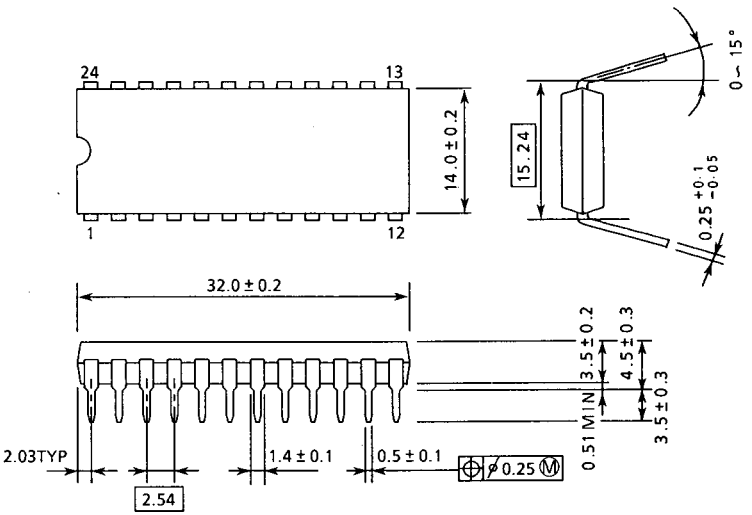
4.5 Timing Waveform



5. OUTLINE DRAWINGS

DIP24-P-600

Unit : mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.