The following information applies to the N- iteration of the MA31750.

Console Mode is an optional feature of MIL-STD-1750 processors in general and is mentioned in MIL-STD-1750. The mode is provided within the MA31750 to allow the system designer to control, monitor and modify internal operation of the processor without having to substantially rewrite system software. This Applications Note describes this mode in detail, giving information on the commands available and the external hardware required to support the Console. This Note updates and corrects the previous issues for the relevant iterations.

OVERVIEW

The processor can operate in one of a number of different modes. One of these is Console mode where the normal MIL-STD-1750 operation is suspended and a special debugging interface is presented instead.

Console mode may be entered by either hardware or software means. When in Console mode the processor receives its instructions from a fixed IO-mapped location. Operands and results (as appropriate) associated with these instructions are passed between system and processor via two other fixed locations in the IO map. Any number of Console commands may be performed before issuing a special command which returns control back to the interrupted 1750 program.

Note that the two interval timers, Timer A and Timer B, are stopped on entry to Console mode, in accordance with MIL-STD-1750.

ENTERING CONSOLE MODE USING CONREQN

Asserting CONREQN low for 2 machine cycles during normal operation will cause the processor to enter Console mode following the completion of the current instruction (but see note on Console inhibit). Whilst CONREQN is low, the device will loop round three machine cycles, one of which will perform a read of the command register (8402_{16}). The command is not executed whilst CONREQN remains low. CONREQN may stay low for as long as required. The user should load the system Console Command register with the desired command before asserting CONREQN high, at which point the requested command will be executed. The flowchart shows the remainder of the command operation. See Table 1 for command information.

ENTERING CONSOLE MODE WITH BPT

If the processor encounters a BPT instruction the processor will enter Console mode (but see note on Console inhibit) and will immediately process the Console command contained in the Command register. It is important, therefore, that the Command register is loaded before any BPT instructions may be encountered. Operation then continues as for CONREQN-initiated commands (see flowchart).

CONSOLE INHIBIT

When CONREQN is asserted low, the CPU checks its internal copy of the configuration register to see if a console is present. If console is entered via the BPT instruction, the CPU reads the system configuration word, hence giving dynamic control over console entry by BPT. If no console is declared in the configuration, CONREQN is ignored and BPT instructions are treated as NOPs.

CONTROLLING THE PROCESSOR IN CONSOLE MODE

When in Console mode the processor communicates with the system console via a number of locations in IO space, as listed below:

Address	Function
8402_{16}	Console command input
$C000_{16}$	Data input
4000_{16}	Data output
$C001_{16}$	Read Console Status (not used in MA31750)
4001_{16}	Clear Console (not used in MA31750)

The user should provide a method of supplying values when these addresses are polled by the processor. A typical approach is to implement three IO-mapped registers which respond to the above addresses and which may be loaded from an external controller or banks of switches.

The required action is communicated to the processor by placing the appropriate command at IO location 8402_{16} and asserting CONREQN high. If the command takes an operand (such as a value to Write Register) then this should first be placed at location $C000_{16}$. Following completion of the command, any results are returned via location 4000_{16}. Note that during XIO and Next XIO operations, external read XIO commands execute an extra read of the Data input register. This does not affect the operation in any way. Also note that the IO addresses $C001_{16}$ and 4001_{16} are enabled when Console mode is selected, but is not used as part of the Console Mode operation.

Following the execution of the first command, the processor will halt (provided the command is not 'continue') and wait for a further negative edge on CONREQN. The next command to be executed should be set at address 8402_{16} before the rising edge of CONREQN. Any number of commands may be issued in this way, using CONREQN to control execution and to signal the presence of a new command code to the processor.

LEAVING CONSOLE MODE

To release the MA31750 from Console mode, a 'continue' command should be issued. The instruction pipeline will be refilled with the 1750 instruction immediately following the point at which the Console request or BPT was registered; normal instruction execution then resumes from that point.

SINGLE STEP

Single step operation is also accomplished using a 'continue' command. Once Console mode has been entered, raising CONREQN will cause the processor to execute the command and leave Console mode. If the user reasserts CONREQN low after the 2nd internal cycle after the read and before the 2nd pipe-line pre-fetch, then exactly one 1750 instruction will be executed before the processor returns to Console mode. This allows the processor to step through the 1750 code one instruction at a time.

COMMAND SUMMARY

Table 1 shows a summary of all commands available in Console mode, with a description of their function. Commands should be constructed according to Figure 1. It should be noted that although many of the internal registers are made available in Console mode, attempting to change them may produce predictable but unexpected results. In particular, temporary registers T0, T1 and T9-T11 are used by the Console interface to store operands such as the IC register prior to Console Mode entry.

Command	Function	Code
Continue	Resumes normal MIL-STD-1750 operation. This command is also used for single stepping instructions.	0
Read Register	Places the contents of a specified internal register into the Console Output register (IO address 4000). The register to be accessed is specified as a value placed in the lower 12 bits of the Command register according to Table 2.	1
Write Register	Places the contents of the Console Input register (IO location C000) into a specified internal register. The register to be accessed is specified as a value placed in the lower 12 bits of the Command register according to Table 2.	2
Read and Clear Fault Register	Places the contents of the 1750 Fault register into the Console Output register and then clears the Fault Register.	3
Write Status Word	Copies the contents of the Console Input register to the 1750-defined Status Word register. Note that the A reg is changed to 200E.	4
Read memory	The contents of operand memory space at address A (the contents of the Alternate Address register) are placed in the Console Output register.	5
Write memory	The contents of the Console Input register are placed in operand memory space at address A.	6
Read next memory	The contents of the A register is incremented. The contents of operand memory space at address A are then placed in the Console Output register.	7
Write next memory	The contents of the A register is incremented. The contents of the Console Input register are then placed in operand memory space at address A.	8
XIO	The XIO command specified by the content of the A register is performed using data read from the Console Input register. If the XIO command is illegal the command is ignored. No Status Word Processor State checking is performed.	9
Next XIO	As above, but the command in A is incremented before the XIO is attempted.	A
Disable	Console operation is suspended pending a new Console request or an interrupt. If an interrupt occurs then the Instruction Counter will be restored and normal MIL-STD-1750 operation will be resumed with the interrupt service routine.	B
Reserved	Reserved for internal use by GPS - do not use.	C
Other...	Any other command not described above is ignored and has no action. User should reload Command register with correct value as for a new instruction.	X

Table 1: Console Instructions

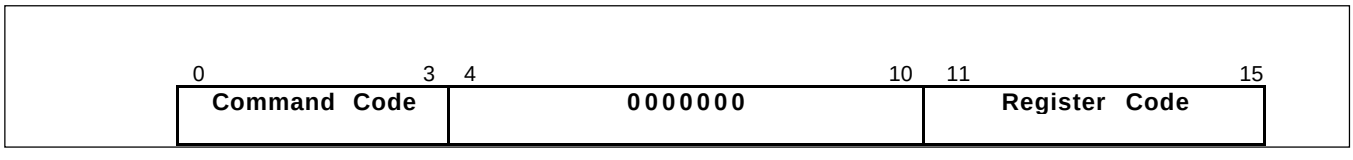

Figure 1: Command Register Format

Register	Register Description	Code (bottom 12 bits)
R0-R15	General purpose register R0-R15	000-00F
T0-T11	Microcode registers T0-T11	010-01B
A	Operand or alternate address register	01C
IC	Instruction Counter (take great care when modifying this value)	01D

Table 2: Register Map

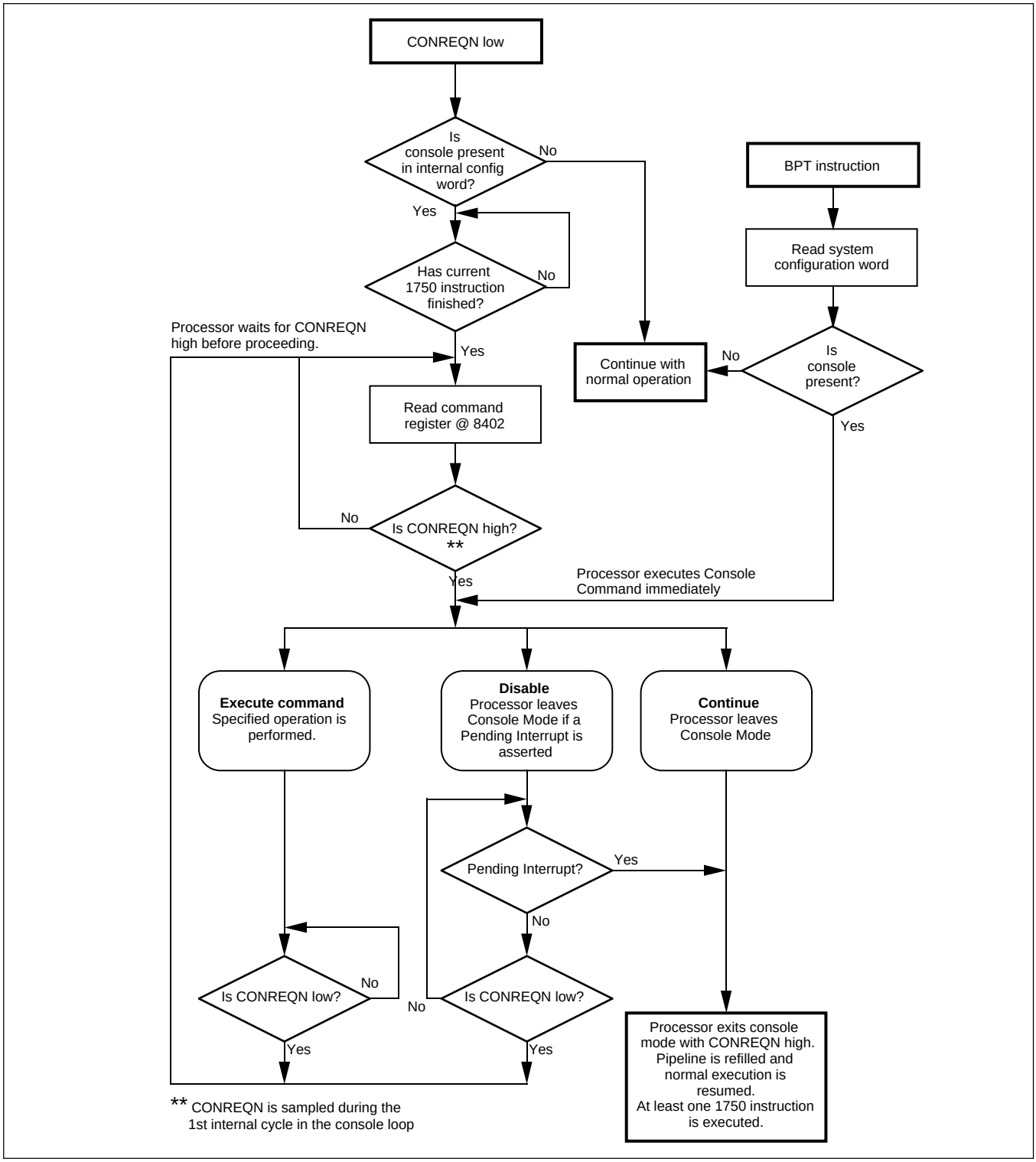

Figure 2: Console Operation Flowchart

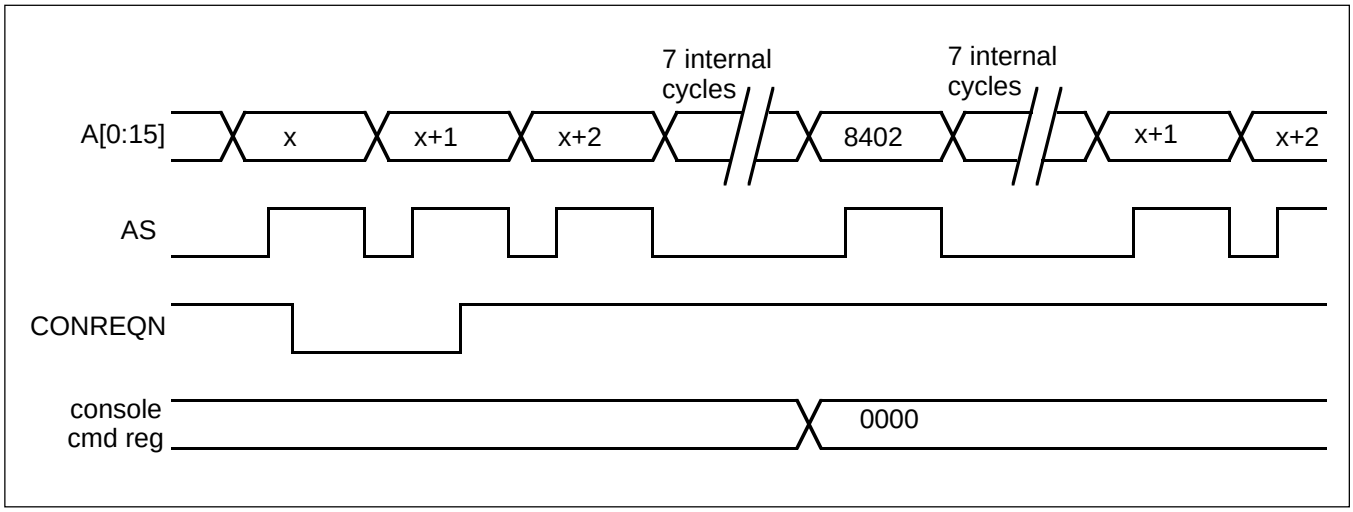

Figure 3: Entering Console Mode

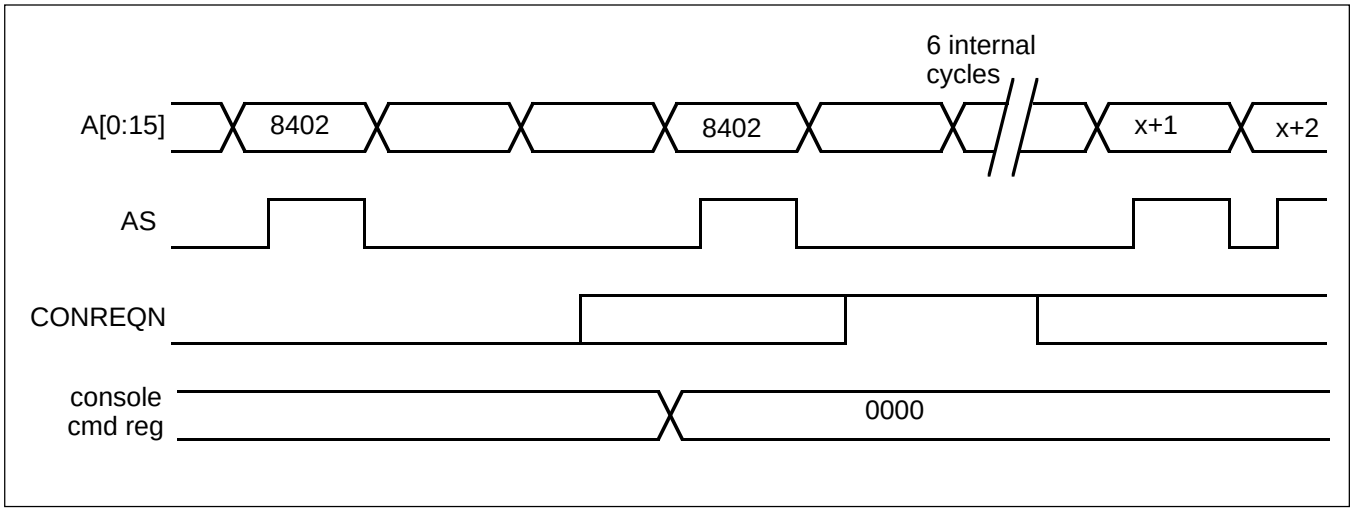

Figure 4: Exiting Console Mode

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