

**8-bit 20 MSPS Flash A/D Converter (TTL I/O)**

**Description**

The CXA1096M is an 8-bit 20 MSPS high speed A/D converter IC. This IC is suitable for a wide range of applications where A/D high speed operation is required.

**Features**

- Resolution 8-bit  $\pm 1/2$  LSB
- High speed operation 20MSPS
- Wide band analog input 8MHz ( $-3$ dB)
- Low input capacitance 30pF (Typ.)
- Low power consumption 390mW (Typ.)
- I/O level TTL
- Two ways of power supply (Single +5V or dual +5V/-5.2V)
- Sample and Hold amplifier not required
- Binary or Two's complement mode
- Over range output



**Structure**

Bipolar silicon monolithic IC

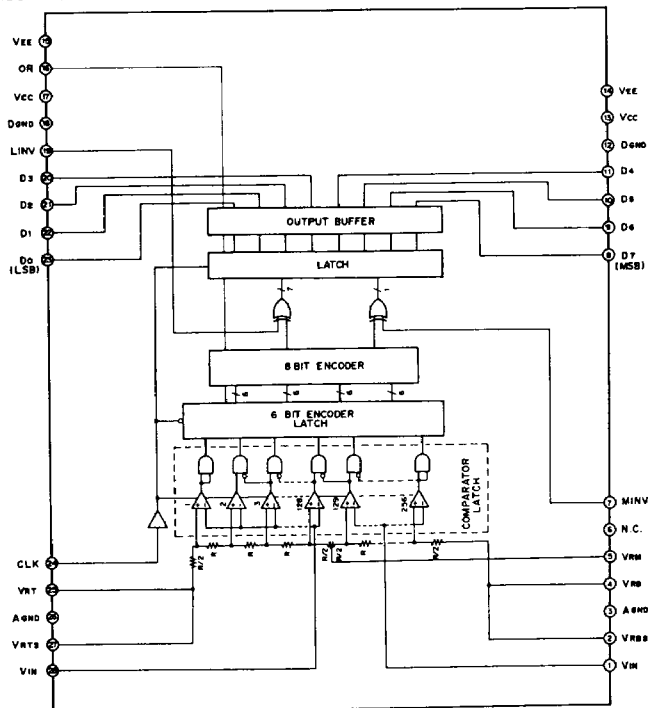
**Applications**

- Digital TV
- High speed signal processing

**Function**

8-bit, 20MSPS flash A/D converter

**Block Diagram**



**Absolute Maximum Ratings (Ta = 25°C)**

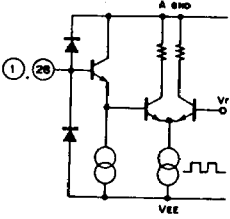
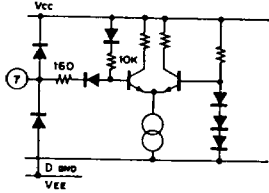
|                               |                 |                  |    |
|-------------------------------|-----------------|------------------|----|
| • Supply voltage              | VCC—DGND        | 0 to +6          | V  |
|                               | VEE—AGND        | 0 to -6          | V  |
|                               | AGND—DGND       | 0 to +6          | V  |
| • Input voltage(analog)       | VIN             | VEE to AGND +0.3 | V  |
| • Input voltage (reference)   | VRT, VRB, VRM   | VEE to AGND +0.3 | V  |
|                               | VRT - VRB       | 2.5              | V  |
| • Input current (VRM)         | IVRM            | -3 to +3         | mA |
| • Input voltage (digital)     | CLK, MINV, LINV | DGND-0.5 to VCC  | V  |
| • Storage temperature         | Tstg            | -55 to +150      | °C |
| • Allowable power dissipation | PD              | 0.83             | W  |

**Recommended Operating Conditions**

|                                     |            |                        |    |
|-------------------------------------|------------|------------------------|----|
| • Supply voltage<br>(Single supply) | VCC, AGND  | 4.75 to 5.25           | V  |
|                                     | DGND, VEE  | 0                      | V  |
| • (Dual supply)                     | VCC        | 4.75 to 5.25           | V  |
|                                     | VEE        | -5.5 to -4.75          | V  |
|                                     | DGND, AGND | 0                      | V  |
|                                     |            |                        |    |
| • Reference input                   | VRT        | AGND -0.1 to AGND +0.1 | V  |
|                                     | VRB        | AGND -2.2 to AGND -1.8 | V  |
| • Analog input                      | VIN        | VRB to VRT             |    |
| • Clock pulse width                 | TPW1       | 35 (Min.)              | ns |
|                                     | TPW0       | 10 (Min.)              | ns |
| • Operating temperature             | Topt       | -20 to +75             | °C |

Pin Description and Equivalent Circuit

| No.                 | Symbol   | Voltage  | Equivalent circuit | Description   |
|---------------------|----------|--|--------------------|---|
| 8 to 11<br>20 to 23 | D0 to D7 | TTL  |                    | Digital data output pin<br>D0 (LSB) to D7 (MSB)   |
| 16                  | OR       |  |                    | Over range output pin   |
| 12, 18              | DGND     | GND  |                    | Digital GND<br>Separated from AGND  |
| 13, 17              | Vcc      | 5V (Typ)   |                    | Digital power supply  |
| 14, 15              | VEE      | GND<br>(Single supply)<br>- 5V<br>(Dual supply)              |                    | Analog power supply   |
| 19                  | LINV     | TTL  |                    | Input pins for output<br>polarity inversion of D0<br>(LSB) to D6 (See the<br>Input-Output Reference<br>and Output Format)<br>when open "1" is<br>maintained |
| 24                  | CLK      | TTL  |                    | Clock input pin   |
| 25                  | VRT      | 5V (Typ)<br>(Single supply)                                  |                    | Reference voltage<br>(Top)  |
| 27                  | VRTS     | GND<br>(Dual supply)   |                    | Reference voltage sense<br>(Top)  |
| 4                   | VRB      | 3V (Typ)<br>(Single supply)<br>- 2V (Typ.)<br>(Dual supply)  |                    | Reference voltage<br>(Bottom)   |
| 2                   | VRBS     |  |                    | Reference voltage sense<br>(Bottom)   |
| 5                   | VRM      | 4V (Typ.)<br>(Single supply)<br>- 1V (Typ.)<br>(Dual supply) |                    | Middle point of reference<br>voltage can be used as<br>the compensation pin<br>for linearity  |

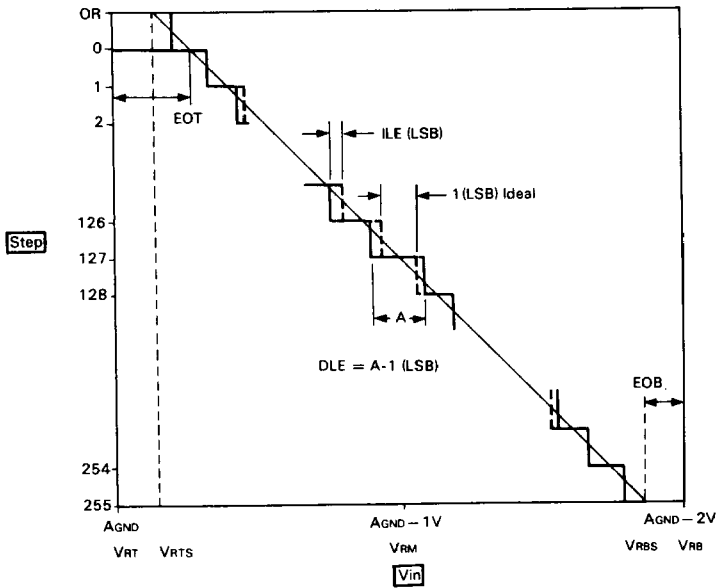
| No.   | Symbol | Voltage  | Equivalent circuit  | Description   |
|-------|--------|--|---|---|
| 3, 26 | AGND   | 5V (Typ.)<br>(Single supply)<br>GND<br>(Dual supply) |   | Analog power supply   |
| 1, 28 | VIN    | VRT to VRB   |  | Analog input<br>Pin 1 and 28 should<br>be connected together.                             |
| 7     | MINV   | TTL  |  | Input pin for output polarity<br>inversion of D7 (MSB)<br>when open "1" is<br>maintained. |

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Input-Output Reference and Output Format

| Vin      | Step | MINV | 1          | 1          | 0          | 0          |        |     |
|----------|------|------|------------|------------|------------|------------|--------|-----|
|          |      | LINV | 1          | 0          | 1          | 0          | OR MSB | LSB |
| AGND     | 0    | 0    | 000...00   | 0 011...11 | 0 100...00 | 0 111...11 | OR MSB | LSB |
|          |      | 1    | 000...00   | 1 011...11 | 1 100...00 | 1 111...11 | OR MSB | LSB |
|          |      | 1    | 000...01   | 1 011...10 | 1 100...01 | 1 111...10 | OR MSB | LSB |
| AGND -1V | 127  | 1    | 011...11   | 1 000...00 | 1 111...11 | 1 100...00 | OR MSB | LSB |
|          |      | 128  | 1 100...00 | 1 111...11 | 1 000...00 | 1 011...11 | OR MSB | LSB |
|          |      |      |            |            |            |            |        |     |
| AGND -2V | 254  | 1    | 111...10   | 1 100...01 | 1 011...10 | 1 000...01 | OR MSB | LSB |
|          |      | 255  | 1 111...11 | 1 100...00 | 1 011...11 | 1 000...00 | OR MSB | LSB |
|          |      | 1    | 111...11   | 1 100...00 | 1 011...11 | 1 000...00 | OR MSB | LSB |

1: VIH, VOH  
0: VIL, VOL



**Electrical Characteristics  
(Single supply)**

VCC = +5V, DGND = 0V, AGND = +5V, VEE = 0V,  
VRT = +5V, VRB = +3V, Ta = 25°C

| Item                              | Symbol                            | Test condition   | Min.                     | Typ. | Max.  | Unit |    |
|-----------------------------------|-----------------------------------|--|--------------------------|------|-------|------|----|
| Maximum conversion rate           | F <sub>C</sub>                    | V <sub>IN</sub> = 5 to 3V<br>F <sub>IN</sub> = F <sub>C</sub> /4 - 1 kHz | 20                       |      |       | MSPS |    |
| Supply current                    | I <sub>CC</sub> + I <sub>EE</sub> |  | 56                       | 71   | 91    | mA   |    |
| Reference pin current             | I <sub>REF</sub>                  |  | 11                       | 15   | 18    | mA   |    |
| Analog input bandwidth            | BW                                |  | 8                        |      |       | MHz  |    |
| Analog input capacitance          | C <sub>IN</sub>                   | V <sub>IN</sub> = 4V + 0.07V <sub>rms</sub>                              |                          | 30   | 35    | pF   |    |
| Analog input bias current         | I <sub>IN</sub>                   | V <sub>IN</sub> = 4V   | 15                       | 50   | 110   | μA   |    |
| Reference resistance (VRT to VRB) | R <sub>REF</sub>                  |  |                          | 130  |       | Ω    |    |
| Offset voltage                    | V <sub>RT</sub>                   | E <sub>OT</sub>  | 8                        | 13   | 19    | mV   |    |
|                                   | V <sub>RB</sub>                   | E <sub>OB</sub>  | 0                        | 5    | 11    | mV   |    |
| Digital input voltage             | V <sub>IH</sub>                   |  | 2.0                      |      |       | V    |    |
|                                   | V <sub>IL</sub>                   |  |                          |      | 0.8   | V    |    |
| Digital input current             | I <sub>IH</sub>                   | V <sub>CC</sub> = Max.   | V <sub>IH</sub> = 2.7V   | 0    | -100  | -150 | μA |
|                                   | I <sub>IL</sub>                   |  | V <sub>IL</sub> = 0.5V   | -0.1 | -0.32 | -0.5 | mA |
| Digital output voltage            | V <sub>OH</sub>                   | V <sub>CC</sub> = Min.   | I <sub>OH</sub> = -500μA | 2.7  | 3.4   |      | V  |
|                                   | V <sub>OL</sub>                   |  | I <sub>OL</sub> = 3mA    |      |       | 0.5  | V  |
| Output data delay                 | T <sub>D<sub>LH</sub></sub>       | LOAD 1   |                          | 15   | 19    | 22   | ns |
|                                   | T <sub>D<sub>HL</sub></sub>       |  |                          | 22   | 27    | 31   | ns |
| Non linearity                     | E <sub>L</sub>                    | F <sub>C</sub> = 20 MSPS<br>V <sub>IN</sub> = 5 to 3V                    |                          |      | ± 1/2 | LSB  |    |
| Differential non linearity        | E <sub>D</sub>                    |  |                          |      | ± 1/2 | LSB  |    |
| Differential gain error           | DG                                | NTSC 40 IRE mod. ramp,<br>F <sub>C</sub> = 14.3 MSPS                     |                          |      | 1.5   | %    |    |
| Differential phase error          | DP                                |  |                          |      | 0.5   | deg. |    |
| Aperture jitter                   | E <sub>AP</sub>                   |  |                          | 30   |       | ps   |    |
| Sampling delay                    | t <sub>ds</sub>                   |  | 5                        | 7    | 9     | ns   |    |

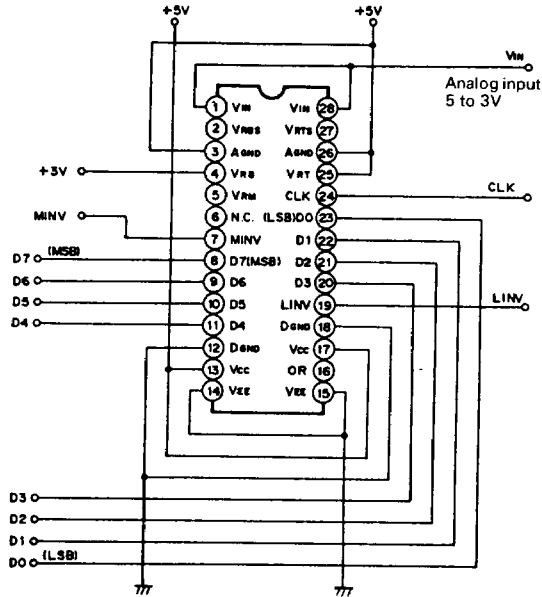
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**Electrical Characteristics**  
**(Dual supply)**
 $V_{CC} = +5V$ ,  $DGND = 0V$ ,  $AGND = 0V$ ,  $V_{EE} = -5V$ ,  
 $V_{RT} = 0V$ ,  $V_{RB} = -2V$ ,  $T_a = 25^\circ C$ 

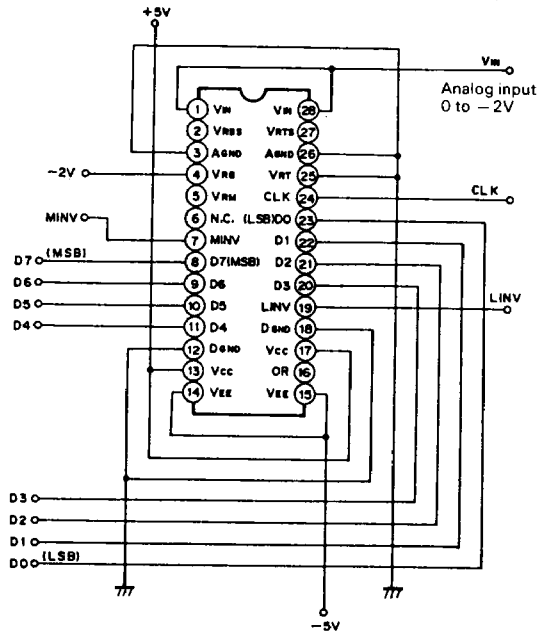
| Item  | Symbol    | Test condition                                    |                      | Min. | Typ.  | Max.      | Unit     |
|---|-----------|---|----------------------|------|-------|-----------|----------|
| Maximum conversion rate                       | FC        | $V_{IN} = 0$ to $-2V$<br>$F_{IN} = F_C/4 - 1$ kHz |                      | 20   |       |           | MSPS     |
| Supply current                                | $I_{CC}$  |   |                      | 7    | 10    | 14        | mA       |
|   | $I_{EE}$  |   |                      | 50   | 62    | 78        | mA       |
| Reference pin current                         | $I_{REF}$ |   |                      | 11   | 15    | 18        | mA       |
| Analog input bandwidth                        | BW        |   |                      | 8    |       |           | MHz      |
| Analog input capacitance                      | $C_{IN}$  | $V_{IN} = -1V + 0.07V_{rms}$                      |                      |      | 30    | 35        | pF       |
| Analog input bias current                     | $I_{IN}$  | $V_{IN} = -1V$                                    |                      | 15   | 50    | 110       | $\mu A$  |
| Reference resistance ( $V_{RT}$ to $V_{RB}$ ) | $R_{REF}$ |   |                      |      | 130   |           | $\Omega$ |
| Offset voltage                                | $V_{RT}$  | $E_{OT}$  |                      | 8    | 13    | 19        | mV       |
|   | $V_{RB}$  | $E_{OB}$  |                      | 0    | 5     | 11        | mV       |
| Digital input voltage                         | $V_{IH}$  |   |                      | 2.0  |       |           | V        |
|   | $V_{IL}$  |   |                      |      |       | 0.8       | V        |
| Digital input current                         | $I_{IH}$  | $V_{CC} = \text{Max.}$                            | $V_{IH} = 2.7V$      | 0    | -100  | -150      | $\mu A$  |
|   | $I_{IL}$  |   | $V_{IL} = 0.5V$      | -0.1 | -0.32 | -0.5      | mA       |
| Digital output voltage                        | $V_{OH}$  | $V_{CC} = \text{Min.}$                            | $I_{OH} = -500\mu A$ | 2.7  | 3.4   |           | V        |
|   | $V_{OL}$  |   | $I_{OL} = 3mA$       |      |       | 0.5       | V        |
| Output data delay                             | $T_{DLH}$ | LOAD 1  |                      | 15   | 19    | 22        | ns       |
|   | $T_{DHL}$ |   |                      | 22   | 27    | 31        | ns       |
| Non linearity                                 | EL        | $F_C = 20$ MSPS<br>$V_{IN} = 0$ to $-2V$          |                      |      |       | $\pm 1/2$ | LSB      |
| Differential non linearity                    | ED        |   |                      |      |       | $\pm 1/2$ | LSB      |
| Differential gain error                       | DG        | NTSC 40 IRE mod. ramp,<br>$F_C = 14.3$ MSPS       |                      |      |       | 1.5       | %        |
| Differential phase error                      | DP        |   |                      |      |       | 0.5       | deg.     |
| Aperture jitter                               | EAP       |   |                      |      | 30    |           | ps       |
| Sampling delay                                | tds       |   |                      | 5    | 7     | 9         | ns       |

Application Circuit and Electrical Characteristics Test Circuit  
Single supply

1)

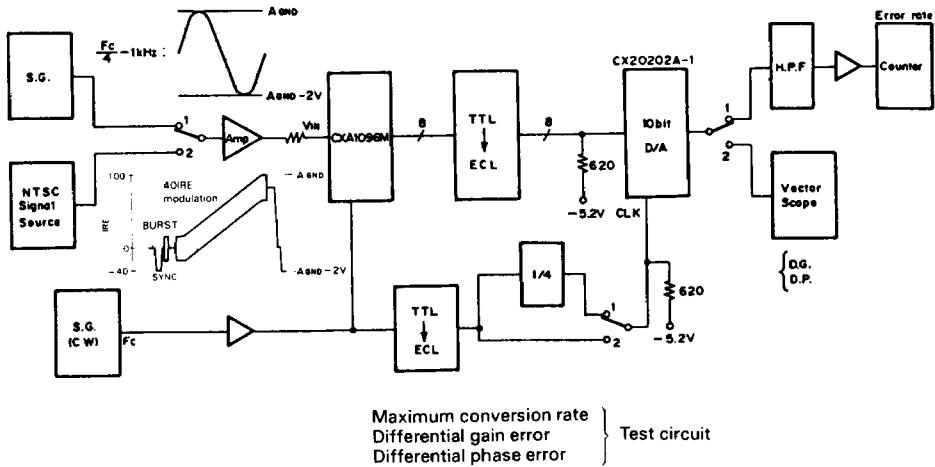
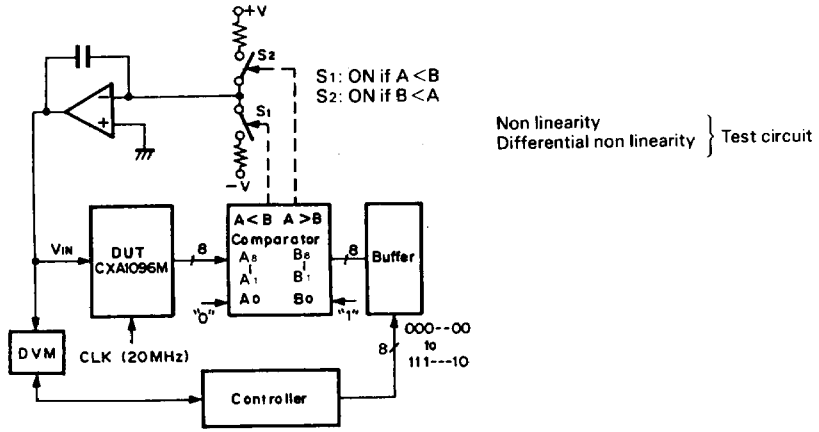


Dual supply

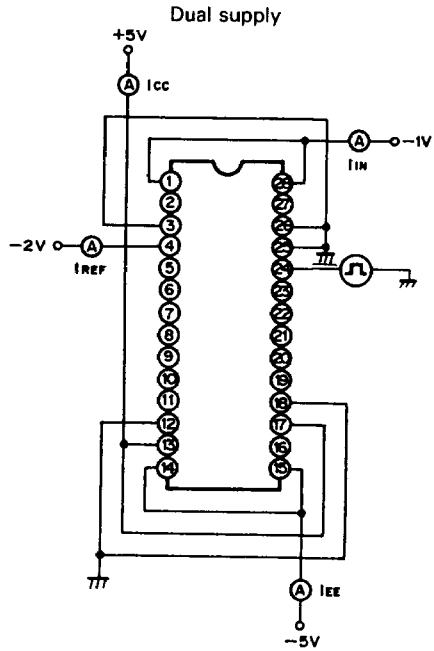
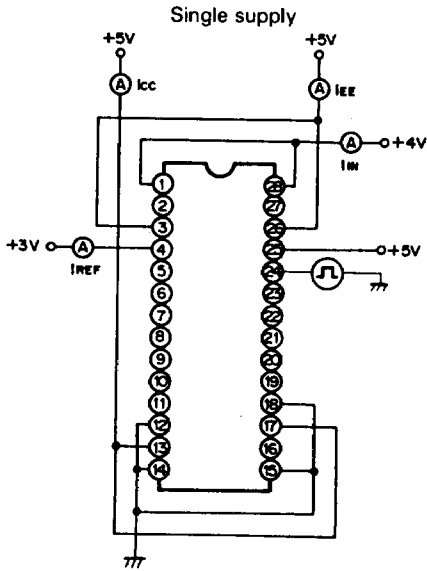


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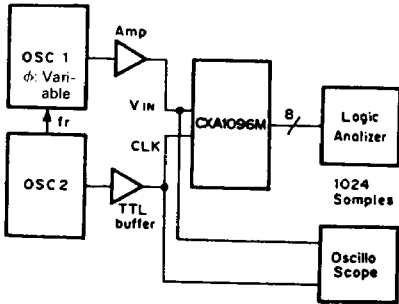
2)



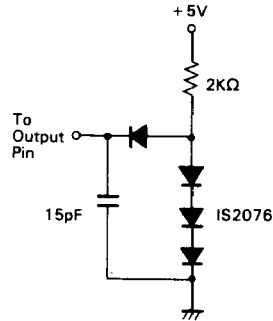
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**Note)** VIN pin is connected to VRT pin for ICC and IEE measurement.

Supply current  
 Analog input bias current  
 Reference pin current } Test circuit

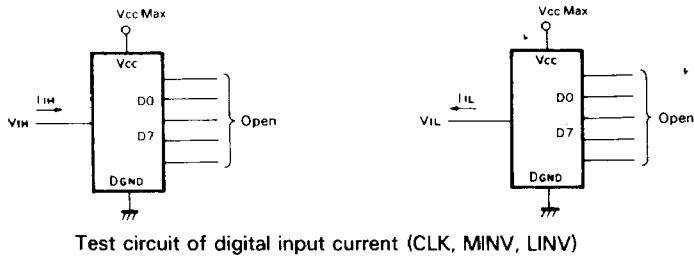
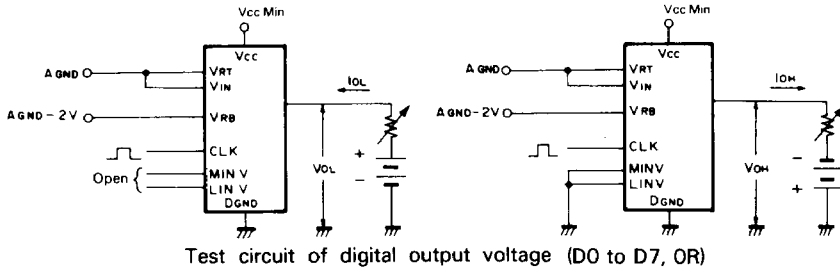


Aperture jitter  
 Sampling delay } Test circuit

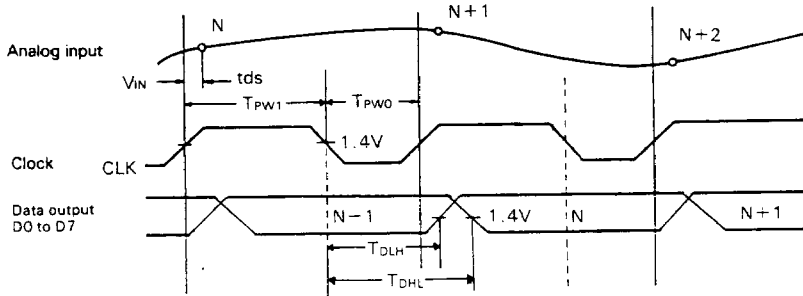


LOAD1 Test Load for Output data delay

3)

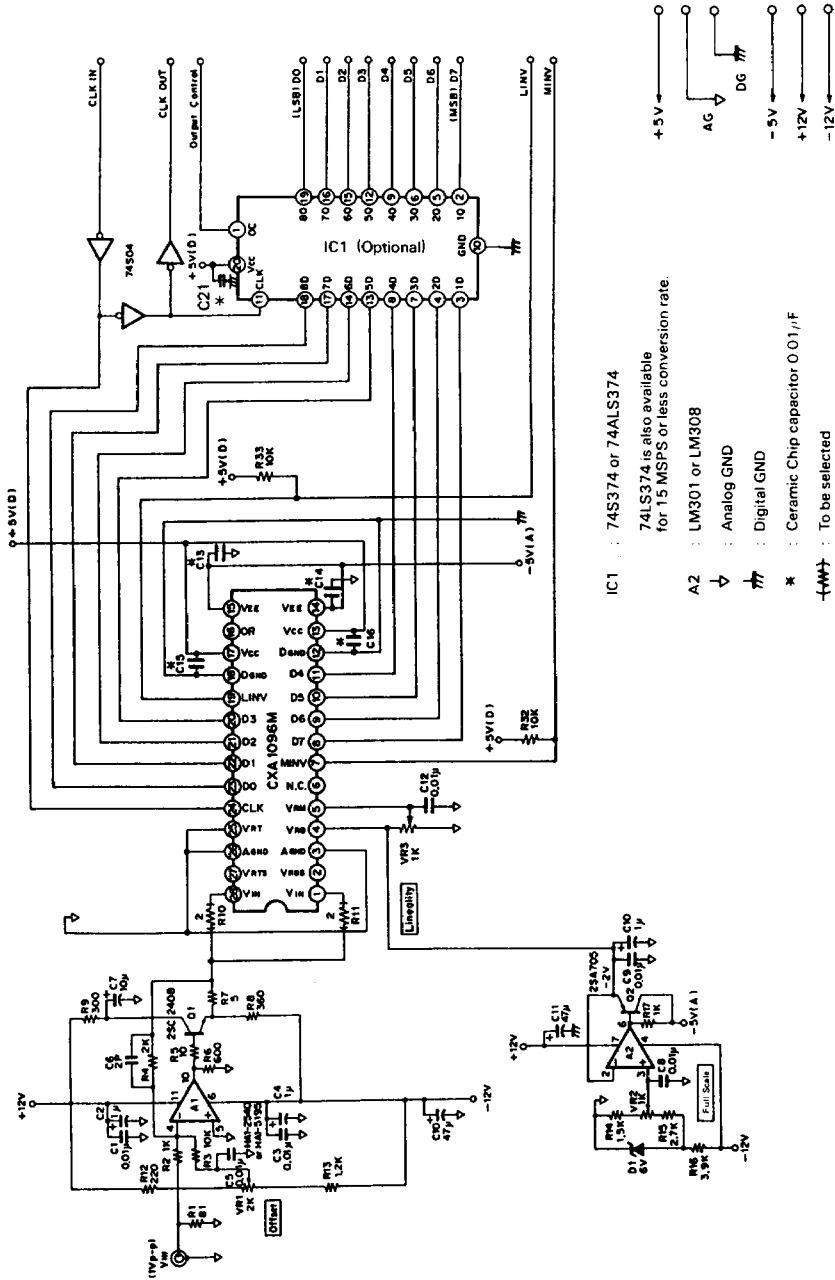


Timing Chart



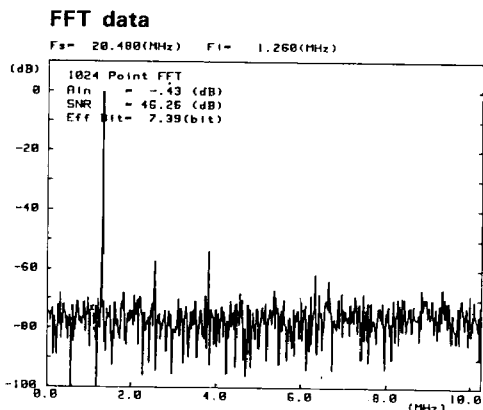


Application Circuit (Dual supply)

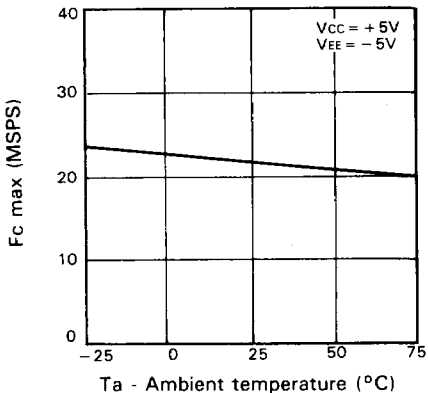


## Notes on Application

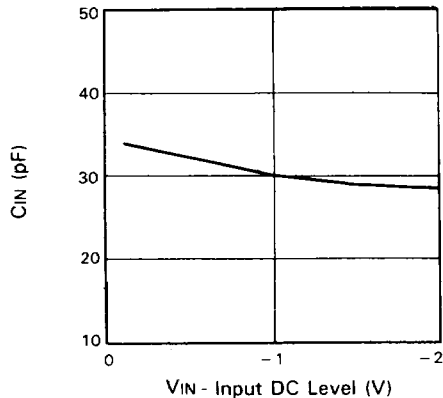
- Each of DGND pins (12, 18) and each of VCC Pins (13, 17) are divided in internal circuit. All of the pins should be connected to respective PCB patterns.
- Layout of the analog and digital sections should be separated to reduce noise effect.  
VEE pins to AGND and VCC pins to DGND should be bypassed as closely as possible by means of  $1\mu\text{F}$  and  $0.01\mu\text{F}$  capacitors.  
For the  $0.01\mu\text{F}$ , a ceramic chip capacitor should be used.
- The input capacitance of the analog input is much smaller than that of the Flash Type A/D converters in use so far. It is necessary to use an amplifier with sufficient band width and driving power.  
Pins VIN (1, 28) are divided in it, so they should be connected together. When driving with a low output impedance amplifier, parasitic oscillation may occur. This can be prevented by introducing between the amplifier output and A/D input a small resistance of 2 to  $10\Omega$  with smaller inductance, in series. And, that also each VIN pins are divided with small resistances (shown in the Application Circuit) is effective.  
The amplifier output and A/D input should be connected as closely as possible.
- Voltage between VRT to VRB is equivalent to the dynamic range of the analog input. VRB pin should be bypassed to AGND by means of  $1\mu\text{F}$  and  $0.01\mu\text{F}$  capacitors.  
Through bypassing VRM pin with a  $0.01\mu\text{F}$  capacitor to AGND, characteristics at high frequency become more balanced. Also, VRM pin can be used as a trimming pin for more precise linearity compensation.
- CLK line should be wired in short distance and that should be separated from the other section to reduce the inductive.
- Analog input signal is sampled at the positive going edge of the CLK, and a corresponding digital data appears to the output parts at the negative going edge with a short delay time (TDLH, TDHL).  
If digital data will be latched externally, it should be latched at the negative going edge. (See the Timing Chart)
- It is recommended to connect free pins to AGND for prevention of noise effect.



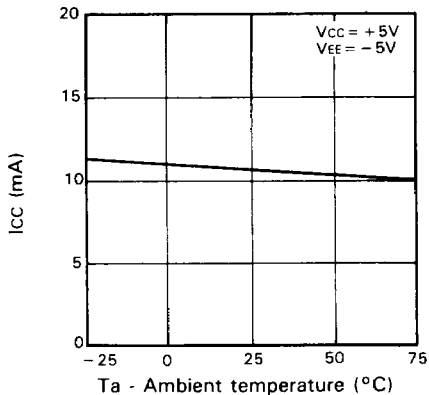
**Fc max vs. Ambient temperature**



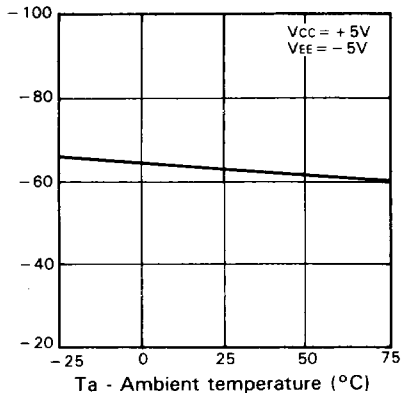
**CIN vs. VIN - Input DC level**



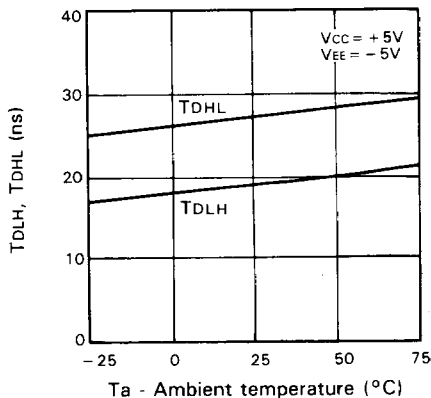
**ICC vs. Ambient temperature**



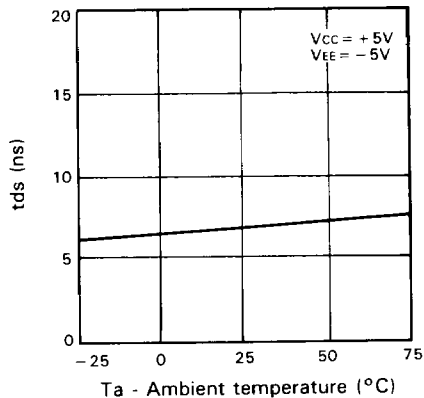
**IEE vs. Ambient temperature**



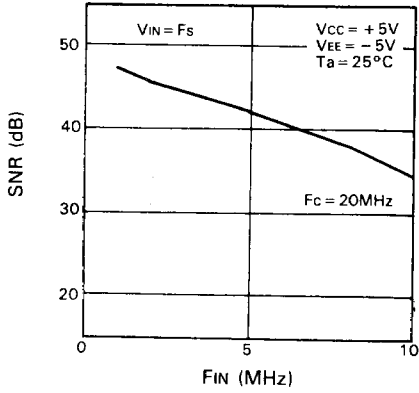
**TDLH, TDHL vs. Ambient temperature**



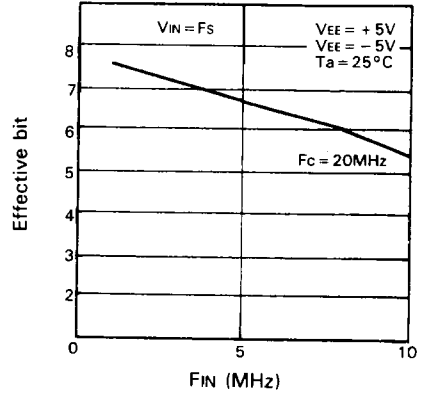
**tds vs. Ambient temperature**



SNR vs.  $F_{IN}$

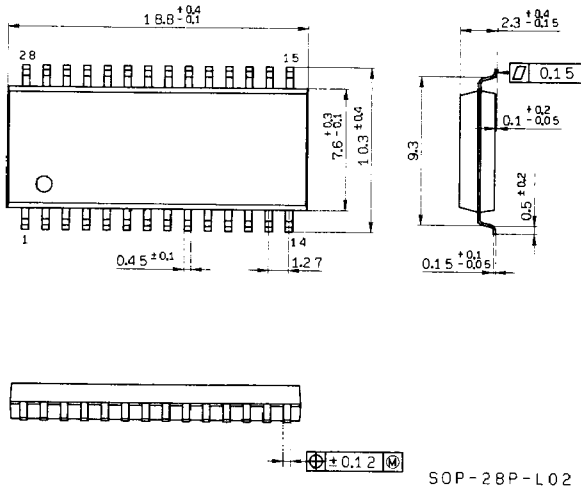


Effective bit vs.  $F_{IN}$



Package Outline Unit : mm

28pin SOP(Plastic) 375mil 0.6g



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