DS3144DK
Quad DS3/E3 Framer
Demo Kit Daughter Card

www.maxim-ic.com

GENERAL DESCRIPTION

The DS3144DK is an easy-to-use evaluation board for the DS3144 quad DS3/E3 framer. It is intended to be used as a daughter card with the DK101 motherboard or the DK2000 motherboard. The DS3144DK comes complete with a DS3144 quad framer, DS3154 quad LIU, transformers, termination resistors, network connectors, and motherboard connectors. The DK101/DK2000 motherboard and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate loss-of-signal, out-of-frame, and interrupt status. An on-board FPGA contains mux logic to connect framer ports to one another or to the DK2000 in a variety of configurations.

Each DS3144DK is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

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DEMO KIT CONTENTS

DS3144DK Demo Kit Daughter Card
DK101 Demo Kit Motherboard

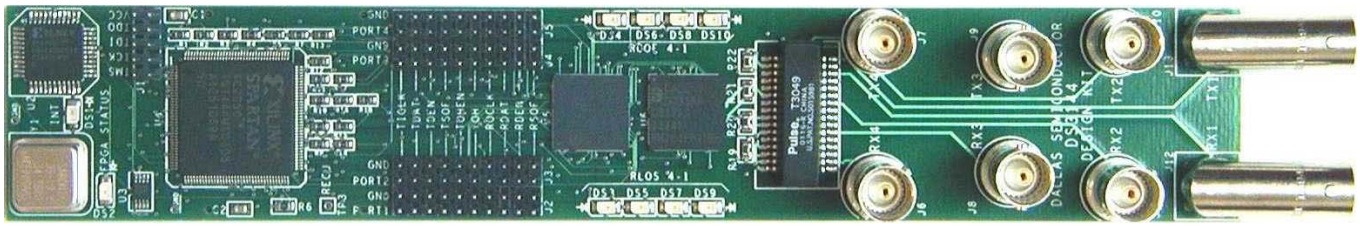
Download from www.maxim-ic.com/DS3144DK:
- DS3144DK Data Sheet
- DS3144DK Support Files
- ChipView Software

FEATURES

- Demonstrates Key Functions of DS3144 Quad DS3/E3 Framer
- Includes DS3154 Quad LIU, Transformers, BNC Connectors, and Termination Passives for Communication with Test Equipment over Coax
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and ChipView Software Provide Point-and-Click Access to the DS3144 Register Set
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- Memory-Mapped FPGA Provides Flexible Clock/Data/Sync Connections Among Framer Ports and DK2000 Motherboard
- LEDs for Out-of-Frame, Loss-of-Signal, and Interrupt
- Easy-to-Read Silk Screen Labels Identify the Signals Associated with all Connectors, Jumpers, and LEDs

ORDERING INFORMATION

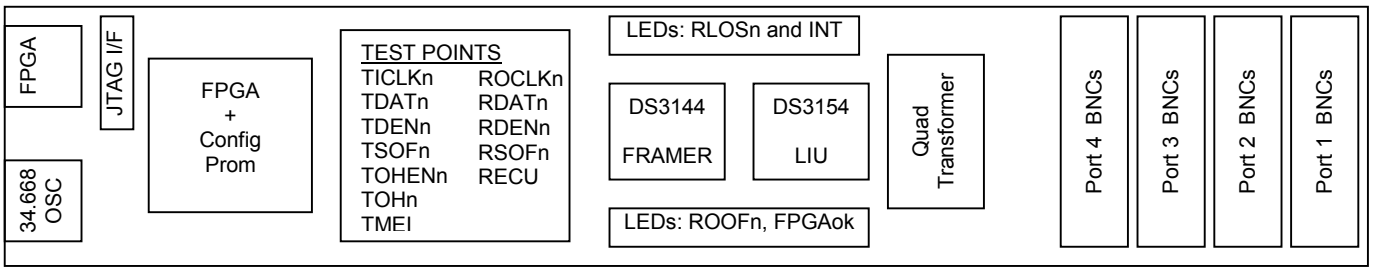
PART	DESCRIPTION
DS3144DK	DS3144 Demo Kit Daughter Card (with included DK101 motherboard)



COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C2, C15	3	0.1µF 10%, 16V ceramic capacitors (0805)	Panasonic	ECJ-2VB1C104K
C3–C9, C11–C14, C16, C20, C22, C23, C25–C32	23	0.1µF 10%, 16V ceramic capacitors (0603)	Phycomp	06032R104K7B20D
C10, C17, C18, C24	4	1µF 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C19, C21	2	10µF 20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
DS1, DS3–DS10	9	LED, red, SMD	Panasonic	LN1251C
DS2	1	LED, green, SMD	Panasonic	LN1351C
J1	1	10-pin connector, dual-row vertical	Digi-Key	S2012-05-ND
J2–J5	4	20-pin headers, dual-row vertical	Samtec	HDR-TSW-110-14-T-D
J6–J11	6	5-pin BNC connectors, right-angle vertical	Cambridge	CP-BNCPC-004
J12, J13	2	5-pin BNC connectors, right-angle	Kruvand	UCBJR220
J14, J15	2	50-pin connectors, dual-row vertical	Samtec	TFM-125-02-S-D-LC
R1–R5, R7–R18, R23, R28–R59	49	30Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ300V
R6	1	470Ω 5%, 1/10W resistor (0805)	Panasonic	ERJ-6GEYJ471V
R19–R22, R69–R72	8	332Ω 1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF3320V
R24	1	10kΩ 5%, 1/10W resistor (0805)	Panasonic	ERJ-6GEYJ103V
R25, R26	2	330Ω 5% 1/10W MF resistors (0805)	Panasonic	ERA-6YEB331V
R27	1	Not populated	—	—
R60	1	10kΩ 5%, 1/10W resistor (0805)	Panasonic	ERJ-6ENF1002V
R61–R68	8	100Ω 1/16W 5% resistors (0603)	Panasonic	ERJ-3GEYJ101V
T1	1	XFMR, XMIT/RCV, 1 to 2, SMT 32-pin	Pulse Engineering	T3049
U1	1	Serial configuration EEPROM for Xilinx, 65kB 8-pin DIP. Socketed (not populated)	Atmel	AT17LV65EUA and 61499-30831007000-ND
U2	1	1M PROM for FPGA 44-pin TQFP (not populated)	Xilinx	XC18V01VQ44C_U
U3	1	8-Pin µMAX V_{OUT} = 2.5V or Adj	Maxim	MAX1792EUA25
U4	1	Xilinx Spartan 2.5V FPGA, 20mm X 20mm 144-pin TQFP	Xilinx	XC2S50-5TQ144C
U5	1	Quad DS3/E3 framer 144-pin BGA, 0°C to +70°C	Dallas Semiconductor	DS3144
U6	1	Quad DS3/E3/STS-1 LIU 144-pin BGA	Dallas Semiconductor	DS3154
Y1	1	3.3V, 34.368MHz crystal clock oscillator	SaRonix	NTH089AA3-34.368

BOARD FLOORPLAN



LINE-SIDE CONNECTIONS

The DS3144DK implements the transmit (Tx) and receive (Rx) line interface networks recommended in the DS3154 data sheet. The BNC connectors are labeled TX1 through TX4 and RX1 through RX4. Note that the purpose of the DS3144DK is to evaluate the DS3144 framer, not the DS3154 LIU. The DS3144DK is not an impedance-matched board and therefore has not been designed to have transmit waveforms with optimal template fit. To evaluate the analog performance of the DS3154, request a DS3154DK demo kit.

INTERFACE CONNECTORS

Two 50-pin connectors (J14, J15) on the bottom of the DS3144DK daughter card provide the processor interface, DS3 clock, and power supply from the DK101 or DK2000 motherboards. These connectors also provide a bidirectional clock/data/sync connection with the DK2000.

CONNECTION TO A COMPUTER

Refer to the DK101 data sheet or the DK2000 data sheet for information. After power is applied, if the DS3144DK is working correctly, the FPGA status LED (green) is lit, the INT LED (red) on the DS3144DK is not lit, and the RLOS and ROOF LEDs (red) may or may not be lit.

QUICK SETUP (REGISTER VIEW)

1) Connect the DS3144DK daughter card to the DK101 motherboard or the DK2000 motherboard.
2) Connect the motherboard to a PC and a power supply as described in the motherboard data sheet.
3) Install and run the ChipView software, as described in the motherboard data sheet.
4) ChipView offers a choice between Register View, Demo, and Terminal Mode. Select Register View.
5) In the Definition File Assignment window, select the file DS3144DC_FPGA.def. This definition file will, in turn, load DS3154DC.def, DS3144_1_DC.def, DS3144_2_DC.def, DS3144_3_DC.def, and DS3144_4_DC.def.
6) Next the Register View Screen appears, showing the register names, acronyms, and values for the DS3144, DS3154, and the FPGA. Select among the register views using the pulldown menu box on the right.

Several register initialization (.INI) files are available for the DS3144DK. Initialization files are loaded by selecting the menu option File→Register .INI File→Load .INI File.

7) Load the .INI file DS3144_1_txPRBS215-1_Cbit.ini.
8) Switch to the DS3154 register view (DS3154DC.def) and set TCR1 = 0 and RCR1 = 0 on the DS3154 (this clears the transmit tri-state and receive tri-state bits that are set on power-up in the DS3154).
9) Loopback port 1 by either (a) connecting a length of coax cable between the TX1 BNC and the RX1 BNC, or (b) setting the GCR1:LLB (local loopback) bit in the DS3154.
10) Switch to the DS3144 port 1 register view (DS3144_1_DC.def). Toggle BCR1:TC high then low to begin transmitting a 2^{15} - 1 PRBS pattern. Toggle BCR1:RESYNC high then low to resynchronize the BERT receiver.
11) At this point the following may be observed:
    - Port 1 RLOS and ROOF LEDs are not lit, meaning the port 1 framer has acquired frame sync. This can also be observed in the port 1 T3E3SR status register.
    - The port 1 BSR:SYNC bit is set, indicating the BERT receiver is receiving the 2^{15} - 1 PRBS pattern.

This is a very basic setup designed to build familiarity with the DS3144DK. Many other configurations are possible. Consult the DS3144 data sheet and the remainder of this data sheet for further information.

MEMORY MAP

DK101 daughter card address space begins at 0x81000000.

DK2000 daughter card address space begins at:
- 0x30000000 for slot 0
- 0x40000000 for slot 1
- 0x50000000 for slot 2
- 0x60000000 for slot 3

All offsets in Table 1 below are relative to the beginning of the daughter card address space.

Table 1. Daughter Card Address Map

DS3/E3 PORT NUMBER	DS3144 OFFSET	DS3154 OFFSET	FPGA OFFSET
1	0x1300 to 0x13FF	0x2030 to 0x203F	0x0010 to 0x001F
2	0x1000 to 0x10FF	0x2010 to 0x201F	0x0020 to 0x002F
3	0x1100 to 0x11FF	0x2020 to 0x202F	0x0030 to 0x003F
4	0x1200 to 0x12FF	0x2000 to 0x200F	0x0040 to 0x004F

All offsets in Table 2 below are relative to the daughter card address space *plus* the DS3/E3 port offset in Table 1.

Table 2. DS3144DK FPGA Register Map

OFFSET	REGISTER	TYPE	DESCRIPTION
0x0000	BID	Read-Only	Board ID
0x0002	XBIDH	Read-Only	High Nibble Extended Board ID
0x0003	XBIDM	Read-Only	Middle Nibble Extended Board ID
0x0004	XBIDL	Read-Only	Low Nibble Extended Board ID
0x0005	BREV	Read-Only	Board Fab Revision
0x0006	AREV	Read-Only	Board Assembly Revision
0x0007	PREV	Read-Only	PLD Revision
0x000A	PCTC_SR	Control	PCM_TXCLK Source
0x000B	PCTS_SR	Control	PCM_TSYNC Source
0x000C	PCRX_SR	Control	PCM_RXD Source
0x000D	PCRC_SR	Control	PCM_RXCLK Source
0x000E	PCRS_SR	Control	PCM_RSYNC Source
0x0010	TDAT_SR	Control	DS3144 TDAT Source
0x0020			
0x0030			
0x0040			
0x0011	TICK_SR	Control	DS3144 TICLK Source
0x0021			
0x0031			
0x0041			
0x0012	TSOF_SR	Control	DS3144 TSOF Source
0x0022			
0x0032			
0x0042			

Registers in the FPGA can be easily modified using the ChipView software and the definition file named DS3144DC_FPGA.def. Registers 0x00 through 0x07 (excluding register 0x01, which has no function on the DS3144DK) are read-only and are programmed at the factory to document board identification and revision information. The remaining registers in the FPGA control the connection of the DS3144's equipment-side framer pins. With these control registers, the framers within the DS3144 can be looped back on themselves externally, connected to each other back-to-back, or connected to the DK2000 motherboard.

In Table 2 and the control register descriptions below, PCM_TXCLK, PCM_TXD, and PCM_TSYNC are clock/data/sync lines over which the DS3144 can transmit a DS3/E3 data stream to the DK2000 motherboard or other daughter cards plugged into the DK2000. PCM_RXCLK, PCM_RXD, and PCM_RSYNC are clock/data/sync lines over which the DS3144DK can receive a DS3/E3 data stream from the DK2000 or a daughter card plugged into the DK2000. See the DS3144DK schematics for additional details.

Note that the DS3/E3 port numbers of the DS3144DK (as silk-screened on the board) do not match the DS3144 port numbers and the DS3154 port numbers. Table 3 details the mapping of device port numbers to board port numbers. This mapping is reflected in the address ranges shown in Table 1.

Table 3. Relationship of Silk-Screened Port Numbers to IC Ports Numbers

SILK-SCREENED PORT NUMBER ON BNCs AND RLOS/ROOF LEDs	DS3144 PORT	DS3154 PORT
1	4	4
2	1	2
3	2	3
4	3	1

From this it can be seen that, for example, the BNCs and LEDs for DS3144DK port 4 are associated with port 3 of the DS3144 and port 1 of the DS3154.

CONTROL REGISTERS

Register Name: **PCTC_SR**
Register Description: **PCM_TXCLK Source**
Register Address Offset: **0x0A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	PCS2	PCS1	PCS0
Default	—	—	—	—	—	0	0	0

Bits 2 to 0: PCM_TXCLK Source (PCS[2:0])
000 = Tri-state PCM_TXCLK
001 = Drive PCM_TXCLK with TDEN/TGCLK1
010 = Drive PCM_TXCLK with TDEN/TGCLK2
011 = Drive PCM_TXCLK with TDEN/TGCLK3
100 = Drive PCM_TXCLK with TDEN/TGCLK4

Register Name: **PCTS_SR**
Register Description: **PCM_TSYNC Source**
Register Address Offset: **0x0B**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	PSS2	PSS1	PSS0
Default	—	—	—	—	—	0	0	0

Bits 2 to 0: PCM_TSYNC Source (PSS[2:0])
000 = Tri-state PCM_TSYNC
001 = Drive PCM_TSYNC with TSOF1
010 = Drive PCM_TSYNC with TSOF2
011 = Drive PCM_TSYNC with TSOF3
100 = Drive PCM_TSYNC with TSOF4

Note: Only use non-zero settings of PSS[2:0] when the TSOFx pin is configured as an output by setting MC3:TSOFC = 1 in the corresponding DS3144 framer.

Register Name: **PCRX_SR**
Register Description: **PCM_RXD Source**
Register Address Offset: **0x0C**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	PRXS2	PRXS1	PRXS0
Default	—	—	—	—	—	0	0	0

Bits 2 to 0: PCM_RXD Source (PRXS[2:0])
000 = Tri-state PCM_RXD
001 = Drive PCM_RXD with RDAT1
010 = Drive PCM_RXD with RDAT2
011 = Drive PCM_RXD with RDAT3
100 = Drive PCM_RXD with RDAT4

Register Name: **PCRC_SR**
Register Description: **PCM_RXCLK Source**
Register Address Offset: **0x0D**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	PRCS2	PRCS1	PRCS0
Default	—	—	—	—	—	0	0	0

Bits 2 to 0: PCM_RXCLK Source (PRCS[2:0])
000 = Tri-state PCM_RXCLK
001 = Drive PCM_RXCLK with RDEN/RGCLK1
010 = Drive PCM_RXCLK with RDEN/RGCLK2
011 = Drive PCM_RXCLK with RDEN/RGCLK3
100 = Drive PCM_RXCLK with RDEN/RGCLK4

Register Name: **PCRS_SR**
Register Description: **PCM_RSYNC Source**
Register Address Offset: **0x0E**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	PRSS2	PRSS1	PRSS0
Default	—	—	—	—	—	0	0	0

Bits 2 to 0: PCM RSYNC Source (PRSS[2:0])
000 = Tri-state PCM_RSYNC
001 = Drive PCM_RSYNC with RSOF1
010 = Drive PCM_RSYNC with RSOF2
011 = Drive PCM_RSYNC with RSOF3
100 = Drive PCM_RSYNC with RSOF4

Register Name: **TDAT_SR**
Register Description: **DS3144 TDATx Source**
Register Address Offset: **0x10, 0x20, 0x30, 0x40**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	TDS2	TDS1	TDS0
Default	—	—	—	—	—	See note	See note	See note

Bits 2 to 0: TDATx Source (TDS[2:0])
000 = Tri-state TDATx
001 = Drive TDATx with RDAT1
010 = Drive TDATx with RDAT2
011 = Drive TDATx with RDAT3
100 = Drive TDATx with RDAT4
101 = Drive TDATx with PCM_TXD

Note: Initial values are such that TDAT1←RDAT1, TDAT2←RDAT2, TDAT3←RDAT3, TDAT4←RDAT4, which corresponds to address 0x10 = 001, address 0x20 = 010, address 0x30 = 011, and address 0x40 = 100.

Register Name: **TICK_SR**
Register Description: **DS3144 TICLKx Source**
Register Address Offset: **0x11, 0x21, 0x31, 0x41**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	TCS2	TCS1	TCS0
Default	—	—	—	—	—	1	0	1

Bits 2 to 0: TICLKx Source (TCS[2:0])
000 = Tri-state TICLKx
001 = Drive TICLKx with ROCLK1
010 = Drive TICLKx with ROCLK2
011 = Drive TICLKx with ROCLK3
100 = Drive TICLKx with ROCLK4
101 = Drive TICLKx with DS3_CLK
110 = Drive TICLKx with E3_CLK

Register Name: **TSOF_SR**
Register Description: **DS3144 TSOFx Source**
Register Address Offset: **0x12, 0x22, 0x32, 0x42**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	TSS2	TSS1	TSS0
Default	—	—	—	—	—	0	0	0

Bits 2 to 0: TICLKx Source (TSS[2:0])
000 = Tri-state TSOFx
001 = Drive TSOFx with RSOF1
010 = Drive TSOFx with RSOF2
011 = Drive TSOFx with RSOF3
100 = Drive TSOFx with RSOF4

Note: Only use non-zero settings of TSS[2:0] when the TSOFx pin is configured as an input by setting MC3:TSOFC = 0 in the corresponding DS3144 framer.

FPGA CONTROL EXAMPLES

The control registers in the DS3144DK's FPGA support a number of different connection scenarios. Figure 1 shows three example scenarios, and Table 4 lists the FPGA control registers settings required to implement them.

Figure 1. Example Connection Scenarios

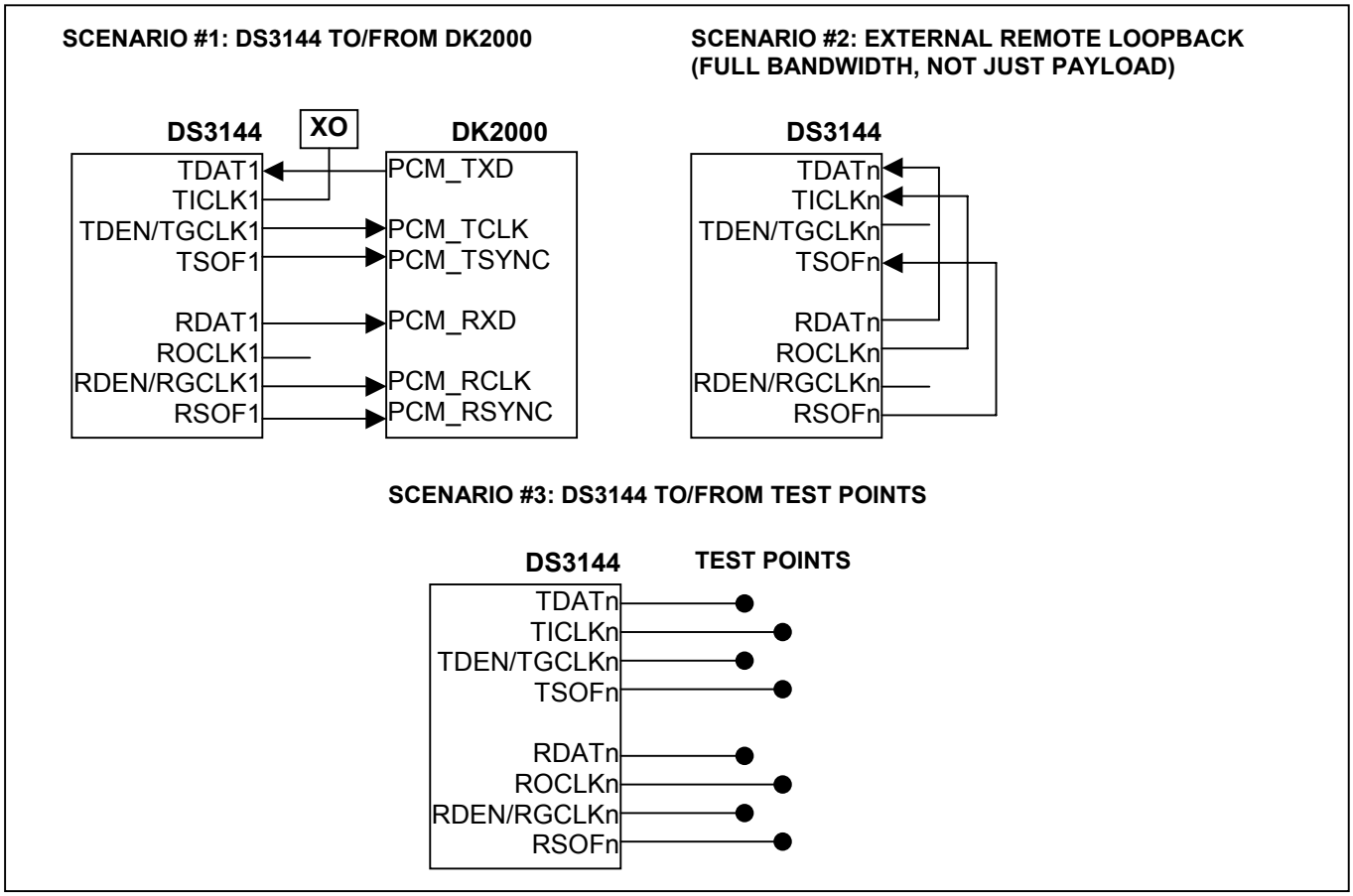


Table 4. Register Settings for Sample Configurations

OFFSET(S)	REGISTER	SCENARIO #1 (PORT 1 ONLY)	SCENARIO #2 (ALL PORTS)	SCENARIO #3 (ALL PORTS)
0x000A	PCTC_SR	001	N/A	N/A
0x000B	PCTS_SR	001	N/A	N/A
0x000C	PCRX_SR	001	N/A	N/A
0x000D	PCRC_SR	001	N/A	N/A
0x000E	PCRS_SR	001	N/A	N/A
0x0010	TDAT_SR	101	001	000
0x0020		N/A	010	000
0x0030		N/A	011	000
0x0040		N/A	100	000
0x0011	TICK_SR	101	001	000
0x0021		N/A	010	000
0x0031		N/A	011	000
0x0041		N/A	100	000
0x0012	TSOF_SR	000	001	000
0x0022		N/A	010	000
0x0032		N/A	011	000
0x0042		N/A	100	000

DS3144 INFORMATION

For more information about the DS3144 quad DS3/E3 framer, please consult the DS3144 data sheet, available on our website at www.maxim-ic.com/DS3144.

DS3154 INFORMATION

For more information about the DS3154 quad DS3/E3/STS-1 LIU, please consult the DS3154 data sheet, available on our website at www.maxim-ic.com/DS3154.

DS3144DK INFORMATION

For more information about the DS3144DK—including the ChipView software, the latest support files (.DEF, .INI, etc.), and the latest data sheet—please visit our website at www.maxim-ic.com/DS3144DK.

DK101/DK2000 INFORMATION

For more information about the DK101 or DK2000, please consult their respective data sheets, available on our website at www.maxim-ic.com/DK101 or www.maxim-ic.com/DK2000.

TECHNICAL SUPPORT

For additional technical support, please email your questions to telecom.support@dalsemi.com.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

DS3144 DESIGN KIT

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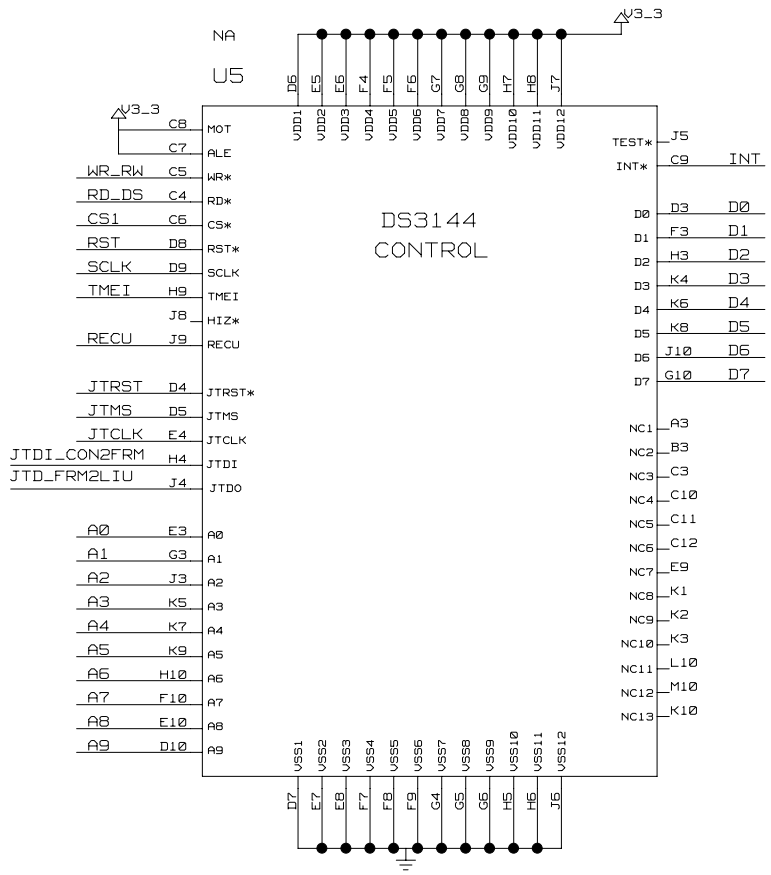

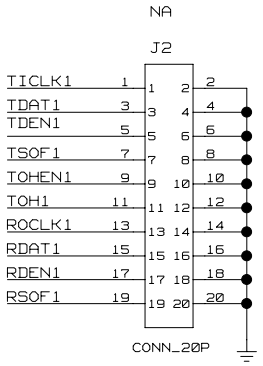

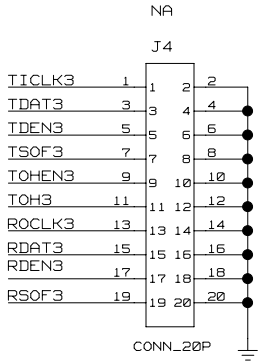

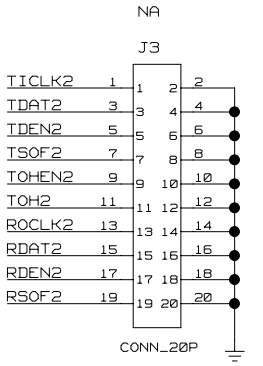

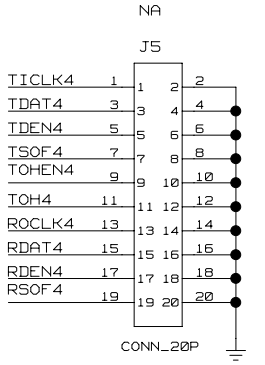

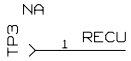

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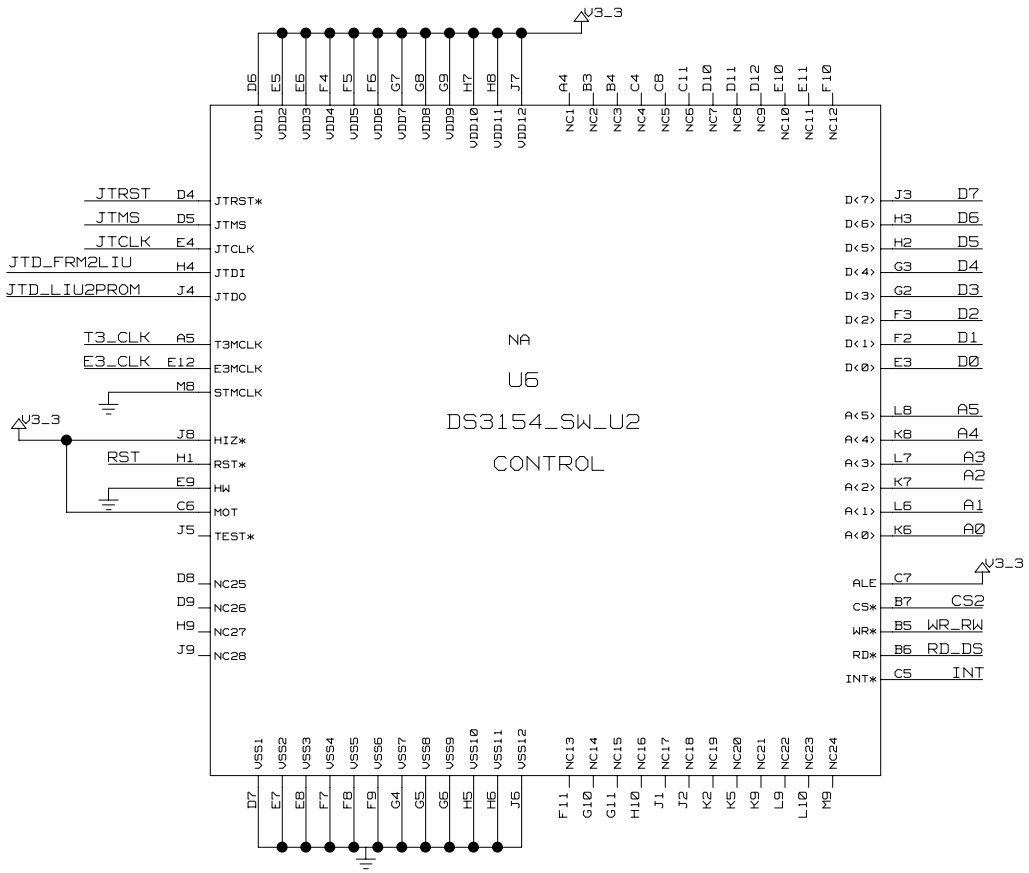

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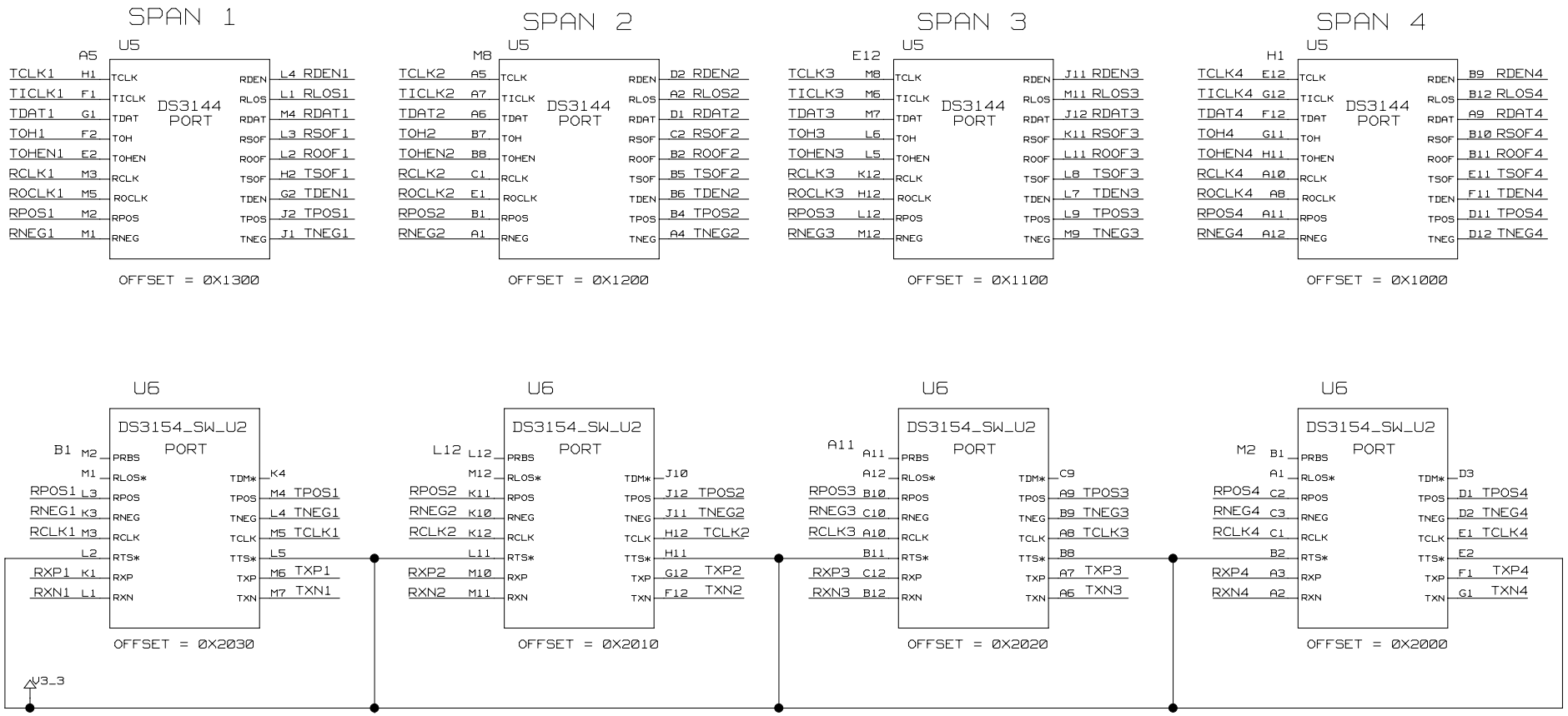

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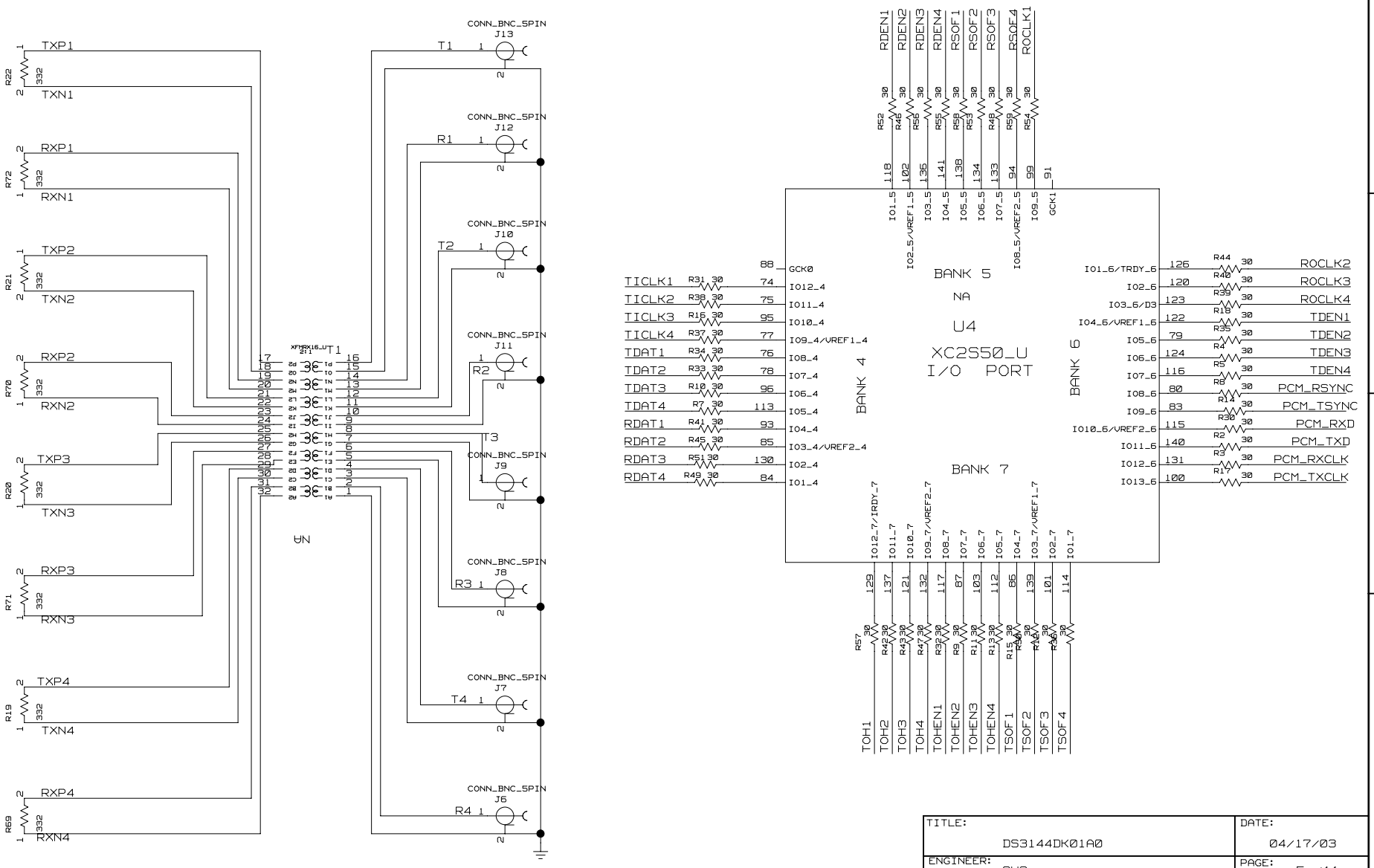
CONN_BNC_5PIN
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J12
J10
J11
J9
J8
J7
J6
T1
T2
T3
T4
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R3
R4
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IO3_5
IO4_5
IO5_5
IO6_5
IO7_5
IO8_5/VREF2_5
IO9_5
GCK1
BANK 5
NA
U4
XC2S50_U
I/O PORT
BANK 4
BANK 6
BANK 7
GCK0
IO12_4
IO11_4
IO10_4
IO9_4/VREF1_4
IO8_4
IO7_4
IO6_4
IO5_4
IO4_4
IO3_4/VREF2_4
IO2_4
IO1_4
TICLK1
TICLK2
TICLK3
TICLK4
TDAT1
TDAT2
TDAT3
TDAT4
RDAT1
RDAT2
RDAT3
RDAT4
IO1_6/TRDY_6
IO2_6
IO3_6/D3
IO4_6/VREF1_6
IO5_6
IO6_6
IO7_6
IO8_6
IO9_6
IO10_6/VREF2_6
IO11_6
IO12_6
IO13_6
ROCLK2
ROCLK3
ROCLK4
TDEN1
TDEN2
TDEN3
TDEN4
PCM_RSYNC
PCM_TSYNC
PCM_RXD
PCM_TXD
PCM_RXCLK
PCM_TXCLK
IO12_7/IRDY_7
IO11_7
IO10_7
IO9_7/VREF2_7
IO8_7
IO7_7
IO6_7
IO5_7
IO4_7
IO3_7/VREF1_7
IO2_7
IO1_7
TOH1
TOH2
TOH3
TOH4
TOHEN1
TOHEN2
TOHEN3
TOHEN4
TSOF1
TSOF2
TSOF3
TSOF4
TITLE:
DS3144DK01A0
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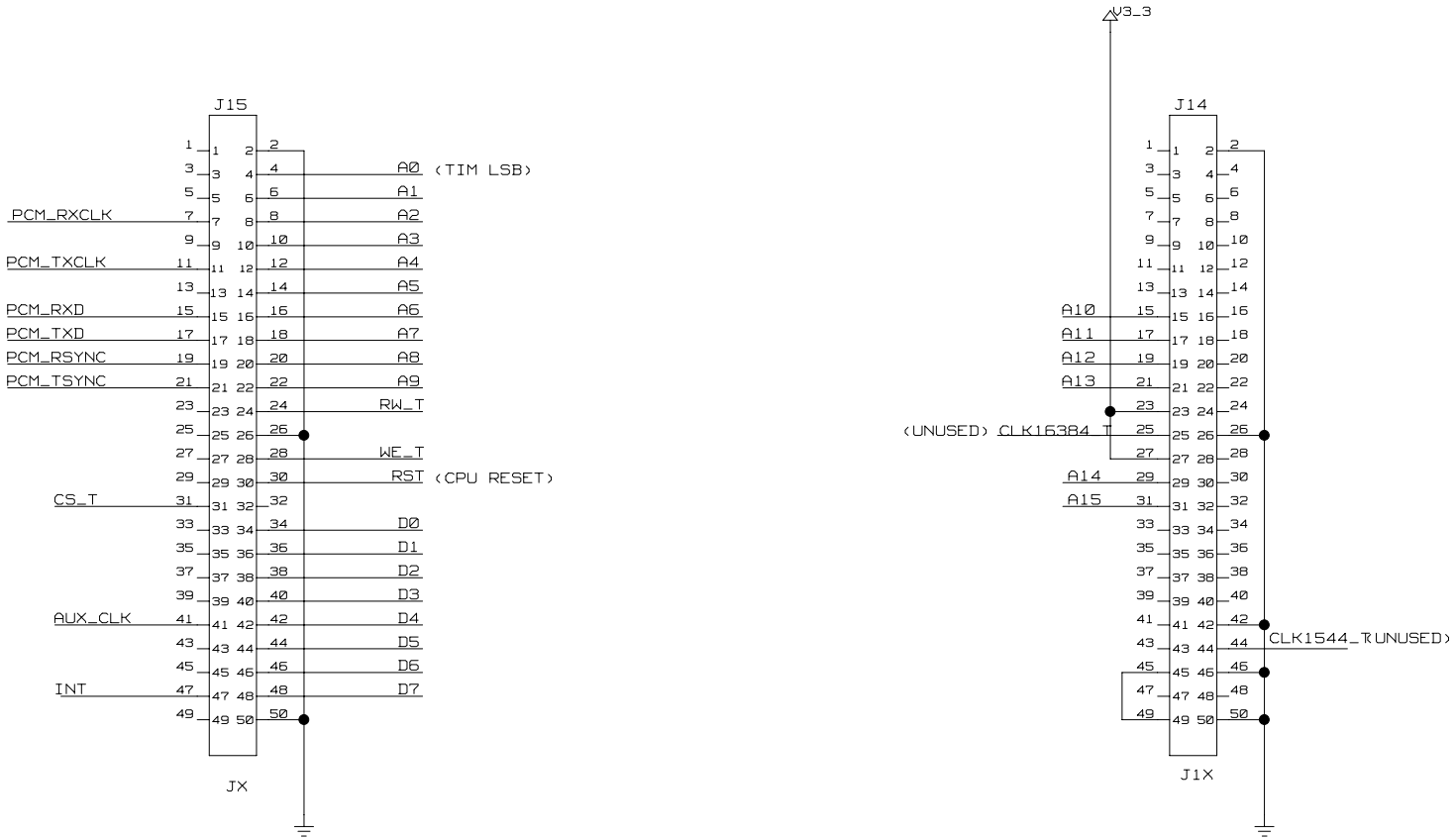

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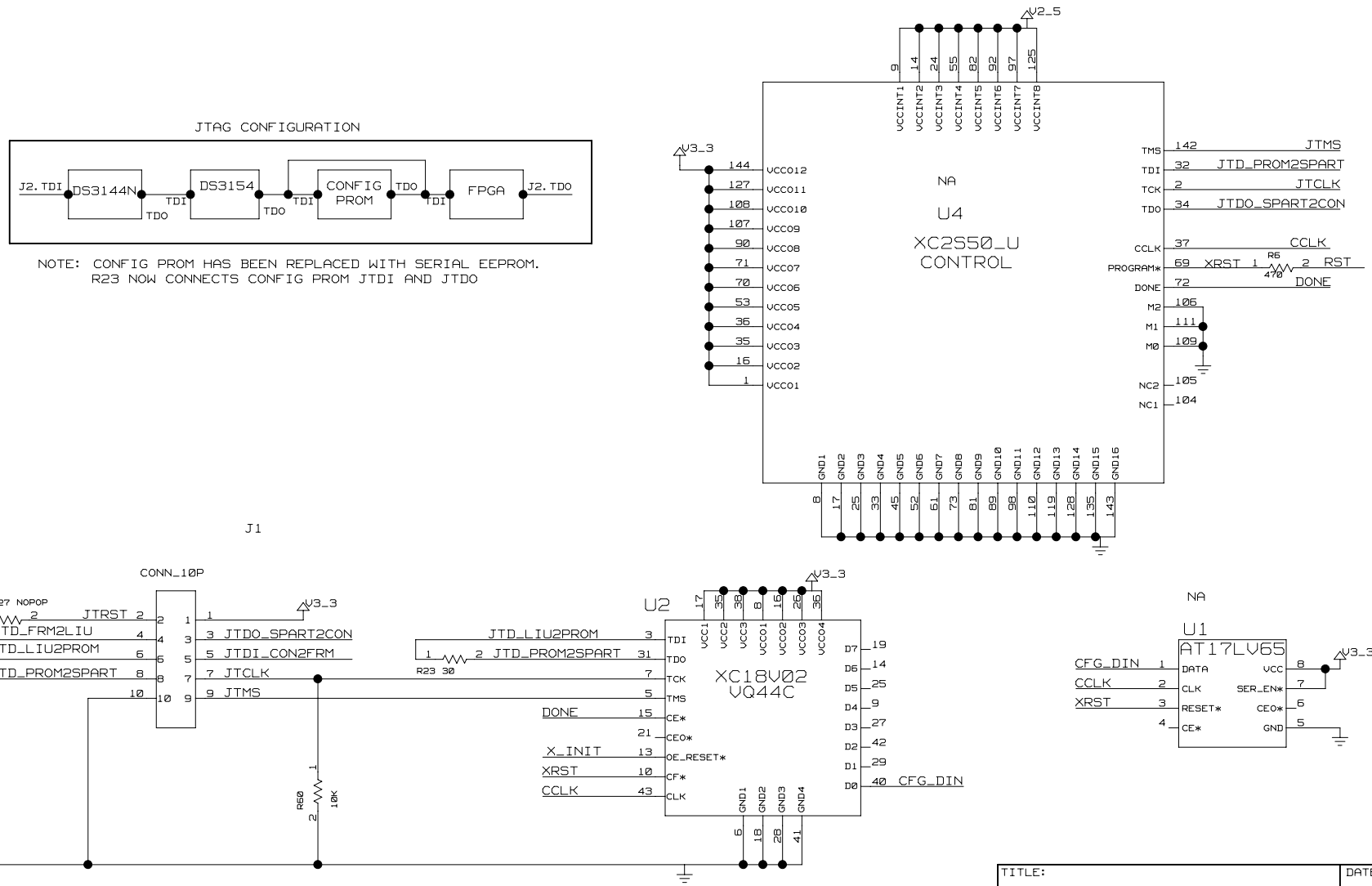

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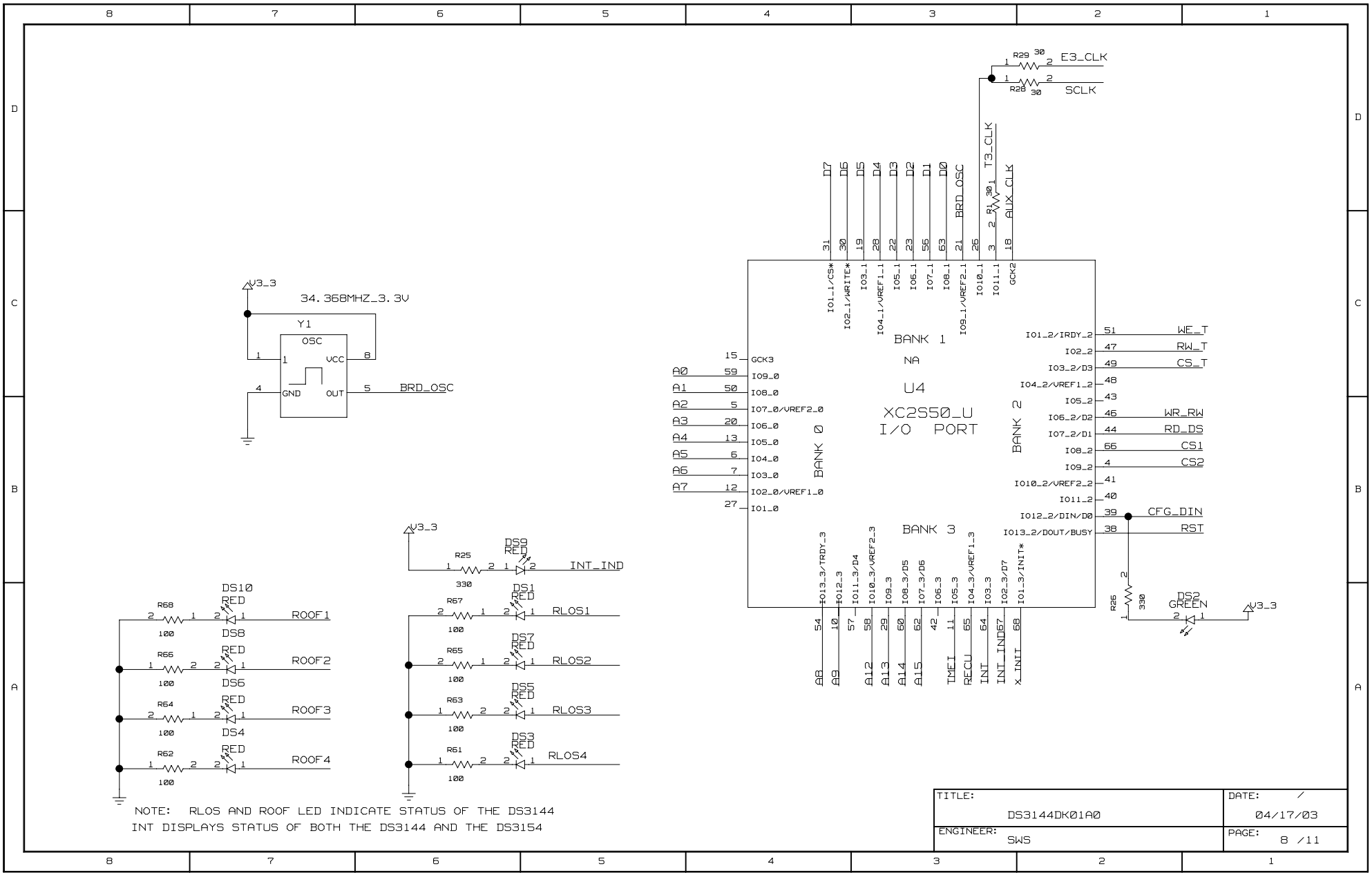

NOTE: RLOS AND ROOF LED INDICATE STATUS OF THE DS3144
INT DISPLAYS STATUS OF BOTH THE DS3144 AND THE DS3154

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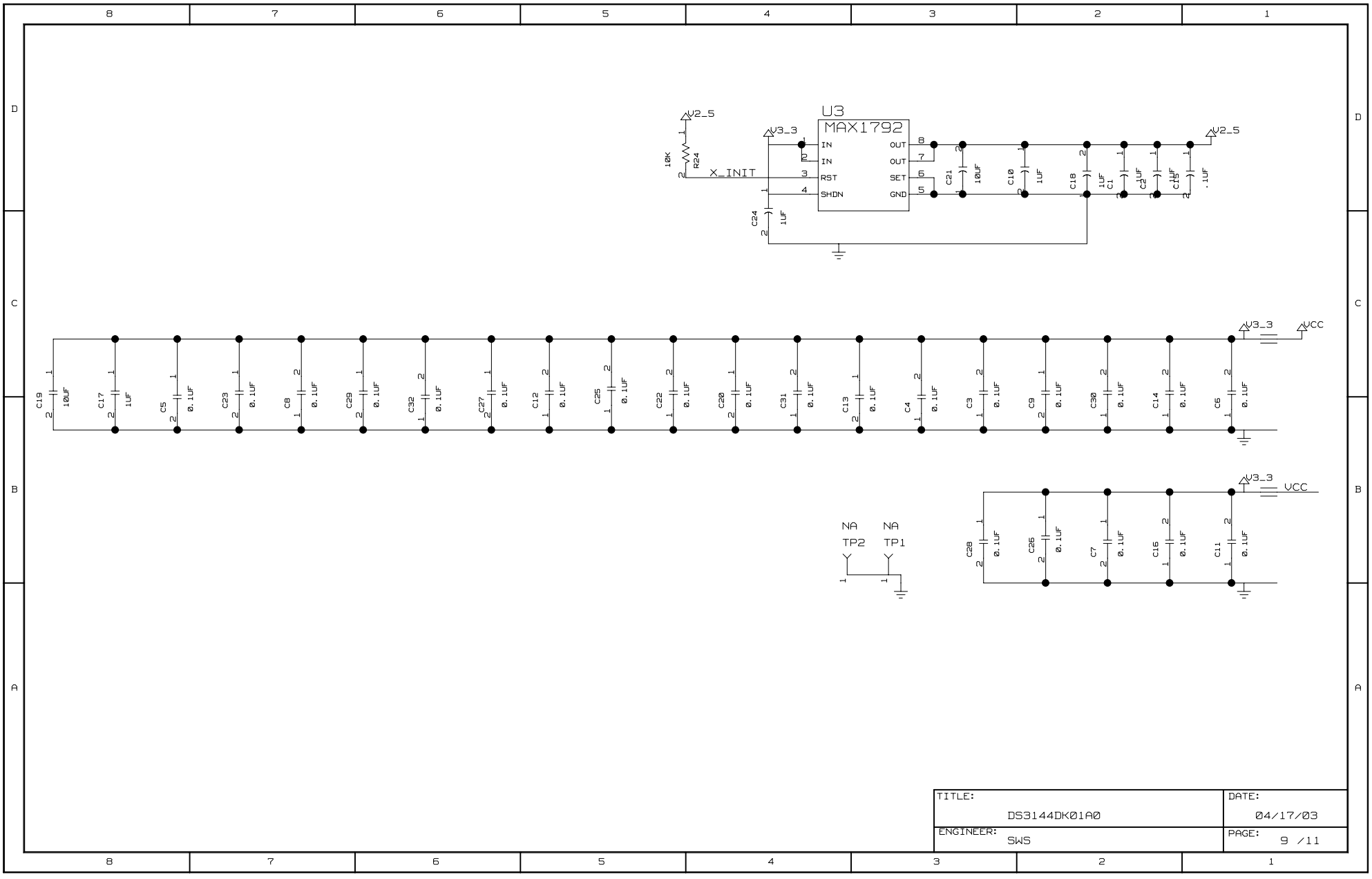

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*** Signal Cross-Reference for the entire design ***

A0	6D6<> 8C5<> 2B8< 3B4<
A1	6C6<> 8C5<> 2B8< 3B4<
A2	6C6<> 8B5<> 2B8< 3B4<
A3	6C6<> 8B5<> 2B8< 3B4<
A4	6C6<> 8B5<> 2B8< 3B4<
A5	6C6<> 8B5<> 2B8< 3B4<
A6	6C6<> 8B5<> 2A8<
A7	6C6<> 8B5<> 2A8<
A8	6C6<> 8A4<> 2A8<
A9	6C6<> 8A4<> 2A8<
A10	6C3<>
A11	6C3<>
A12	6C3<> 8A3<>
A13	6C3<> 8A3<>
A14	6B3<> 8A3<>
A15	6B3<> 8A3<>
AUX_CLK	6B8<> 8D3<
BRD_OSC	8C6> 8D3<>
CCLK	7A3< 7A5< 7C1<
CFG_DIN	7A3> 7A3<> 8B1<>
CLK1544_T	6B2<>
CLK16384_T	6C4<>
CS1	8B1<> 2C8<
CS2	8B1<> 3B4<
CS_T	6B8<> 8C1<>
D0	2C5<> 3C4<> 6B6<> 8D3<>
D1	2C5<> 3C4<> 6B6<> 8D3<>
D2	2C5<> 3C4<> 6B6<> 8D3<>
D3	2C5<> 3C4<> 6B6<> 8D3<>
D4	2C5<> 3C4<> 6B6<> 8D3<>
D5	2C5<> 3C4<> 6B6<> 8D3<>
D6	2C5<> 3C4<> 6B6<> 8D4<>
D7	2C5<> 3C4<> 6B6<> 8D4<>
DONE	7A5< 7C1<
E3_CLK	3C8< 8D2<
INT	2C5<> 3A4> 6B8<> 8A3<>
INT_IND	8A3<> 8B5<>
JTCLK	7A7<> 2B8< 3C8< 7C1<
JTDI_CON2FRM	7A6<> 2B8<
JTDO_SPART2CON	7A6<> 7C1>
JTD_FRM2LIU	2B8<> 7A8<> 3C8<
JTD_LIU2PROM	3C8> 7A8<> 7A6<
JTD_PROM2SPART	7A6<> 7A8<> 7D1<
JTMS	7A7<> 2B8< 3C8< 7D1<
JTRST	7B8<> 2B8< 3C8<
PCM_RSYNC	6C8<> 5B1<
PCM_RXCLK	6C8<> 5B1<
PCM_RXD	6C8<> 5B1<
PCM_TSYNC	6C8<> 5B1<
PCM_TXCLK	6C8<> 5B1<
PCM_TXD	6C8<> 5B1<
R1	5D6<>
R2	5C6<>
R3	5B6<>
R4	5A6<>
RCLK1	4B8<> 4C8<
RCLK2	4B6<> 4C6<
RCLK3	4B4<> 4C5<
RCLK4	4B2<> 4C2<
RDAT1	2C4<> 4D7> 5B5<
RDAT2	2B4<> 4D5> 5B5<
RDAT3	2C2<> 4D3> 5B5<
RDAT4	2A2<> 4D1> 5B5<
RDEN1	2C4<> 4D7> 5D3<
RDEN2	2A4<> 4D5> 5D3<
RDEN3	2C2<> 4D3> 5D3<
RDEN4	2A2<> 4D1> 5D3<
RD_DS	8B1<> 2C8< 3B4<
RECU	2A2<> 8A3<> 2C8<
RLOS1	4D7> 8A5<>
RLOS2	4D5> 8A5<>
RLOS3	4D3> 8A5<>
RLOS4	4D1> 8A5<>
RNEG1	4B8<> 4C8<
RNEG2	4B6<> 4C6<
RNEG3	4B4<> 4C5<
RNEG4	4B2<> 4C2<
ROCLK1	2C4<> 4C8> 5D2<
ROCLK2	2B4<> 4C6> 5C1<
ROCLK3	2C2<> 4C5> 5C1<
ROCLK4	2B2<> 4C2> 5C1<
ROOF1	4C7> 8A7<>
ROOF2	4C5> 8A7<>
ROOF3	4C3> 8A7<>
ROOF4	4C1> 8A7<>
RPOS1	4B8<> 4C8<
RPOS2	4B6<> 4C6<
RPOS3	4B4<> 4C5<
RPOS4	4B2<> 4C2<
RSOF1	2C4<> 4D7> 5D3<
RSOF2	2A4<> 4D5> 5D3<
RSOF3	2C2<> 4D3> 5D3<
RSOF4	2A2<> 4D1> 5D2<
RST	6B6<> 8B1<> 2C8< 3B8< 7C1<
RW_T	6C6<> 8C1<>
RXN1	4B8< 5C8<
RXN2	4B6< 5B8<
RXN3	4B4< 5A8<
RXN4	4B2< 5A8<
RXP1	4B8< 5D8<
RXP2	4B6< 5C8<
RXP3	4B4< 5B8<
RXP4	4B2< 5A8<
SCLK	2C8< 8D2<
T1	5D6<>
T2	5C6<>
T3	5B6<>
T3_CLK	3C8< 8D3<
T4	5A6<>
TCLK1	4D8> 4B7<
TCLK2	4D6> 4B5<
TCLK3	4D5> 4B3<
TCLK4	4D2> 4B1<
TDAT1	2D4<> 4D8< 5C5<
TDAT2	2B4<> 4D6< 5C5<
TDAT3	2D2<> 4D5< 5B5<
TDAT4	2B2<> 4D2< 5B5<
TDEN1	2D4<> 4C7> 5C1<
TDEN2	2B4<> 4C5> 5C1<
TDEN3	2D2<> 4C3> 5C1<
TDEN4	2B2<> 4C1> 5C1<
TICLK1	2D4<> 4D8< 5C5<
TICLK2	2B4<> 4D6< 5C5<
TICLK3	2D2<> 4D5< 5C5<
TICLK4	2B2<> 4D2< 5C5<
TMEI	8A3<> 2C8<
TNEG1	4C7> 4B7<
TNEG2	4C5> 4B5<
TNEG3	4C3> 4B3<
TNEG4	4C1> 4B1<
TOH1	2C4<> 4D8< 5A3<
TOH2	2B4<> 4D6< 5A3<
TOH3	2C2<> 4D5< 5A3<
TOH4	2B2<> 4D2< 5A3<
TOHEN1	2C4<> 4C8< 5A3<
TOHEN2	2B4<> 4C6< 5A3<
TOHEN3	2C2<> 4C5< 5A3<
TOHEN4	2B2<> 4C2< 5A3<
TPOS1	4C7> 4B7<
TPOS2	4C5> 4B5<
TPOS3	4C3> 4B3<
TPOS4	4C1> 4B1<
TSOF1	2D4<> 4C7<> 5A2<
TSOF2	2B4<> 4C5<> 5A2<
TSOF3	2C2<> 4C3<> 5A2<
TSOF4	2B2<> 4C1<> 5A2<
TXN1	4B7<> 5D8<
TXN2	4B5<> 5C8<
TXN3	4B3<> 5B8<
TXN4	4B1<> 5A8<
TXP1	4B7<> 5D8<
TXP2	4B5<> 5C8<
TXP3	4B3<> 5B8<
TXP4	4B1<> 5A8<
WE_T	6B6<> 8C1<>
WR_RW	8B1<> 2C8< 3B4<
XRST	7A3> 7A5> 7C2<
X_INIT	7A5<> 8A2<> 9D4<>

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*** Part Cross-Reference for the entire design ***

C1	CAP1	9D2
C2	CAP1	9D2
C3	CAP	9B3
C4	CAP	9B3
C5	CAP	9B8
C6	CAP	9B1
C7	CAP	9B2
C8	CAP	9B7
C9	CAP	9B2
C10	CAP	9D3
C11	CAP	9B1
C12	CAP	9B5
C13	CAP	9B4
C14	CAP	9B2
C15	CAP1	9D2
C16	CAP	9B2
C17	CAP	9B8
C18	CAP	9D2
C19	CAP	9B8
C20	CAP	9B4
C21	CAP	9D3
C22	CAP	9B5
C23	CAP	9B7
C24	CAP	9C4
C25	CAP	9B5
C26	CAP	9B2
C27	CAP	9B6
C28	CAP	9B3
C29	CAP	9B7
C30	CAP	9B2
C31	CAP	9B4
C32	CAP	9B6
DS1	LED	8B5
DS2	LED	8A2
DS3	LED	8A6
DS4	LED	8A7
DS5	LED	8A6
DS6	LED	8A7
DS7	LED	8A6
DS8	LED	8A7
DS9	LED	8B6
DS10	LED	8B7
J1	CONN_10P	7B7
J2	CONN_20P	2D3
J3	CONN_20P	2B3
J4	CONN_20P	2D2
J5	CONN_20P	2B2
J6	CONN_BNC_5PIN	5A5
J7	CONN_BNC_5PIN	5A5
J8	CONN_BNC_5PIN	5B5
J9	CONN_BNC_5PIN	5B5
J10	CONN_BNC_5PIN	5C5
J11	CONN_BNC_5PIN	5C5
J12	CONN_BNC_5PIN	5D5
J13	CONN_BNC_5PIN	5D5
J14	CONN_50P2	6D3
J15	CONN_50P2	6D7
R1	RES1	8C3
R2	RES1	5B1
R3	RES1	5B1
R4	RES1	5C1
R5	RES1	5C1
R6	RES	7C2
R7	RES1	5B4
R8	RES1	5C1
R9	RES1	5A3
R10	RES1	5C4
R11	RES1	5A3
R12	RES1	5A2
R13	RES1	5A3
R14	RES1	5B1
R15	RES1	5A3
R16	RES1	5C4
R17	RES1	5B1
R18	RES1	5C1
R19	RES1	5A8
R20	RES1	5B8
R21	RES1	5C8
R22	RES1	5D8
R23	RES1	7A6
R24	RES	9D4
R25	RES1	8B6
R26	RES1	8A2
R27	RES	7B8
R28	RES1	8D2
R29	RES1	8D3
R30	RES1	5B1
R31	RES1	5C4
R32	RES1	5A3
R33	RES1	5C4
R34	RES1	5C4
R35	RES1	5C1
R36	RES1	5A2
R37	RES1	5C4
R38	RES1	5C4
R39	RES1	5C1
R40	RES1	5C1
R41	RES1	5B4
R42	RES1	5A3
R43	RES1	5A3
R44	RES1	5C1
R45	RES1	5B4
R46	RES1	5D3
R47	RES1	5A3
R48	RES1	5D3
R49	RES1	5B4
R50	RES1	5A2
R51	RES1	5B4
R52	RES1	5D3
R53	RES1	5D3
R54	RES1	5D2
R55	RES1	5D3
R56	RES1	5D3
R57	RES1	5A3
R58	RES1	5D3
R59	RES1	5D3
R60	RES1	7A7
R61	RES1	8A6
R62	RES1	8A8
R63	RES1	8A6
R64	RES1	8A8
R65	RES1	8A6
R66	RES1	8A8
R67	RES1	8A6
R68	RES1	8A8
R69	RES1	5A8
R70	RES1	5B8
R71	RES1	5A8
R72	RES1	5C8
T1	XFMRX16_U	5C6
TP1	TESTPOINT	9B3
TP2	TESTPOINT	9B4
TP3	TESTPOINT	2A2
U1	AT17LV65	7A2
U2	XC18V02VQ44C_U	7B5
U3	MAX1792	9D4
U4	XC2S50_U	5C3 7C3 8C3
U5	DS3144	2D7 4D2 4D4 4D6 4D8
U6	DS3154_SW_U2	3C6 4B2 4B4 4B6 4B8
Y1	OSC2_U	8C7

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