



## HYM5V64404A Q-Series

SO DIMM 4Mx64 bit CMOS DRAM MODULE  
based on 4Mx16 DRAM, EDO, 3.3V, 4K/8K-Refresh

### DESCRIPTION

The HYM5V64404A Q-Series is a 4Mx64-bit EDO mode CMOS DRAM module consisting of four 4Mx16 TSOP and one 2048-bit EEPROM on a 144 pin glass-epoxy printed circuit board. 0.1μF and 0.01μF decoupling capacitors are mounted for each DRAM. The HYM5V64404AQ G-series is gold plated socket type Dual In-line Memory Module suitable for easy interchange and addition of 32M byte memory.

### FEATURES

- Max. Active Power Dissipation

| Speed | 8K    | 4K    |
|-------|-------|-------|
| 50    | 1.58W | 2.02W |
| 60    | 1.30W | 1.73W |

- Fast access time and cycle time

| Speed | tRAC | tCAC | tHPC |
|-------|------|------|------|
| 50    | 50ns | 13ns | 25ns |
| 60    | 60ns | 15ns | 30ns |

- 144-Pin SO DIMM
- Serial Presence Detect with EEPROM
- Extended Data Out Operation

- Single power supply of 3.3V ± 10%
- Read-Modify-Write Capability
- LVTTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- Refresh cycles

| Part No.             | Ref.            |
|----------------------|-----------------|
| HYM5V64404A Q-Series | 4K              |
| HYM5V64434A Q-Series | 8K <sup>£</sup> |

£ /CAS-before-/RAS refresh, Hidden refresh mode : 4K cycles / 64ms

### PIN DISCRIPTION

|             |                             |
|-------------|-----------------------------|
| /RAS0       | Row Address Strobe          |
| /CAS0-CAS7, | Column Address Strobe       |
| /WE         | Write Enable                |
| /OE         | Output Enable               |
| A0 -A12     | Address Input(8K Product)   |
| A0 -A11     | Address Input(4K Product)   |
| DQ0-DQ63    | Data Input / Output         |
| SCL         | Serial PD Clock Input       |
| SDA         | Serial PD Data Input/Output |
| VCC         | Power (+3.3V)               |
| VSS         | Ground                      |

**PIN NAME**

| #  | NAME  | #  | NAME  | #   | NAME  | #   | NAME  |
|----|-------|----|-------|-----|-------|-----|-------|
| 1  | Vss   | 2  | Vss   | 73  | /OE   | 74  | NC    |
| 3  | DQ0   | 4  | DQ32  | 75  | Vss   | 76  | Vss   |
| 5  | DQ1   | 6  | DQ33  | 77  | NC    | 78  | NC    |
| 7  | DQ2   | 8  | DQ34  | 79  | NC    | 80  | NC    |
| 9  | DQ3   | 10 | DQ35  | 81  | Vcc   | 82  | Vcc   |
| 11 | Vcc   | 12 | Vcc   | 83  | DQ16  | 84  | DQ48  |
| 13 | DQ4   | 14 | DQ36  | 85  | DQ17  | 86  | DQ49  |
| 15 | DQ5   | 16 | DQ37  | 87  | DQ18  | 88  | DQ50  |
| 17 | DQ6   | 18 | DQ38  | 89  | DQ19  | 90  | DQ51  |
| 19 | DQ7   | 20 | DQ39  | 91  | Vss   | 92  | Vss   |
| 21 | Vss   | 22 | Vss   | 93  | DQ20  | 94  | DQ52  |
| 23 | /CAS0 | 24 | /CAS4 | 95  | DQ21  | 96  | DQ53  |
| 25 | /CAS1 | 26 | /CAS5 | 97  | DQ22  | 98  | DQ54  |
| 27 | Vcc   | 28 | Vcc   | 99  | DQ23  | 100 | DQ55  |
| 29 | A0    | 30 | A3    | 101 | Vcc   | 102 | Vcc   |
| 31 | A1    | 32 | A4    | 103 | A6    | 104 | A7    |
| 33 | A2    | 34 | A5    | 105 | A8    | 106 | A11   |
| 35 | Vss   | 36 | Vss   | 107 | Vss   | 108 | Vss   |
| 37 | DQ8   | 38 | DQ40  | 109 | A9    | 110 | *A12  |
| 39 | DQ9   | 40 | DQ41  | 111 | A10   | 112 | NC    |
| 41 | DQ10  | 42 | DQ42  | 113 | Vcc   | 114 | Vcc   |
| 43 | DQ11  | 44 | DQ43  | 115 | /CAS2 | 116 | /CAS6 |
| 45 | Vcc   | 46 | Vcc   | 117 | /CAS3 | 118 | /CAS7 |
| 47 | DQ12  | 48 | DQ44  | 119 | Vss   | 120 | Vss   |
| 49 | DQ13  | 50 | DQ45  | 121 | DQ24  | 122 | DQ56  |
| 51 | DQ14  | 52 | DQ46  | 123 | DQ25  | 124 | DQ57  |
| 53 | DQ15  | 54 | DQ47  | 125 | DQ26  | 126 | DQ58  |
| 55 | Vss   | 56 | Vss   | 127 | DQ27  | 128 | DQ59  |
| 57 | NC    | 58 | NC    | 129 | Vcc   | 130 | Vcc   |
| 59 | NC    | 60 | NC    | 131 | DQ28  | 132 | DQ60  |
| 61 | NC    | 62 | NC    | 133 | DQ29  | 134 | DQ61  |
| 63 | Vcc   | 64 | Vcc   | 135 | DQ30  | 136 | DQ62  |
| 65 | NC    | 66 | NC    | 137 | DQ31  | 138 | DQ63  |
| 67 | /WE   | 68 | NC    | 139 | Vss   | 140 | Vss   |
| 69 | /RAS0 | 70 | NC    | 141 | SDA   | 142 | SCL   |
| 71 | NC    | 72 | NC    | 143 | Vcc   | 144 | Vcc   |

NOTE :

1.A12 is used for 8K-Refresh Product (HYM5V64434A Q-Series)

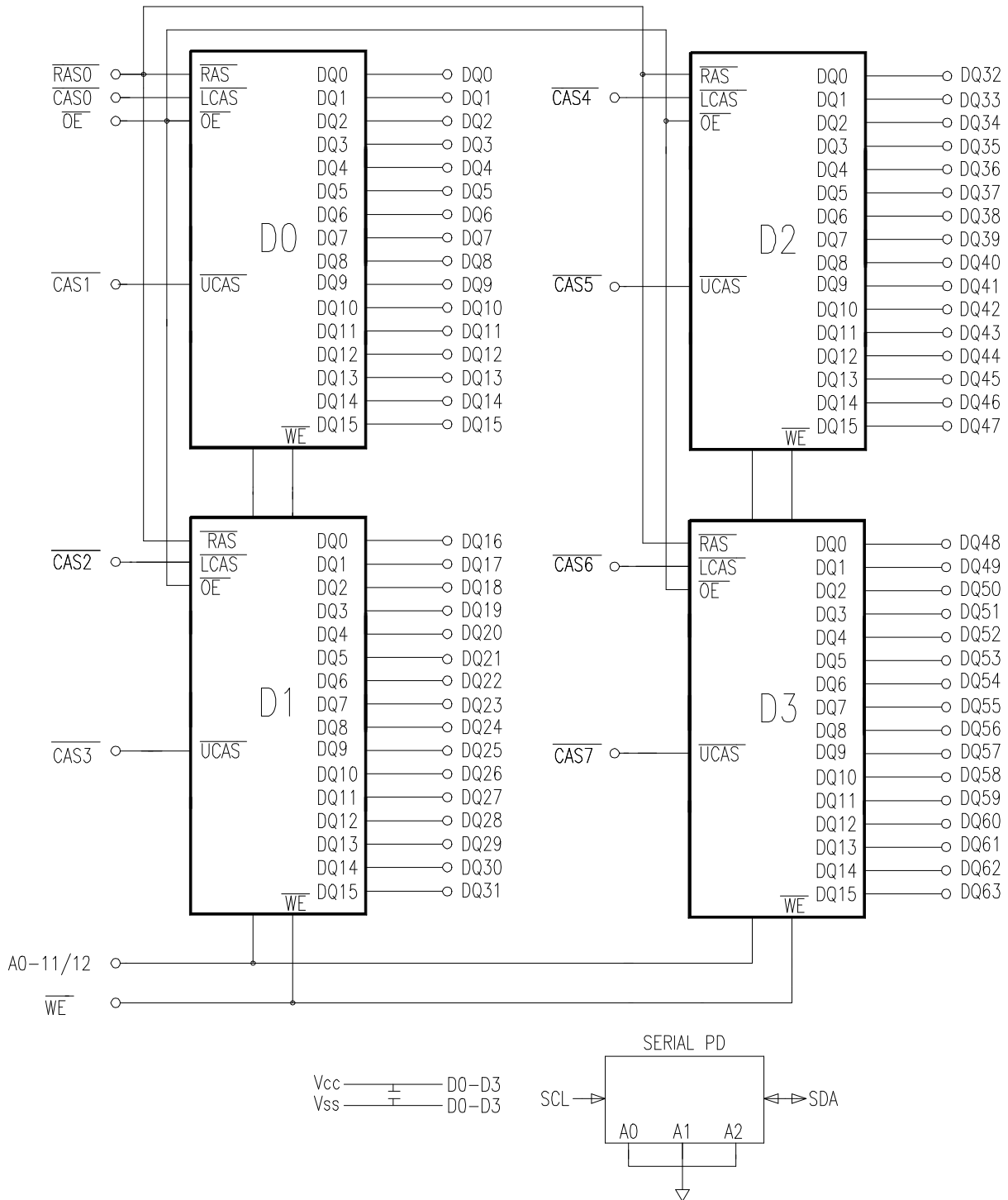
**SERIAL PRESENCE DETECT**

| BYTE NUMBER | FUNCTION DESCRIBED                                          | FUNCTION                     |              | VALUE      |
|-------------|-------------------------------------------------------------|------------------------------|--------------|------------|
| BYTE0       | # of Byte Written into Serial Memory at Module Manufacturer | 128 Bytes                    |              | 80h        |
| BYTE1       | Total # of Bytes of SPD Memory Device                       | 256 Bytes                    |              | 08h        |
| BYTE2       | Fundamental Memory Type                                     | EDO                          |              | 02h        |
| BYTE3       | # of Row Addresses on This Assembly                         | 12(4K Ref)                   |              | 0Ch        |
|             |                                                             | 13(8K Ref)                   |              | 0Dh        |
| BYTE4       | # of Column Addresses on This Assembly                      | 10(4K Ref)                   |              | 0Ah        |
|             |                                                             | 9(8K Ref)                    |              | 09h        |
| BYTE5       | # of Module Banks on This Assembly                          | 1 Bank                       |              | 01h        |
| BYTE6       | Data Width of This Assembly                                 | 64 Bits                      |              | 40h        |
| BYTE7       | Data Width of This Assembly(Continued)                      | -                            |              | 00h        |
| BYTE8       | Voltage Interface Standard of This Assembly                 | LVTTTL                       |              | 01h        |
| BYTE9       | tRAC                                                        | 50ns                         |              | 32h        |
|             |                                                             | 60ns                         |              | 3Ch        |
| BYTE10      | tCAC                                                        | 13ns                         |              | 0Dh        |
|             |                                                             | 15ns                         |              | 0Fh        |
| BYTE11      | DIMM Configuration Type                                     | None                         |              | 00h        |
| BYTE12      | Refresh Rate/Type                                           | 4K/8K Ref, Normal(15.6μs)    |              | 00h        |
|             |                                                             | 4K/8K Ref, SL-Part (31.25μs) |              | 83h        |
| BYTE13      | Primary DRAM Width                                          | x16                          |              | 10h        |
| BYTE14      | Error Checking DRAM Width                                   | None                         |              | 00h        |
| BYTE15-61   | Undefined                                                   | Undefined                    |              | FFh        |
| BYTE62      | SPD Data Revision Code                                      | Initial                      |              | 00h        |
| BYTE63      | Checksum for Byte 0-62                                      | 4K/8K Ref. Normal(15.6μs)    | 50ns<br>60ns | 02h<br>0Eh |
|             |                                                             | 4K/8K Ref. SL-Part(31.25μs)  | 50ns<br>60ns | 85h<br>91h |
| BYTE64-125  | Manufacturer Data Field                                     | HYUNDAI MFD                  |              | -          |
| BYTE126-127 | Reserved                                                    | Reserved                     |              | FFh        |
| BYTE128-255 | Undefined                                                   | Undefined                    |              | FFh        |

**NOTE :**

- 1.Serial PD interface is standard IIC architecture.
- 2.Pull-up resistors(4.7K typical value) are required on all open collector bus devices(SCL and SDA).
- 3.Current sink capability on SCL and SDA (Iol max) must be at least 3mA to maintain a valid low level.
- 4.Checksum can be obtained by adding the binary values in Byte 0-62, and eliminate all but low order byte.  
The low order byte would be the `Checksum`.
- 5.Refer to HYUNDAI Manufacturer Data SPEC for Byte 64-125.

**BLOCK DIAGRAM**



**NOTE :**  
 1.A12 is used for 8K-Refresh Product (HYM5V64434A Q-Series)

**ABSOLUTE MAXIMUM RATINGS**

| SYMBOL                             | PARAMETER                                      | RATING      | UNIT   |
|------------------------------------|------------------------------------------------|-------------|--------|
| T <sub>A</sub>                     | Ambient Temperature                            | 0 to 70     | °C     |
| T <sub>STG</sub>                   | Storage Temperature                            | -55 to 150  | °C     |
| V <sub>IN</sub> , V <sub>OUT</sub> | Voltage on Any Pin relative to V <sub>SS</sub> | -0.5 to 4.6 | V      |
| V <sub>CC</sub>                    | Voltage on VCC relative to V <sub>SS</sub>     | -0.5 to 4.6 | V      |
| I <sub>OS</sub>                    | Short Circuit Output Current                   | 50          | mA     |
| P <sub>D</sub>                     | Power Dissipation                              | 4           | W      |
| T <sub>SOLDER</sub>                | Soldering Temperature•Time                     | 260•10      | °C•sec |

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(T<sub>A</sub>=0°C to 70°C )

| SYMBOL          | PARAMETER            | MIN. | TYP. | MAX.                 | UNIT |
|-----------------|----------------------|------|------|----------------------|------|
| V <sub>CC</sub> | Power Supply Voltage | 3.0  | 3.3  | 3.6                  | V    |
| V <sub>IH</sub> | Input High Voltage   | 2.0  | -    | V <sub>CC</sub> +0.3 | V    |
| V <sub>IL</sub> | Input Low Voltage    | -0.3 | -    | 0.8                  | V    |

Note: All voltages are referenced to V<sub>SS</sub>.

**DC CHARACTERISTICS**

( $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC}=3.3\text{V} \pm 10\%$ ,  $V_{SS}=0\text{V}$ , unless otherwise noted.)

| Symbol           | Parameter                         | Test Conditions                                                                                                                                                                                                   | Speed    | Max. Current |            | Unit |
|------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------------|------------|------|
|                  |                                   |                                                                                                                                                                                                                   |          | 8K Product   | 4K Product |      |
| I <sub>CC1</sub> | Operating Current                 | /RAS, /CAS Cycling<br>t <sub>RC</sub> =t <sub>RC</sub> (min.)                                                                                                                                                     | 50<br>60 | 440<br>360   | 560<br>480 | mA   |
| I <sub>CC2</sub> | LVTTL Standby Current             | /RAS = /CAS $\geq V_{IH}$<br>other inputs $\geq V_{SS}$                                                                                                                                                           |          | 4            | 4          | mA   |
| I <sub>CC3</sub> | /RAS-only Refresh Current         | /RAS cycling<br>/CAS = $V_{IH}$<br>t <sub>RC</sub> = t <sub>RC</sub> (min.)                                                                                                                                       | 50<br>60 | 440<br>360   | 560<br>480 | mA   |
| I <sub>CC4</sub> | EDO Mode Current                  | /CAS cycling<br>/RAS = $V_{IL}$<br>t <sub>HPC</sub> = t <sub>HPC</sub> (min.)                                                                                                                                     | 50<br>60 | 480<br>400   | 520<br>440 | mA   |
| I <sub>CC5</sub> | CMOS Standby Current              | /RAS = /CAS $\geq V_{CC} - 0.2\text{V}$                                                                                                                                                                           | SL-part  | 2<br>1.2     | 2<br>1.2   | mA   |
| I <sub>CC6</sub> | /CAS-before-/RAS Refresh Current  | t <sub>RC</sub> =t <sub>RC</sub> (min.)                                                                                                                                                                           | 50<br>60 | 440<br>360   | 560<br>480 | mA   |
| I <sub>CC7</sub> | Battery Back-up Current (SL-part) | $V_{IH} = V_{CC} - 0.2\text{V}$ , $V_{IL} = 0.2\text{V}$<br>/CAS = CBR cycling or 0.2V<br>/OE & /WE = $V_{IH} = V_{CC} - 0.2\text{V}$<br>Address = Don't care<br>DQs = Open, t <sub>RC</sub> =31.25 $\mu\text{s}$ |          | 2.2          | 2.2        | mA   |
| I <sub>CC8</sub> | Self Refresh Current (SL-part)    | /RAS & /CAS = 0.2V<br>Other pins are same as I <sub>CC7</sub>                                                                                                                                                     |          | 1.8          | 1.8        | mA   |

| Symbol          | Parameter                         | Test Condition                                                                      | Min. | Max | Unit          |
|-----------------|-----------------------------------|-------------------------------------------------------------------------------------|------|-----|---------------|
| I <sub>LI</sub> | Input Leakage current(Any Input)  | $V_{SS} \leq V_{IN} \leq V_{CC} + 0.3$ ,<br>All other pins not under test= $V_{SS}$ | -20  | 20  | $\mu\text{A}$ |
| I <sub>LO</sub> | Output Leakage current(Any Input) | $V_{SS} \leq V_{OUT} \leq V_{CC}$<br>/RAS & /CAS at $V_{IH}$                        | -5   | 5   | $\mu\text{A}$ |
| V <sub>OL</sub> | Output Low Voltage                | I <sub>OL</sub> = 2.0mA                                                             | -    | 0.4 | V             |
| V <sub>OH</sub> | Output High Voltage               | I <sub>OH</sub> = -2.0mA                                                            | 2.4  | -   | V             |

**NOTE**

- I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> dependent on output loading and cycle rates(t<sub>RC</sub> and t<sub>HPC</sub>).
- Specified values are obtained with outputs unloaded.
- I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC6</sub>, address can be changed only once while /RAS= $V_{IL}$ . In I<sub>CC4</sub>, address can be changed maximum once while /CAS= $V_{IH}$  within one EDO mode cycle time t<sub>HPC</sub>.
- Only /RAS(max.) = 1 $\mu\text{s}$  is applied to refresh of battery backup but t<sub>RAS</sub>(max.) = 10 $\mu\text{s}$  is applied to normal functional operation.
- I<sub>CC5</sub>(max.) = 1.2mA, I<sub>CC7</sub> and I<sub>CC8</sub> are applied to SL-part only.
- V<sub>OH</sub> = 2.0V, V<sub>OL</sub> = 0.8V at AC Functional Test.

**AC CHARACTERISTICS**

(T<sub>A</sub>=0°C to 70°C , V<sub>cc</sub>=3.3V ± 10%, V<sub>ss</sub>=0V, unless otherwise noted.)

| #  | SYMBOL | PARAMETER                                 | HYH5V64404A / HYM5V64434A |      |      |      |      |      | UNIT | NOTE      |
|----|--------|-------------------------------------------|---------------------------|------|------|------|------|------|------|-----------|
|    |        |                                           | -50                       |      | -60  |      | -70  |      |      |           |
|    |        |                                           | MIN.                      | MAX. | MIN. | MAX. | MIN. | MAX. |      |           |
| 1  | tRC    | Random Read or Write Cycle Time           | 90                        | -    | 110  | -    |      |      | ns   |           |
| 2  | tRWC   | Read-Modify-Write Cycle Time              | 128                       | -    | 153  | -    |      |      | ns   |           |
| 3  | tHPC   | EDO Mode Cycle Time                       | 25                        | -    | 30   | -    |      |      | ns   |           |
| 4  | tHPRWC | EDO Mode Read-Modify-Write Cycle Time     | 67                        | -    | 73   | -    |      |      | ns   |           |
| 5  | tRAC   | Access Time from /RAS                     | -                         | 50   | -    | 60   |      |      | ns   | 4,5,10,11 |
| 6  | tCAC   | Access Time from /CAS                     | -                         | 13   | -    | 15   |      |      | ns   | 4,5,10    |
| 7  | tAA    | Access Time from Column Address           | -                         | 25   | -    | 30   |      |      | ns   | 4,5,11    |
| 8  | tCPA   | Access Time from /CAS Precharge           | -                         | 28   | -    | 35   |      |      | ns   | 4         |
| 9  | tCLZ   | /CAS to Output Low Impedance              | 3                         | -    | 3    | -    |      |      | ns   | 3         |
| 10 | tCEZ   | Output Buffer Turn-off delay from /CAS    | 3                         | 13   | 3    | 13   |      |      | ns   |           |
| 11 | tT     | Transition Time (Rise and Fall)           | 2                         | 50   | 2    | 50   |      |      | ns   | 4         |
| 12 | tRP    | /RAS Precharge Time                       | 30                        | -    | 40   | -    |      |      | ns   |           |
| 13 | tRAS   | /RAS Pulse Width                          | 50                        | 10K  | 60   | 10K  |      |      | ns   |           |
| 14 | tRASP  | /RAS Pulse Width (EDO Mode)               | 50                        | 100K | 60   | 100K |      |      | ns   |           |
| 15 | tRSH   | /RAS Hold Time                            | 13                        | -    | 15   | -    |      |      | ns   |           |
| 16 | tCSH   | /CAS Hold Time                            | 40                        | -    | 45   | -    |      |      | ns   |           |
| 17 | tCAS   | /CAS Pulse Width                          | 8                         | 10K  | 10   | 10K  |      |      | ns   |           |
| 18 | tRCD   | /RAS to /CAS Delay                        | 17                        | 37   | 20   | 45   |      |      | ns   | 10        |
| 19 | tRAD   | /RAS to Column Address Delay Time         | 13                        | 25   | 15   | 30   |      |      | ns   | 11        |
| 20 | tCRP   | /CAS to /RAS Precharge Time               | 5                         | -    | 5    | -    |      |      | ns   |           |
| 21 | tCP    | /CAS Precharge Time                       | 8                         | -    | 10   | -    |      |      | ns   |           |
| 22 | tASR   | Row Address Set-up Time                   | 0                         | -    | 0    | -    |      |      | ns   |           |
| 23 | tRAH   | Row Address Hold Time                     | 8                         | -    | 10   | -    |      |      | ns   |           |
| 24 | tASC   | Column Address Set-up Time                | 0                         | -    | 0    | -    |      |      | ns   |           |
| 25 | tCAH   | Column Address Hold Time                  | 8                         | -    | 10   | -    |      |      | ns   |           |
| 26 | tAR    | Column Address Hold Time from /RAS        | 45                        | -    | 50   | -    |      |      | ns   |           |
| 27 | tRAL   | Column Address to /RAS Lead Time          | 25                        | -    | 30   | -    |      |      | ns   |           |
| 28 | tRCS   | Read Command Set-up Time                  | 0                         | -    | 0    | -    |      |      | ns   |           |
| 29 | tRCH   | Read Command Hold Time Referenced to /CAS | 0                         | -    | 0    | -    |      |      | ns   | 7         |
| 30 | tRRH   | Read Command Hold Time Referenced to /RAS | 0                         | -    | 0    | -    |      |      | ns   | 7         |
| 31 | tWCH   | Write Command Hold Time                   | 10                        | -    | 10   | -    |      |      | ns   |           |
| 32 | tWCR   | Write Command Hold Time from /RAS         | 40                        | -    | 45   | -    |      |      | ns   |           |
| 33 | tWP    | Write Command Pulse Width                 | 8                         | -    | 10   | -    |      |      | ns   |           |
| 34 | tRWL   | Write Command to /RAS Lead Time           | 15                        | -    | 15   | -    |      |      | ns   |           |
| 35 | tCWL   | Write Command to /CAS Lead Time           | 8                         | -    | 10   | -    |      |      | ns   |           |

**AC CHARACTERISTICS**

(Continued)

| #  | SYMBOL | PARAMETER                                  | HYH5V64404A / HYM5V64434A |      |      |      |      |      | UNIT | NOTE  |
|----|--------|--------------------------------------------|---------------------------|------|------|------|------|------|------|-------|
|    |        |                                            | -50                       |      | -60  |      | -70  |      |      |       |
|    |        |                                            | MIN.                      | MAX. | MIN. | MAX. | MIN. | MAX. |      |       |
| 36 | tDS    | Data-In Set-up Time                        | 0                         | -    | 0    | -    |      |      | ns   | 8     |
| 37 | tDH    | Data-In Hold Time                          | 10                        | -    | 10   | -    |      |      | ns   | 8     |
| 38 | tDHR   | Data-In Hold Time Referenced to /RAS       | 40                        | -    | 45   | -    |      |      | ns   |       |
| 39 | tREF   | Refresh Period (8192 cycles)               | -                         | 64   | -    | 64   |      |      | ms   | 12,13 |
|    |        | Refresh Period (4096 cycles)               | -                         | 64   | -    | 64   |      |      | ms   | 12    |
|    |        | Refresh Period (SL-part)                   | -                         | 128  | -    | 128  |      |      | ms   | 12,13 |
| 40 | tWCS   | Write Command Set-up Time                  | 0                         | -    | 0    | -    |      |      | ns   | 9     |
| 41 | tCWD   | /CAS to /WE Delay Time                     | 34                        | -    | 36   | -    |      |      | ns   | 9     |
| 42 | tRWD   | /RAS to /WE Delay Time                     | 70                        | -    | 80   | -    |      |      | ns   | 9     |
| 43 | tAWD   | Column Address to /WE Delay Time           | 45                        | -    | 50   | -    |      |      | ns   | 9     |
| 44 | tCSR   | /CAS Set-up Time (CBR Cycle)               | 5                         | -    | 5    | -    |      |      | ns   |       |
| 45 | tCHR   | /CAS Hold Time (CBR Cycle)                 | 10                        | -    | 10   | -    |      |      | ns   |       |
| 46 | tRPC   | /RAS to /CAS Precharge Time                | 5                         | -    | 5    | -    |      |      | ns   |       |
| 47 | tCPT   | /CAS Precharge Time (CBR Counter Test)     | 25                        | -    | 30   | -    |      |      | ns   |       |
| 48 | tROH   | /RAS Hold Time Referenced to /OE           | 0                         | -    | 0    | -    |      |      | ns   |       |
| 49 | tOEA   | /OE Access Time                            | -                         | 13   | -    | 15   |      |      | ns   |       |
| 50 | tOED   | /OE to Data Delay                          | 13                        | -    | 15   | -    |      |      | ns   |       |
| 51 | tOEZ   | Output Buffer Turn-Off Delay Time from /OE | 0                         | 10   | 0    | 15   |      |      | ns   | 6     |
| 52 | tOEH   | /OE Command Hold Time                      | 13                        | -    | 15   | -    | -    | --   | ns   |       |
| 53 | tCPWD  | /WE Delay Time from /CAS Precharge         | 45                        | -    | 54   | -    |      |      | ns   | 9     |
| 54 | tRHCP  | /RAS Hold Time from /CAS Precharge         | 30                        | -    | 35   | -    |      |      | ns   |       |
| 55 | tWRP   | /WE to /RAS Precharge Time(CBR cycle)      | 10                        | -    | 10   | -    |      |      | ns   |       |
| 56 | tWRH   | /WE to /RAS Hold Time (CBR cycle)          | 10                        | -    | 10   | -    |      |      | ns   |       |
| 57 | tWTS   | Write Command Set-up Time (Test Mode In)   | 10                        | -    | 10   | -    |      |      | ns   |       |
| 58 | tWTH   | Write Command Hold Time (Test Mode In)     | 10                        | -    | 10   | -    |      |      | ns   |       |
| 59 | tRASS  | /RAS Pulse Width (Self Refresh)            | 100K                      | -    | 100K | -    |      |      | us   |       |
| 60 | tRPS   | /RAS Precharge Time (Self Refresh)         | 100                       | -    | 100  | -    |      |      | ns   |       |
| 61 | tCHS   | /CAS Hold Time (Self Refresh)              | -50                       | -    | -50  | -    |      |      | ns   |       |
| 62 | tDOH   | Output Data Hold Time                      | 5                         | -    | 5    | -    |      |      | ns   |       |
| 63 | tREZ   | Output Buffer Turn-off Delay from /RAS     | 0                         | 10   | 0    | 15   |      |      | ns   | 6     |
| 64 | tWEZ   | Output Buffer Turn-off Delay from /WE      | 0                         | 10   | 0    | 15   |      |      | ns   | 6     |
| 65 | tWED   | /WE to Data Delay Time                     | 15                        | -    | 15   | -    |      |      | ns   |       |
| 66 | tOEP   | /OE Precharge Time                         | 5                         | -    | 5    | -    |      |      | ns   |       |
| 67 | tWPE   | /WE Pulse Width (EDO cycle)                | 5                         | -    | 5    | -    |      |      | ns   |       |
| 68 | tOCH   | /OE to /CAS Hold Time                      | 5                         | -    | 5    | -    |      |      | ns   |       |
| 69 | tCHO   | /CAS Hold Time to /OE                      | 5                         | -    | 5    | -    |      |      | ns   |       |



**NOTE**

1. An initial pause of 200 $\mu$ s is required after power-up followed by 8 /RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS-before-/RAS initialization cycles instead of 8 /RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode during initialization.
2. If /RAS=Vss during power-up, the HYM5V64404A / HYM5V64434A could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up.
3. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
4. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.), and are assumed to be 5ns for all inputs.
5. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 1 TTL loads and 100pF.
6. tWEZ, tREZ, tCEZ and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles and late Write cycle.
9. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS  $\geq$  tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD  $\geq$  tRWD(min.), tCWD  $\geq$  tCWD(min.), tAWD  $\geq$  tAWD(min.), and tCPWD  $\geq$  tCPWD(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
10. Operation within the tRCD(max.) limit ensures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
11. Operation within the tRAD(max.) limit ensures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
12. tREF(max.)=128ms is applied to SL-parts.
13. A burst of 8192 /RAS-only refresh cycles must be executed within 64ms (128ms for SL-parts) after exiting self refresh. (CBR refresh & Hidden refresh : 4K cycle/64ms)

**CAPACITANCE**

(TA=0°C to 70°C, Vcc=3.3V  $\pm$  10%, Vss=0V, f = 1MHz, unless otherwise noted.)

| SYMBOL | PARAMETER                            | TYP. | MAX. | UNIT |
|--------|--------------------------------------|------|------|------|
| CIN1   | Input Capacitance (A0 - A12)         | -    | 28   | pF   |
| CIN2   | Input Capacitance (/WE, /OE)         | -    | 38   | pF   |
| CIN3   | Input Capacitance (/RAS0)            | -    | 38   | pF   |
| CIN4   | Input Capacitance (/CAS0 - /CAS7)    | -    | 14   | pF   |
| CDQ    | Data Input /Output Capacitance (DQs) | -    | 14   | pF   |

UNIT : INCH(mm)  
TOLERANCE : +/-0.0059(0.15)



**ORDERING INFORMATION**

| Part Number      | Ref. | Power   | Package |
|------------------|------|---------|---------|
| HYM5V64404ATQG   | 4K   | Normal  | TSOP    |
| HYM5V64404ASLTQG | 4K   | SL-part | TSOP    |
| HYM5V64434ATQG   | 8K   | Normal  | TSOP    |
| HYM5V64434ASLTQG | 8K   | SL-part | TSOP    |