

FEATURES

- Fast Access Times: *20/25/35 ns
- Space Saving 400-Mil DIP
- High Density 400-Mil SOJ Package
- Low Standby Power
- TTL Compatible I/O
- $5V \pm 10\%$ Supply
- Fully Static Operation
- Three State Output
- JEDEC Standard Pinout

*20 nanoseconds is advanced information only.

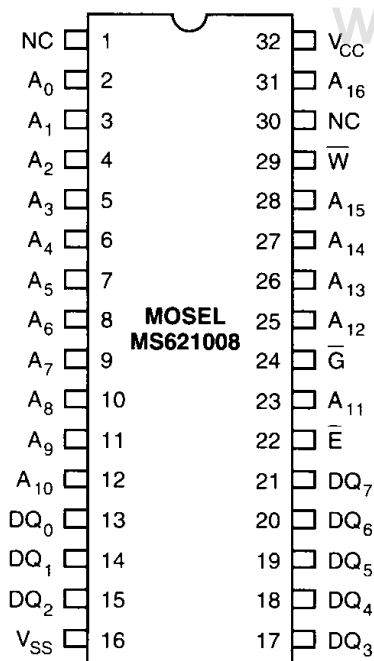
DESCRIPTION

The MS621008 is a high speed 1M-bit static RAM organized as 128K x 8. Fully static in operation, the Chip Enable ($\bar{E}$) control places the RAM in a low-power standby mode when inactive (HIGH). Standby power drops to its lowest level (I_{SB1}) when $\bar{E}$ is raised to within 0.2V of V_{CC} .

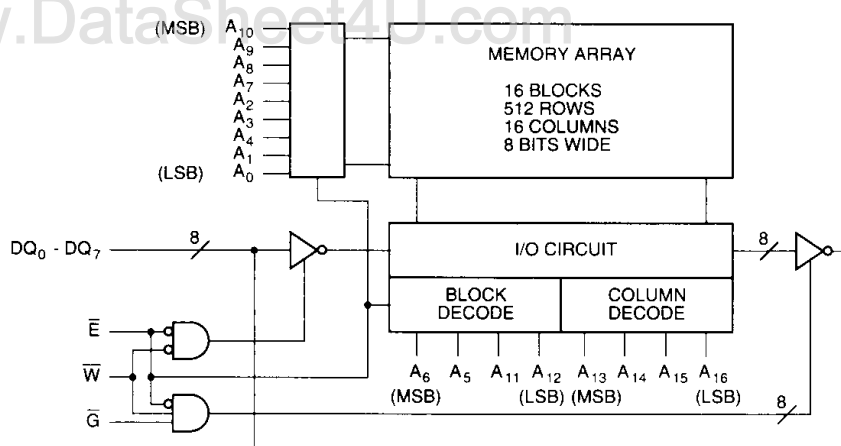
Write cycles occur when both Chip Enable ($\bar{E}$) and Write Enable ($\bar{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the address lines. The Output Enable Control ($\bar{G}$) can prevent bus contention.

High frequency design techniques should be employed to obtain optimum performance from this device. Solid, low impedance power and ground planes, with high frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



MS621008

PIN DESCRIPTIONS

$A_0 - A_{16}$ Address Inputs

These 17 address inputs select one of the 128K x 8 bit segments in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory locations.

DQ₀ - DQ₇ Data Input and Data Output Ports

These 8 bidirectional ports are used to read data from and write data into the RAM.

V_{CC} Power Supply

V_{SS} Ground

TRUTH TABLE

MODE	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D _{OUT}
Read	L	H	H	High Z
Write	L	X	L	D _{IN}

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V _{CC}
Commercial	0°C to +70°C	5V ± 10%

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

PARAMETER NAME	PARAMETER		RATING	UNITS
V _{CC}	Supply Voltage		-0.3 to 7	V
V _{IN}	Input Voltage		-0.3 to 7	V
V _{DQ}	Input/Output Voltage Applied		-0.3 to 6	V
T _{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T _{STG}	Storage Temperature	Plastic	-65 to +150	°C
P _D	Power Dissipation		1.0	W
I _{OUT}	D C Output Current		±40 ⁽²⁾	mA

See Notes following "SWITCHING CHARACTERISTICS".

DC ELECTRICAL CHARACTERISTICS (0°C to +70°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Supply Voltage		0	0	0	V
V_{IL}	Guaranteed Input LOW Voltage ⁽³⁾		-0.5		0.8	V
V_{IH}	Guaranteed Input HIGH Voltage		2.2		$V_{CC} + 0.5$	V
I_{CC1}	Operating Current ⁽⁴⁾	Output open, $t_{CYCLE} = 20ns$			150	mA
I_{CC1}	Operating Current ⁽⁴⁾	Output open, $t_{CYCLE} = 25ns$			140	mA
I_{CC1}	Operating Current ⁽⁴⁾	Output open, $t_{CYCLE} = 35ns$			120	mA
I_{SB1}	Standby Current	$\bar{E} \geq V_{CC} - 0.2V$		0.1	2	mA
I_{SB2}	Standby Current	$\bar{E} \geq V_{IH}$			10	mA
I_{LI}	Input Leakage Current	$V_{in} = 0V$ to V_{CC}	-2		2	μA
I_{LO}	I/O Leakage Current	$V_{in} = 0V$ to V_{CC}	-10		10	μA
V_{OH}	Output High Voltage	$I_{OH} = -4.0mA$	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 8.0mA$			0.4	V

See Notes following "SWITCHING CHARACTERISTICS".

CAPACITANCE⁽¹⁾ ($T_A = 25^\circ C$, $f = 1.0MHz$)

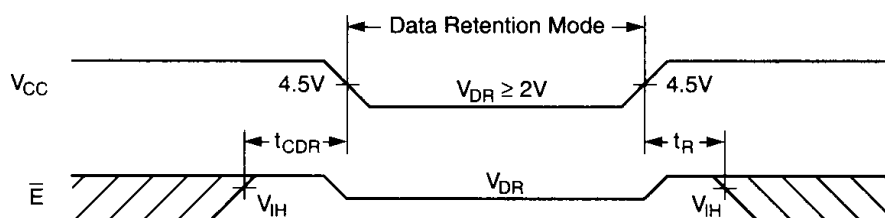
PARAMETER NAME	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
C_{DO}	I/O Capacitance	$V_{DO} = 0V$	8	pF

1. This parameter is guaranteed and not tested.

DATA RETENTION CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP. ⁽¹⁾	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention	$\bar{E} \geq V_{CC} - 0.2V$, $\bar{G} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\bar{E} \geq V_{CC} - 0.2V$, $\bar{G} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	500 ⁽²⁾	μA
I_{CDR}	Chip Deselected to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC} ⁽³⁾	-	-	ns

NOTES:

1. $V_{CC} = 2V$, $T_A = +25^\circ C$ 2. $V_{CC} = 3V$ 3. t_{RC} = Read Cycle TimeTIMING WAVEFORM LOW V_{CC} DATA RETENTION WAVEFORM

MS621008

AC ELECTRICAL CHARACTERISTICS (over the commercial operating range) ⁽⁶⁾

PARAMETER NAME	PARAMETER	-20		-25		-35		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE								
t _{RC}	Read Cycle Timing	20		25		35		ns
t _{AA}	Address Access Time		20		25		35	ns
t _{OH}	Output Hold from Address Change	3		3		3		ns
t _{EA}	$\bar{E}$ Low to Valid Data		20		25		35	ns
t _{ELZ}	$\bar{E}$ Low to Output Active ^{(7), (8)}	3		3		3		ns
t _{EHZ}	$\bar{E}$ High to Output High-Z ^{(7), (8)}		10		12		20	ns
t _{GA}	$\bar{G}$ Low to Valid Data		8		10		20	ns
t _{GLZ}	$\bar{G}$ Low to Output Active ^{(7), (8)}	0		0		0		ns
t _{GHZ}	$\bar{G}$ High to Output High-Z ^{(7), (8)}		8		10		20	ns
t _{PU}	$\bar{E}$ Low to Power Up Time ⁽⁸⁾	0		0		0		ns
t _{PD}	$\bar{E}$ High to Power Down Time ⁽⁸⁾		20		25		35	ns
WRITE CYCLE								
t _{WC}	Write Cycle Timing	20		25		35		ns
t _{EW}	$\bar{E}$ Low to End of Write	15		20		30		ns
t _{AW}	Address Valid to End of Write	15		20		30		ns
t _{AS}	Address Setup	0		0		0		ns
t _{AH}	Address Hold	0		0		0		ns
t _{WP}	$\bar{W}$ Pulse Width	15		20		25		ns
t _{DW}	Input Data Setup Time	12		15		15		ns
t _{DH}	Input Data Hold Time	0		0		0		ns
t _{WHZ}	$\bar{W}$ Low to Output High-Z ^{(7), (8)}		8		10		15	ns
t _{WLZ}	$\bar{W}$ High to Output Active ^{(7), (8)}	3		3		3		ns

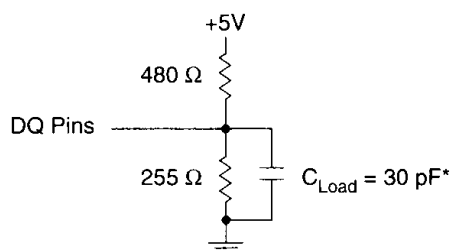
NOTES:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability, and degrade performance characteristics.
- Output should not be shorted for more than 30 seconds.
- Negative undershoot of up to 3.0V is permitted once per cycle.
- I_{CC} is dependent upon output loading and cycle rates. Specified values are with output open, operating at specified cycle times.
- Capacitances are maximum values at 25°C measured at 1.0 MHz with $V_{Bias}=0V$ and $V_{CC}=5.0V$.
- Switching Characteristics measurements specified at "AC Test Conditions" levels.
- Active output to High-Z and High-Z to active output tests specified for a $\pm 200mV$ transition from steady levels into the test load.
- Sample tested only.

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load, Timing Tests	See Figure Below

AC TEST LOAD



* Includes scope and jig capacitance

KEY TO SWITCHING WAVEFORMS

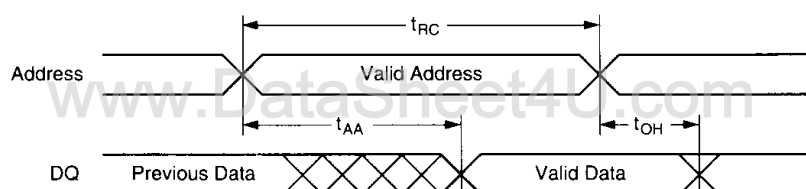
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

2

SWITCHING WAVEFORMS - READ CYCLE

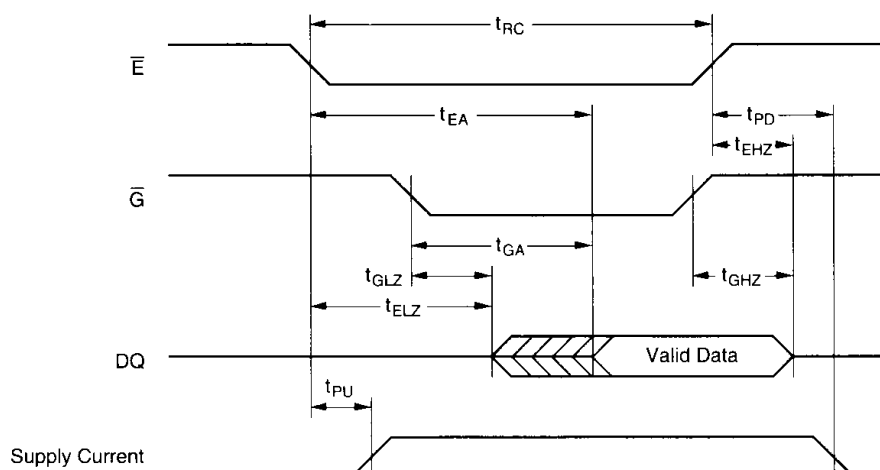
Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data-out implies that data lines are in Low-Z state but the data is not guaranteed to be valid until t_{AA} .



Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data-out is not specified to be valid until t_{EA} or t_{GA} , but may become valid as soon as t_{ELZ} or t_{GLZ} . Outputs will transition directly from High-Z to Valid Data-out. Valid data will be present following t_{GA} only if t_{EA} timing is met.



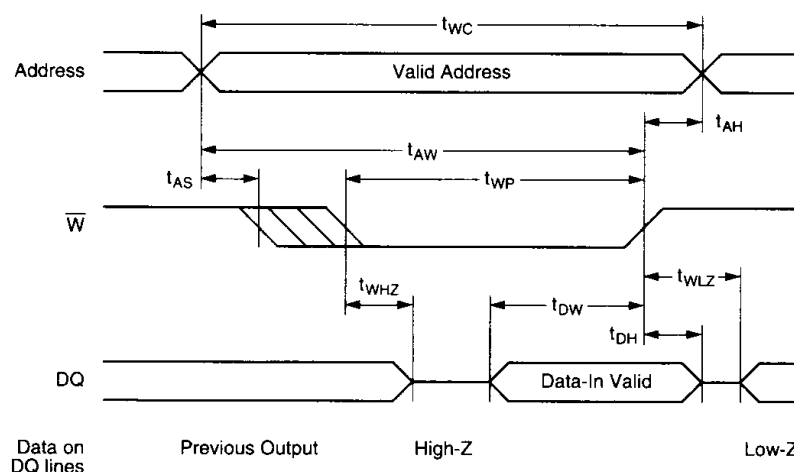
MS621008

SWITCHING WAVEFORM - WRITE CYCLE

Addresses must be stable during Write Cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, The outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Writes cycles. This will prevent the MS62008's outputs from becoming active, preventing bus contention, thereby reducing system noise.

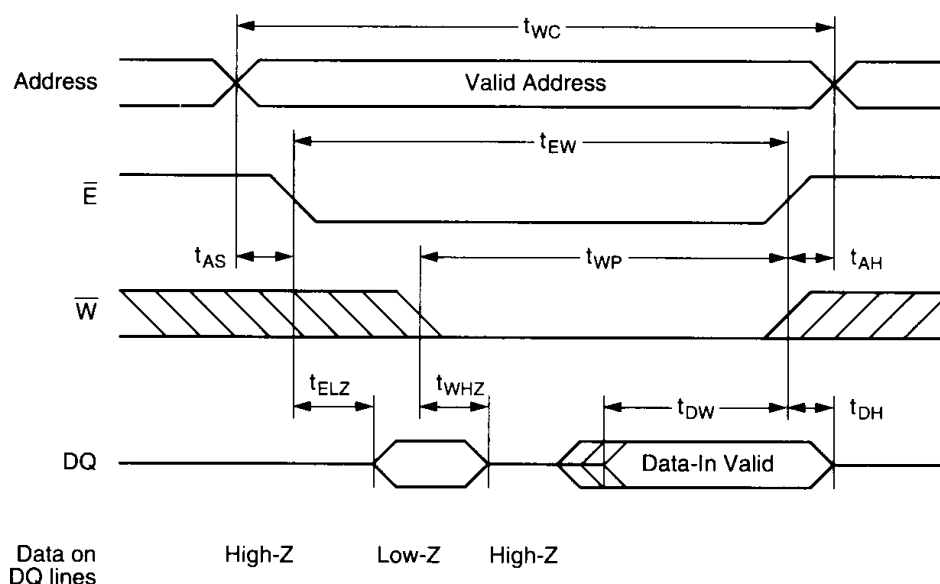
Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance, since both t_{WHZ} and t_{DW} timing specifications must be met.



Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.



MS621008**ORDERING INFORMATION**

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
20	MS621008-20EC	E32-1*	0°C to +70°C
25	MS621008-25EC	E32-1*	0°C to +70°C
35	MS621008-35EC	E32-1*	0°C to +70°C
20	MS621008-20KC	K32-1	0°C to +70°C
25	MS621008-25KC	K32-1	0°C to +70°C
35	MS621008-35KC	K32-1	0°C to +70°C

2

* Contact Factory for Package Drawing

www.DataSheet4U.com