68 X 69 3.2 GBPS DIFFERENTIAL CROSSPOINT SWITCH S2090

FEATURES

- SiGe BiCMOS Technology
- 68 x 69 differential crosspoint switch
- Broadcast and multicast switching capability
- Differential 200 mV to 1600 mV input data
- Differential 400 mV to 1400 mV programmable output swing
- Up to 3.2 Gbps NRZ data rate
- Power down of individual output drivers
- Parallel read back function
- LVTTL configuration controls
- Internal 100 Ω line to line terminations on high-speed differential inputs
- Reconfigurable without disturbing operation
- Single +3.3 V supply or +2.5 V supply
- 9.5 W typical power dissipation with 800 mV output swing
- Compact 32.5 mm x 32.5 mm 624 pin CBGA package
- Complies with Bellcore and ITU-T standards

APPLICATIONS

- Dense Wavelength Division Multiplexing (DWDM) systems
- Internet switches
- Digital video
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Datacom or telecom switching

GENERAL DESCRIPTION

The S2090 is a high-speed 68 x 69 differential crosspoint switch with both full broadcast and multicast capability. Any of its 68 differential LVPECL input signal pairs can be connected to any or all of its 69 differential CML output signal pairs.

The differential logic data path makes the part ideal for high-speed applications. The differential nature of the data path is retained throughout the crosspoint structure to minimize data distortion and to handle NRZ data rates up to 3.2 Gbps. The high-speed serial inputs to the S2090 are internally biased and have internal 100 Ω line-to-line terminations.

LVTTL configuration controls simplify interfacing to slower speed circuitry. Once a new configuration has been entered into the configuration register file, the S2090 can be completely reconfigured by pulsing the CONFIGN input.

Figure 1 shows a system block diagram incorporating the S2090 with other AMCC devices. Figure 2 shows the basic operation of the switch.

Figure 1. System Block Diagram

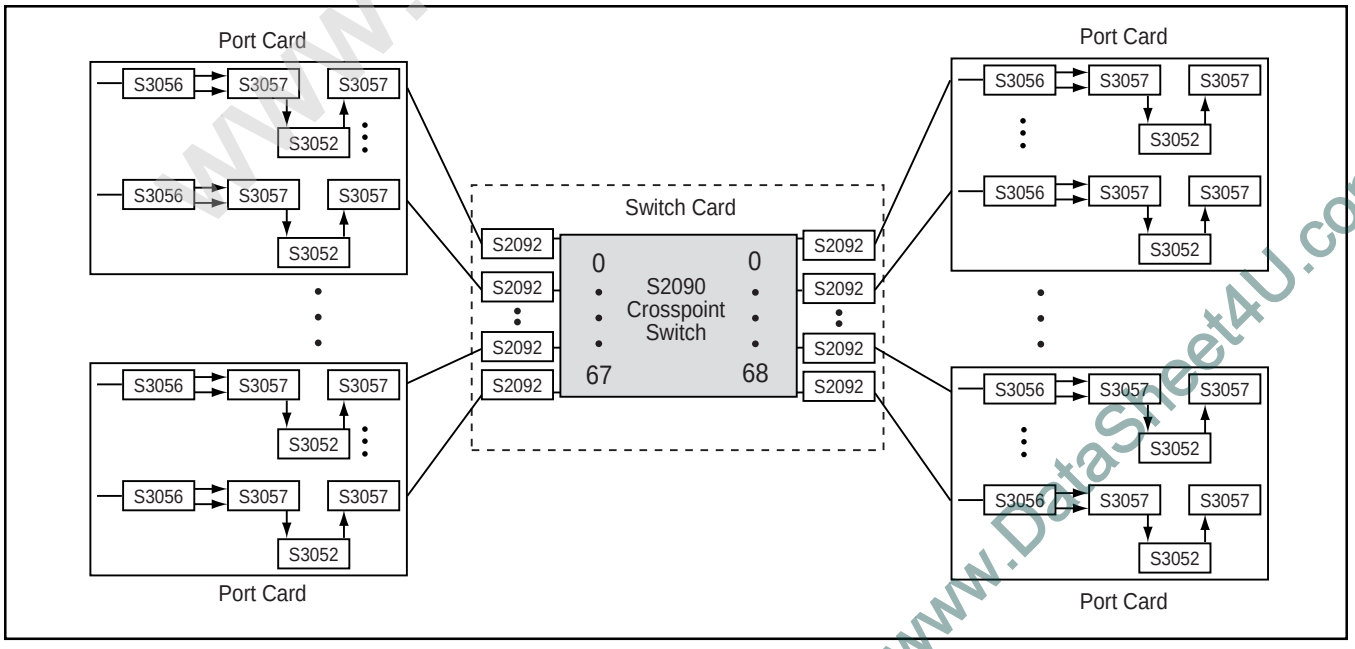
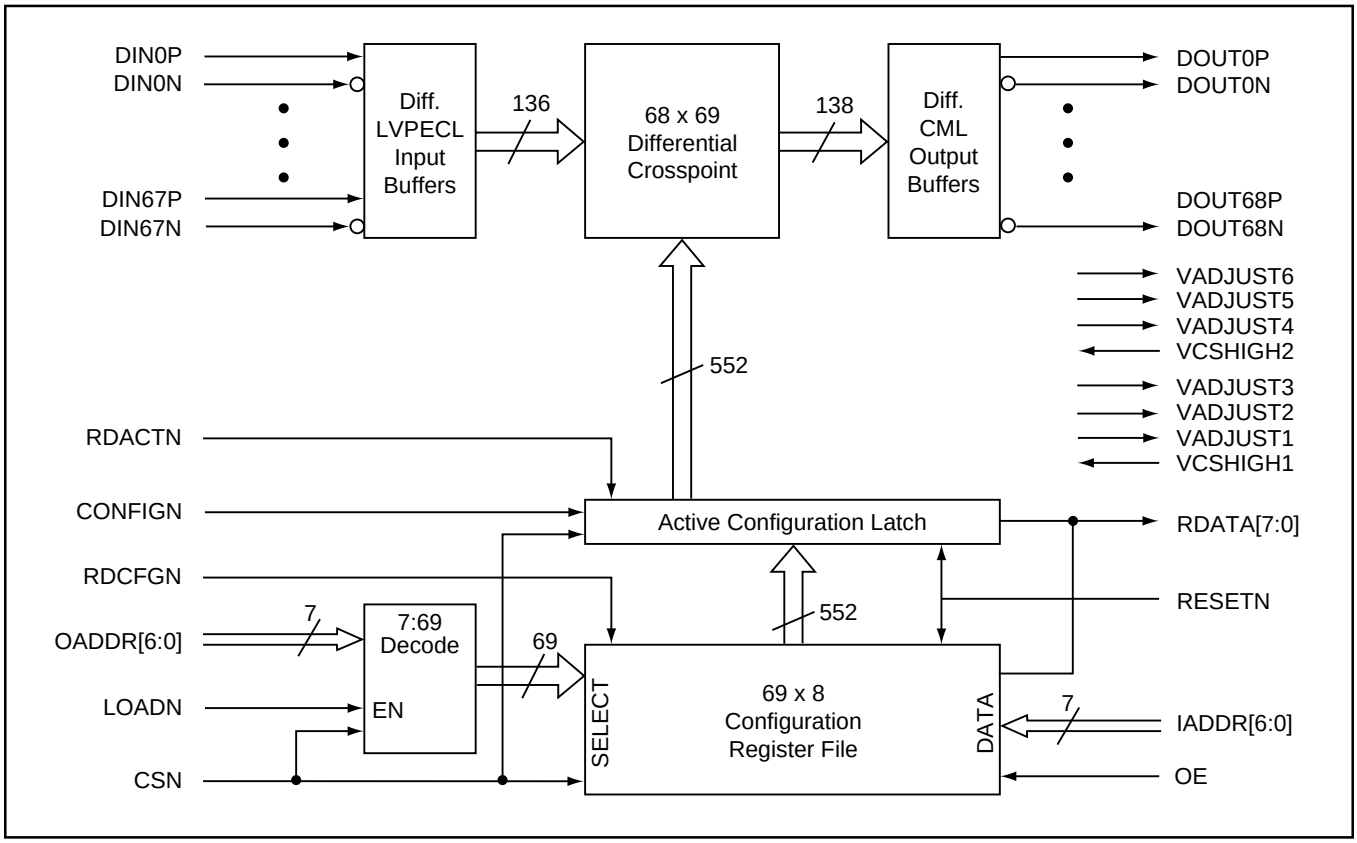


Figure 2. Functional Block Diagram



DATA TRANSFER

For each configured connection between a differential input pair and an enabled output pair, any data appearing at the input pair will be passed immediately through to the output pair.

CONFIGURATION

The S2090 can be selectively configured, either one output pair at a time, or any number of output pairs simultaneously. Configuration data is stored in 69 registers, one register for each output pair. The data in these 69 registers make up the configuration register file. As shown in Figure 2, the configuration data is passed in parallel from all 69 registers to a latch, which holds the active switch configuration. This two-stage arrangement allows one or more output pairs to be reconfigured simultaneously. A Chip Select pin (CSN) is provided to simplify interfacing this switch to the system microprocessor. When CSN is inactive, the LOADN, CONFIGN, RDCFGN, and RDACTN signals will be ignored. Therefore, no new addresses, configurations, or parallel readbacks will occur at the configuration register file or the active matrix. When CSN is active, the crosspoint will operate as specified.

The S2090 minimizes the configuration time through the use of the active configuration latch. While the switch is operational, and prior to the time at which it must be reconfigured, a new configuration is loaded into the configuration register file. Once the configuration register file contains the desired connection information and output pair driver enable information, the contents of the registers are transferred in parallel to the active configuration latch by the CONFIGN strobe.

To connect an output to a given input, the output to be configured is selected using the OADDR[6:0] (OADDR6 = MSB) inputs. See Table 1. With the output configuration register selected, the desired input selection must be provided in the IADDR[6:0] (IADDR6 = MSB) inputs. The IADDR[6:0] information is stored into the selected output configuration register by the LOADN strobe. The configuration process is described by the flow chart in Figure 5.

The active configuration latch can be made transparent by activating the CONFIGN input. When this is done, changes strobed into the output pair configuration registers by the LOADN input pair will be passed immediately to the switch.

The S2090 supports broadcast and multicast operations: any of the 68 differential inputs can be connected to any or all of the 69 differential outputs.

OUTPUT SWING ADJUST

The S2090 output swing can be adjusted by connecting one or more of the VADJUSTx pins to the VCSHIGHx pins. VADJUST1,2,3 controls the amplitude of outputs [0:31, 67, 68] and should be tied (when necessary) to VCSHIGH1. See Tables 2 and 2A. VADJUST4,5,6 controls the amplitude of outputs [32:66] and should be tied (when necessary) to VCSHIGH2. See Tables 3 and 3A. This type of setup allows the two sets of outputs specified to run at different output swings. The user can reduce power dissipation if one set of outputs is running at a lower output swing than the other set. Depending on the system application in which the crosspoint(s) is used, this implementation can assist if half the outputs are required to drive long backplane traces while the other half of the outputs need to only drive much shorter backplane traces or optical interfaces. This allows the user to have multiple transmission media options available for various system architectures. Note that as the output swing is increased, the power dissipated by the part is proportionally increased (see Tables 17 and 18). The typical output swing range for +3.3 V power supply is from 400 mVpp differential up to 1200 mVpp differential per Tables 2 and 2A. The typical output swing range for +2.5 V power supply is from 300 mVpp differential up to 900 mVpp differential per Tables 3 and 3A.

Table 1. Input/Output Addresses of S2090[1]

DIFF INPUT	IADDR6	IADDR5	IADDR4	IADDR3	IADDR2	IADDR1	IADDR0	DIFF OUTPUT	OADDR6	OADDR5	OADDR4	OADDR3	OADDR2	OADDR1	OADDR0
DIN0	0	0	0	0	0	0	0	**DOUT0**	0	0	0	0	0	0	0
DIN1	0	0	0	0	0	0	1	**DOUT1**	0	0	0	0	0	0	1
DIN2	0	0	0	0	0	1	0	**DOUT2**	0	0	0	0	0	1	0
DIN3	0	0	0	0	0	1	1	**DOUT3**	0	0	0	0	0	1	1
DIN4	0	0	0	0	1	0	0	**DOUT4**	0	0	0	0	1	0	0
DIN5	0	0	0	0	1	0	1	**DOUT5**	0	0	0	0	1	0	1
DIN6	0	0	0	0	1	1	0	**DOUT6**	0	0	0	0	1	1	0
DIN7	0	0	0	0	1	1	1	**DOUT7**	0	0	0	0	1	1	1
DIN8	0	0	0	1	0	0	0	**DOUT8**	0	0	0	1	0	0	0
DIN9	0	0	0	1	0	0	1	**DOUT9**	0	0	0	1	0	0	1
DIN10	0	0	0	1	0	1	0	**DOUT10**	0	0	0	1	0	1	0
DIN11	0	0	0	1	0	1	1	**DOUT11**	0	0	0	1	0	1	1
DIN12	0	0	0	1	1	0	0	**DOUT12**	0	0	0	1	1	0	0
DIN13	0	0	0	1	1	0	1	**DOUT13**	0	0	0	1	1	0	1
DIN14	0	0	0	1	1	1	0	**DOUT14**	0	0	0	1	1	1	0
DIN15	0	0	0	1	1	1	1	**DOUT15**	0	0	0	1	1	1	1
DIN16	0	0	1	0	0	0	0	**DOUT16**	0	0	1	0	0	0	0
DIN17	0	0	1	0	0	0	1	**DOUT17**	0	0	1	0	0	0	1
DIN18	0	0	1	0	0	1	0	**DOUT18**	0	0	1	0	0	1	0
DIN19	0	0	1	0	0	1	1	**DOUT19**	0	0	1	0	0	1	1
DIN20	0	0	1	0	1	0	0	**DOUT20**	0	0	1	0	1	0	0
DIN21	0	0	1	0	1	0	1	**DOUT21**	0	0	1	0	1	0	1
DIN22	0	0	1	0	1	1	0	**DOUT22**	0	0	1	0	1	1	0
DIN23	0	0	1	0	1	1	1	**DOUT23**	0	0	1	0	1	1	1
DIN24	0	0	1	1	0	0	0	**DOUT24**	0	0	1	1	0	0	0
DIN25	0	0	1	1	0	0	1	**DOUT25**	0	0	1	1	0	0	1
DIN26	0	0	1	1	0	1	0	**DOUT26**	0	0	1	1	0	1	0
DIN27	0	0	1	1	0	1	1	**DOUT27**	0	0	1	1	0	1	1
DIN28	0	0	1	1	1	0	0	**DOUT28**	0	0	1	1	1	0	0
DIN29	0	0	1	1	1	0	1	**DOUT29**	0	0	1	1	1	0	1
DIN30	0	0	1	1	1	1	0	**DOUT30**	0	0	1	1	1	1	0
DIN31	0	0	1	1	1	1	1	**DOUT31**	0	0	1	1	1	1	1
DIN32	0	1	0	0	0	0	0	**DOUT32**	0	1	0	0	0	0	0
DIN33	0	1	0	0	0	0	1	**DOUT33**	0	1	0	0	0	0	1
DIN34	0	1	0	0	0	1	0	**DOUT34**	0	1	0	0	0	1	0
DIN35	0	1	0	0	0	1	1	**DOUT35**	0	1	0	0	0	1	1
DIN36	0	1	0	0	1	0	0	**DOUT36**	0	1	0	0	1	0	0
DIN37	0	1	0	0	1	0	1	**DOUT37**	0	1	0	0	1	0	1
DIN38	0	1	0	0	1	1	0	**DOUT38**	0	1	0	0	1	1	0
DIN39	0	1	0	0	1	1	1	**DOUT39**	0	1	0	0	1	1	1
DIN40	0	1	0	1	0	0	0	**DOUT40**	0	1	0	1	0	0	0
DIN41	0	1	0	1	0	0	1	**DOUT41**	0	1	0	1	0	0	1
DIN42	0	1	0	1	0	1	0	**DOUT42**	0	1	0	1	0	1	0
DIN43	0	1	0	1	0	1	1	**DOUT43**	0	1	0	1	0	1	1
DIN44	0	1	0	1	1	0	0	**DOUT44**	0	1	0	1	1	0	0
DIN45	0	1	0	1	1	0	1	**DOUT45**	0	1	0	1	1	0	1
DIN46	0	1	0	1	1	1	0	**DOUT46**	0	1	0	1	1	1	0
DIN47	0	1	0	1	1	1	1	**DOUT47**	0	1	0	1	1	1	1
DIN48	0	1	1	0	0	0	0	**DOUT48**	0	1	1	0	0	0	0
DIN49	0	1	1	0	0	0	1	**DOUT49**	0	1	1	0	0	0	1
DIN50	0	1	1	0	0	1	0	**DOUT50**	0	1	1	0	0	1	0
DIN51	0	1	1	0	0	1	1	**DOUT51**	0	1	1	0	0	1	1
DIN52	0	1	1	0	1	0	0	**DOUT52**	0	1	1	0	1	0	0
DIN53	0	1	1	0	1	0	1	**DOUT53**	0	1	1	0	1	0	1
DIN54	0	1	1	0	1	1	0	**DOUT54**	0	1	1	0	1	1	0
DIN55	0	1	1	0	1	1	1	**DOUT55**	0	1	1	0	1	1	1
DIN56	0	1	1	1	0	0	0	**DOUT56**	0	1	1	1	0	0	0
DIN57	0	1	1	1	0	0	1	**DOUT57**	0	1	1	1	0	0	1
DIN58	0	1	1	1	0	1	0	**DOUT58**	0	1	1	1	0	1	0
DIN59	0	1	1	1	0	1	1	**DOUT59**	0	1	1	1	0	1	1
DIN60	0	1	1	1	1	0	0	**DOUT60**	0	1	1	1	1	0	0
DIN61	0	1	1	1	1	0	1	**DOUT61**	0	1	1	1	1	0	1
DIN62	0	1	1	1	1	1	0	**DOUT62**	0	1	1	1	1	1	0
DIN63	0	1	1	1	1	1	1	**DOUT63**	0	1	1	1	1	1	1
DIN64	1	0	0	0	0	0	0	**DOUT64**	1	0	0	0	0	0	0
DIN65	1	0	0	0	0	0	1	**DOUT65**	1	0	0	0	0	0	1
DIN66	1	0	0	0	0	1	0	**DOUT66**	1	0	0	0	0	1	0
DIN67	1	x	x	x	x	1	1	**DOUT67**	1	0	0	0	0	1	1
								DOUT68[2]	1	x	x	x	1	x	x

1. "x" denotes don't care.
2. Do not use '1xxx111' on OADDR[6:0], used for internal test.

Table 2. Swing Adjust Pin Settings for Outputs [0:31, 67, 68] (+3.3 V)

Output Setting #	VADJUST1	VADJUST2	VADJUST3	DOUTxx (mVpp Diff.)
1	O	T	O	380
2	T	T	O	550
3	O	O	T	715
4	T	O	T	870
5	O	T	T	1030
6	T	T	T	1180

Note: T = Tie VADJUSTx (x = 1,2,3) pin(s) to VCSHIGH1.
O = Open

Table 2A. Swing Adjust Pin Settings for Outputs [32:66] (+3.3 V)

Output Setting #	VADJUST4	VADJUST5	VADJUST6	DOUTxx (mVpp Diff.)
1	O	T	O	380
2	T	T	O	550
3	O	O	T	715
4	T	O	T	870
5	O	T	T	1030
6	T	T	T	1180

Note: T = Tie VADJUSTx (x = 4,5,6) pin(s) to VCSHIGH2.
O = Open

Table 3. Swing Adjust Pin Settings for Outputs [0:31, 67, 68] (+2.5 V)

Output Setting #	VADJUST1	VADJUST2	VADJUST3	DOUTxx (mVpp Diff.)
1	O	T	O	300
2	T	T	O	440
3	O	O	T	570
4	T	O	T	685
5	O	T	T	775
6	T	T	T	900

Note: T = Tie VADJUSTx (x = 1,2,3) pin(s) to VCSHIGH1.
O = Open

Table 3A. Swing Adjust Pin Settings for Outputs [32:66] (+2.5 V)

Output Setting #	VADJUST4	VADJUST5	VADJUST6	DOUTxx (mVpp Diff.)
1	O	T	O	300
2	T	T	O	440
3	O	O	T	570
4	T	O	T	685
5	O	T	T	775
6	T	T	T	900

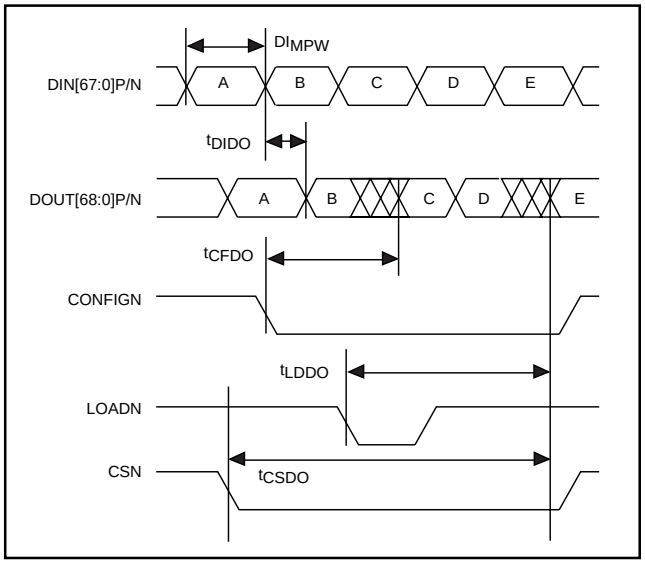
Note: T = Tie VADJUSTx (x = 4,5,6) pin(s) to VCSHIGH2.
O = Open

POWER DOWN OUTPUT ENABLE BIT

The S2090 has a power savings feature designed to have any number of outputs powered down through the use of an extra bit in the configuration and active registers. The extra bit is called Output Enable (OE) and it is programmed on every write to the configuration register. For example, by programming input 4 to output 10 with OE = 0, the configuration register will power down output 10 once the configuration register is transferred to the active register (CONFIGN Low). By programming input 4 to output 10 with OE = 1, the configuration register will enable output 10 once the configuration register is transferred to the active register. The timing of the OE signal will follow the exact timing of the IADDR[6:0] to LOADN (See Figure 4).The output enable bit allows the user to have flexibility in both the array size configuration and ease of system architecture design.

It is recommended that the S2090 reset line (RESETN) be held active during power up to reset the configuration and active registers. This will ensure that all of the output buffers are in the off state. The power dissipated by the S2090 will be at a minimum when the S2090 is powered on. After resetting the configuration and active registers, program the initial switch configuration into the configuration register, making sure OE = 1 for the output buffers to be enabled.

Figure 3. Data Transfer Waveforms

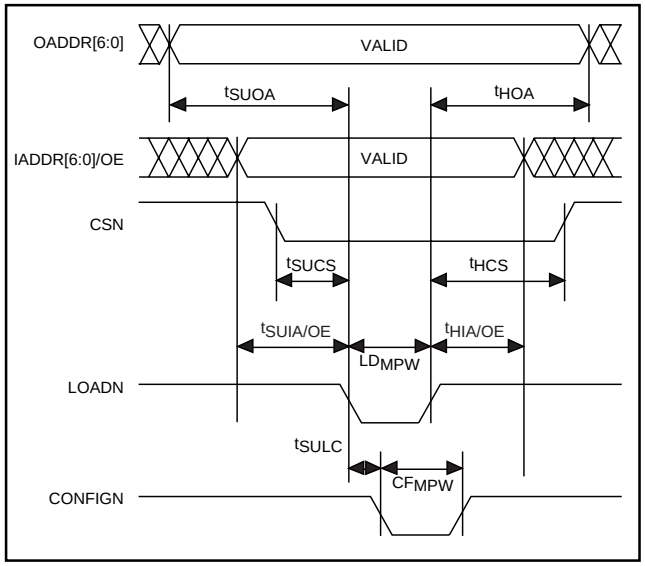


A simple way to use the output enable feature is to tie OE High, reset the part, then only configure the outputs that need to be enabled. When the S2090 is reset, the configuration and active registers are reset, which powers down all of the output buffers. Since OE is tied High, whenever an output is configured, the output will be enabled. For example, if a 68 x 34 configuration is desired, only configure outputs 0 to 33, so outputs 34:69 will remain off.

Enabling or disabling an output can produce a large on-chip transient that can cause excessive jitter on other outputs. Because of this, it is recommended that the outputs be enabled or disabled with a 1 µs delay between power downs or power ups during on-the-fly switching. This means that you can power up or down an output during normal operation as long as the 1 µs delay between enabling or disabling is followed. During system initialization, immediately after power up, the timing of IADDR[6:0]/OE is sufficient (see Figure 4).

The power dissipated for each output depends upon the programmed output amplitude. Table 19 (referenced to a +3.3 V power supply) or Table 20 (referenced to a +2.5 V power supply) describes the power savings for one output at each of the output amplitudes specified by VADJUSTx. The number of outputs powered down multiplied by the number stated in Table 19 or 20 will equal the total power savings.

Figure 4. Reconfiguration Waveforms



PARALLEL READ FUNCTION

The parallel read function allows the user to access stored data, either in the configuration register file or in the active configuration latch. This feature guarantees, prior to asserting CONFIGN Low (configuration register moved to active matrix), that the S2090 is configured to the user's satisfaction. The read function also serves as a checker to see if both the configuration register file and the active configuration latch are being programmed correctly by the software. The read function includes two pins, RDCFGN and RDACTN. RDCFGN selects the configuration register, while the RDACTN pin selects the active configuration latch. Also included is an eight-bit parallel bus, RDATA[7:0]. The data stored in either the configuration register file or the active configuration latch (determined by RDCFGN or RDACTN) will be read out on this bus. RDATA[7] is the power enable bit and RDATA[6:0] is the input address. As the RDCFGN or RDACTN is held Low (only one can be set Low at a time), an OADDR[6:0] must be applied to the device to read out the data that is being requested. When RDCFGN or RDACTN is Low, the IADDRs and OE are ignored, therefore no changes in the IADDRs or OE can occur in the latches. The S2090 can be read or written to, but read and writes can not occur at the same time. Simultaneous reads and writes are not allowed, so CONFIGN and LOADN must remain High while RDCFGN or RDACTN is Low. See Figure 9 for write-to-read and read-to-write waveforms. The parallel read data waveforms are shown in Figures 6 and 7. Figure 8 shows how to check multiple registers by switching OADDRs one after another and asserting RDCFGN or RDACTN Low during the cycling time.

USER NOTE (PARALLEL READ BACK)

This section of text can be ignored if not using the parallel read back feature. When operating the S2090 with a 2.5 V power supply, the drive capability of the RDATA[7:0] bits is not optimal. The parallel read back bits (RDATA[7:0]) have to be buffered to meet the Vih minimum limit of typical LVTTL or LVCMOS circuits. The Voh minimum presented on the RDATA[7:0] outputs is 1.8 V under worst-case conditions. A small 8-bit buffer can be used to resolve this issue. Texas Instruments has a small packaged buffer that will accept the reduced Voh limit from the RDATA[7:0] bits and increase the signal amplitude to provide the correct LVTTL or LVCMOS input limits, part number SN74LVC541A. There are an abundance of these types of buffers available from multiple vendors.

RESET BEHAVIOR

During a RESETN assertion, all the output drivers are powered down. The P and N side of the differential output signals will be pulled up to V_{CC}. The IC will not pass data through the matrix until the inputs and outputs are explicitly reconfigured to be enabled and powered up using the OE signal.

POWER UP

Upon power up, the crosspoint will default to full broadcast mode (DINxx to all the outputs, DOUT0 through DOUT68). DINxx is determined by the state of the bits on IADDR[6:0] at the moment the device is powered up. The OADDR[6:0] and OE bits will not have any affect on the configuration of the switch at power up. The IC will remain in full broadcast mode until the inputs and outputs are explicitly reconfigured to be enabled.

Figure 5. S2090 Configuration Flow Chart

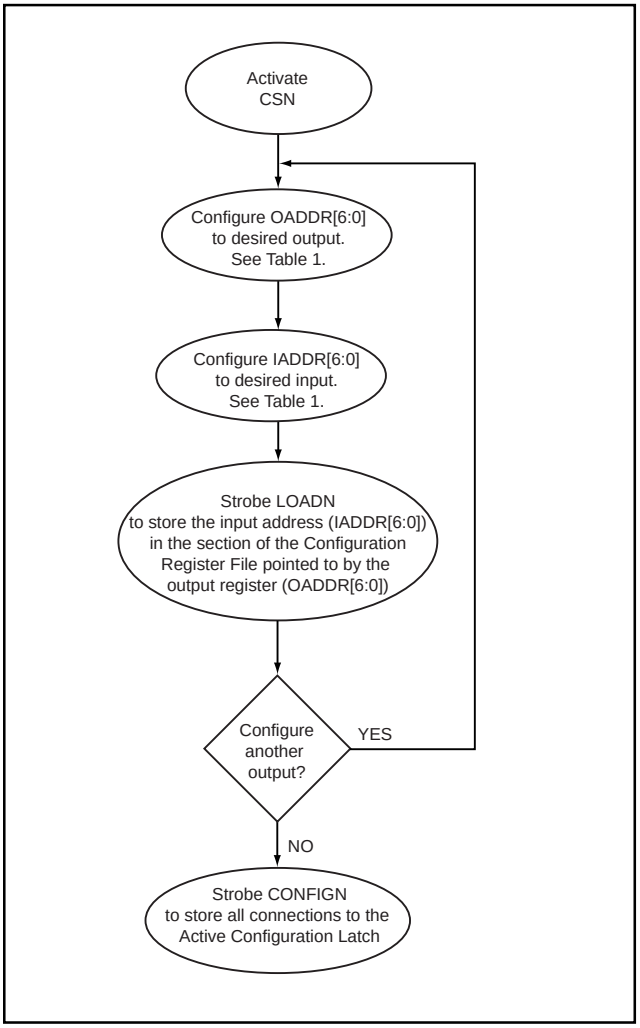
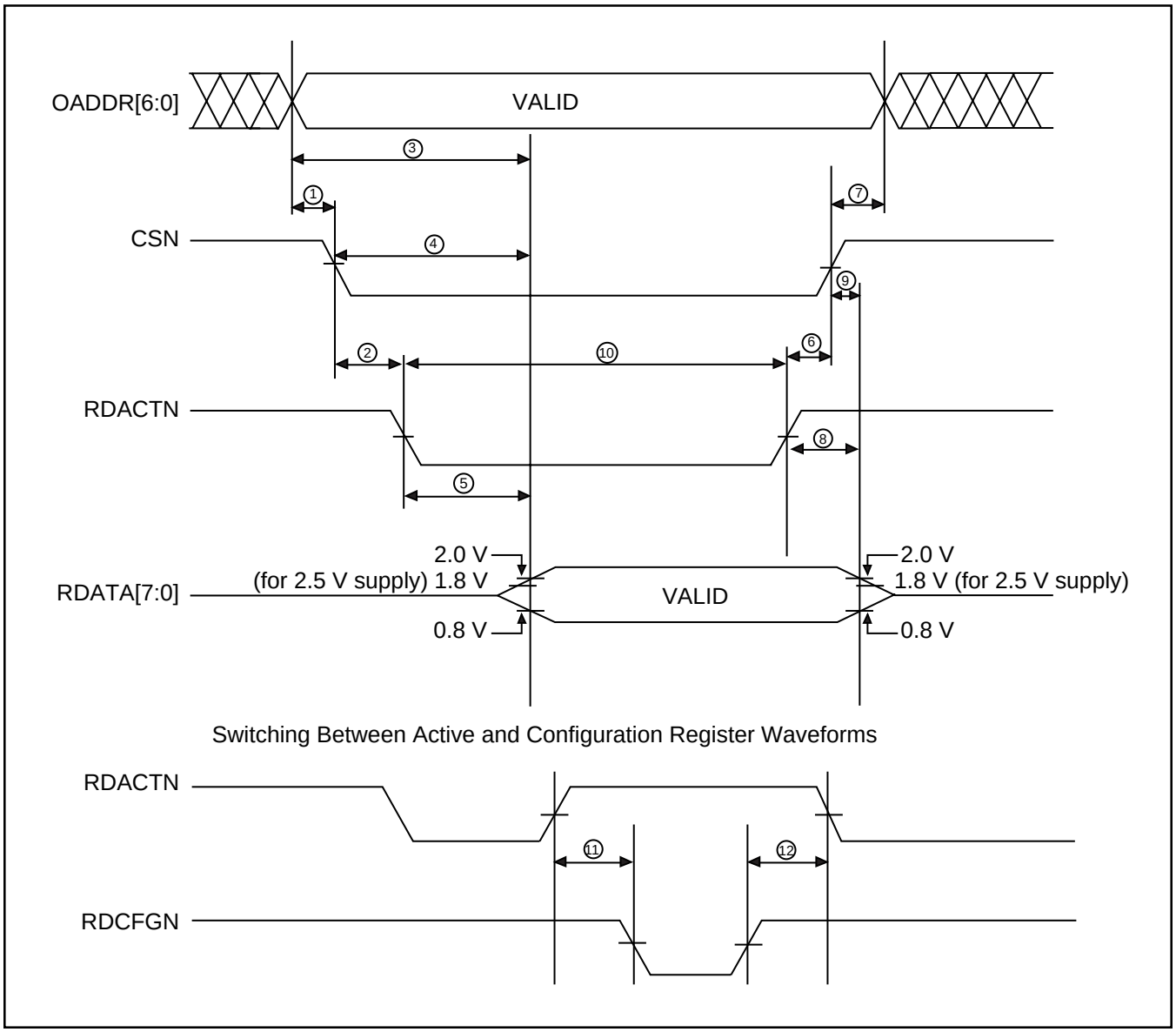
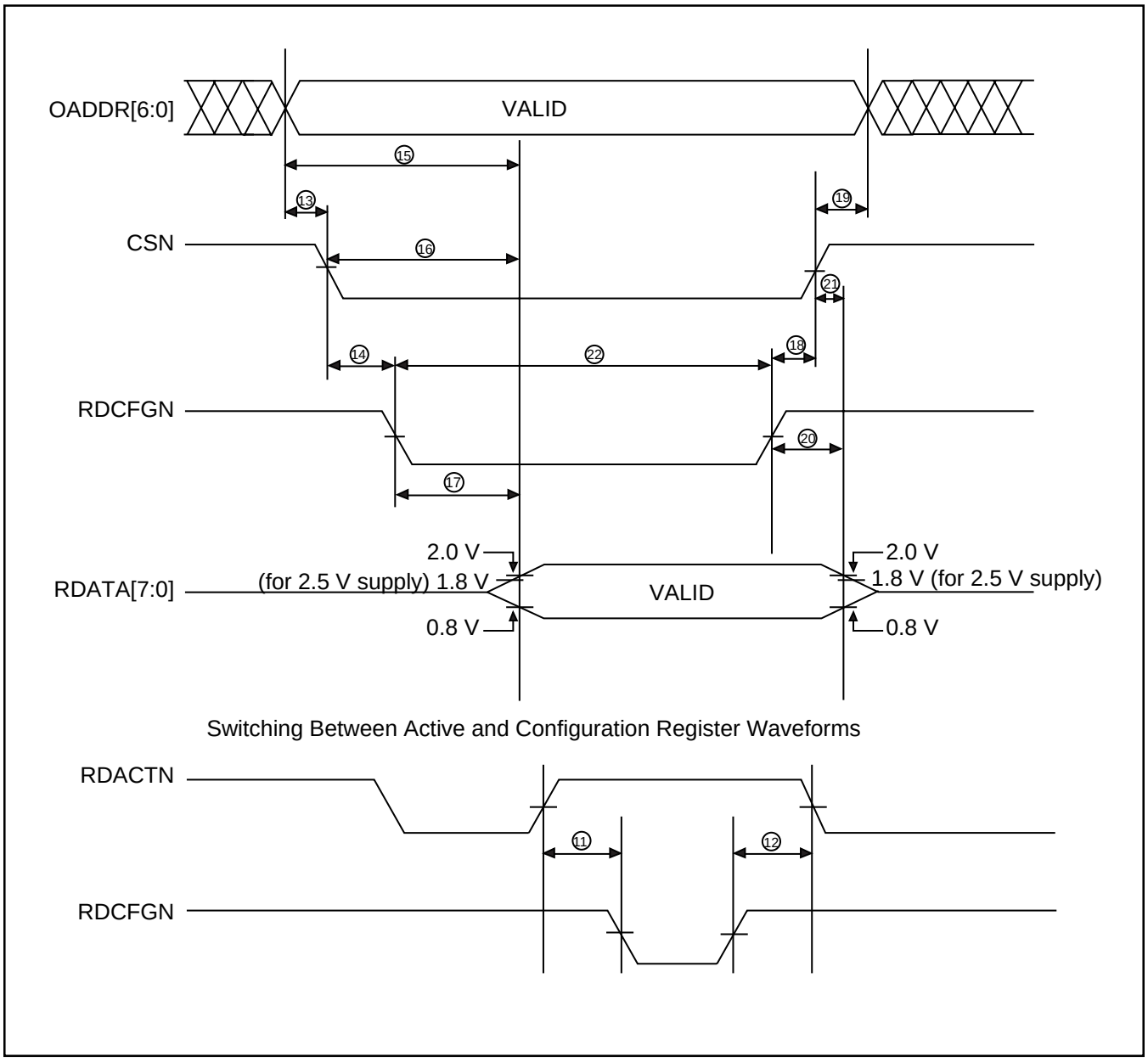


Figure 6. Parallel Read Waveforms (RDACTN)



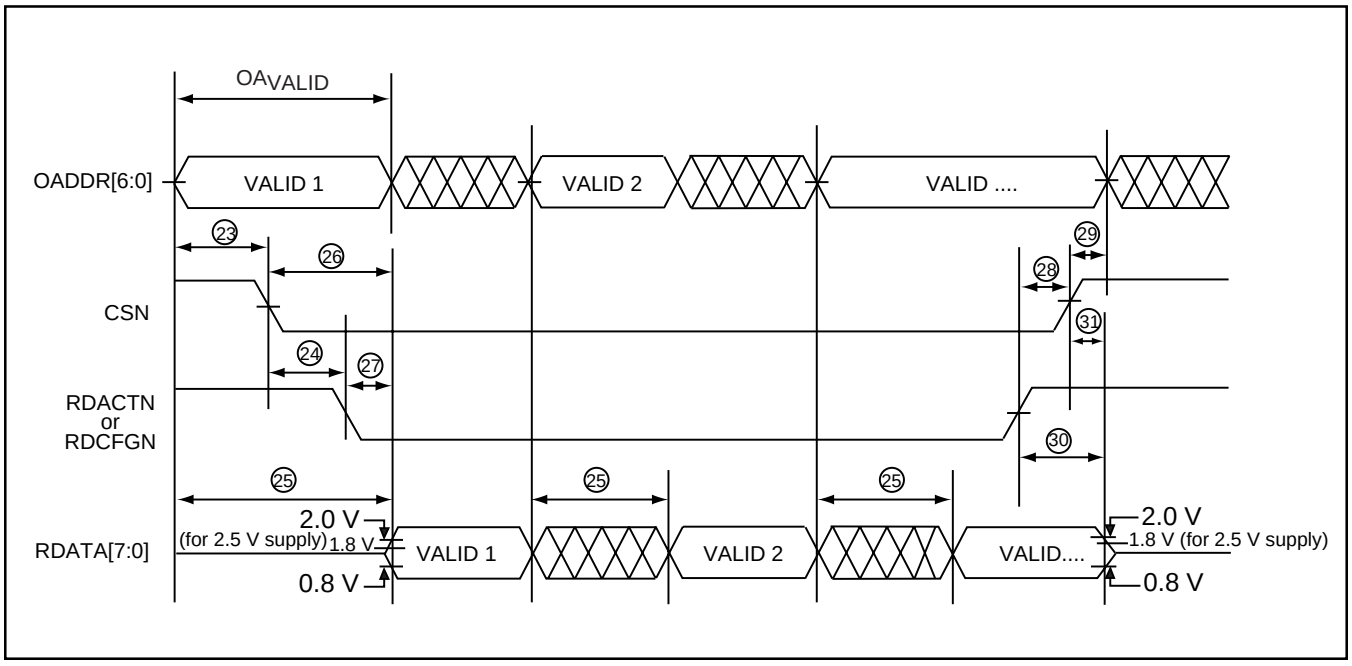
Notes:
1. RDCFGN and RDACTN cannot be Low at the same time.
2. When CSN is inactive or RDCFGN/RDACTN are both inactive, the RDATA[7:0] bus will remain tri-stated.

Figure 7. Parallel Read Waveforms (RDCFGN)



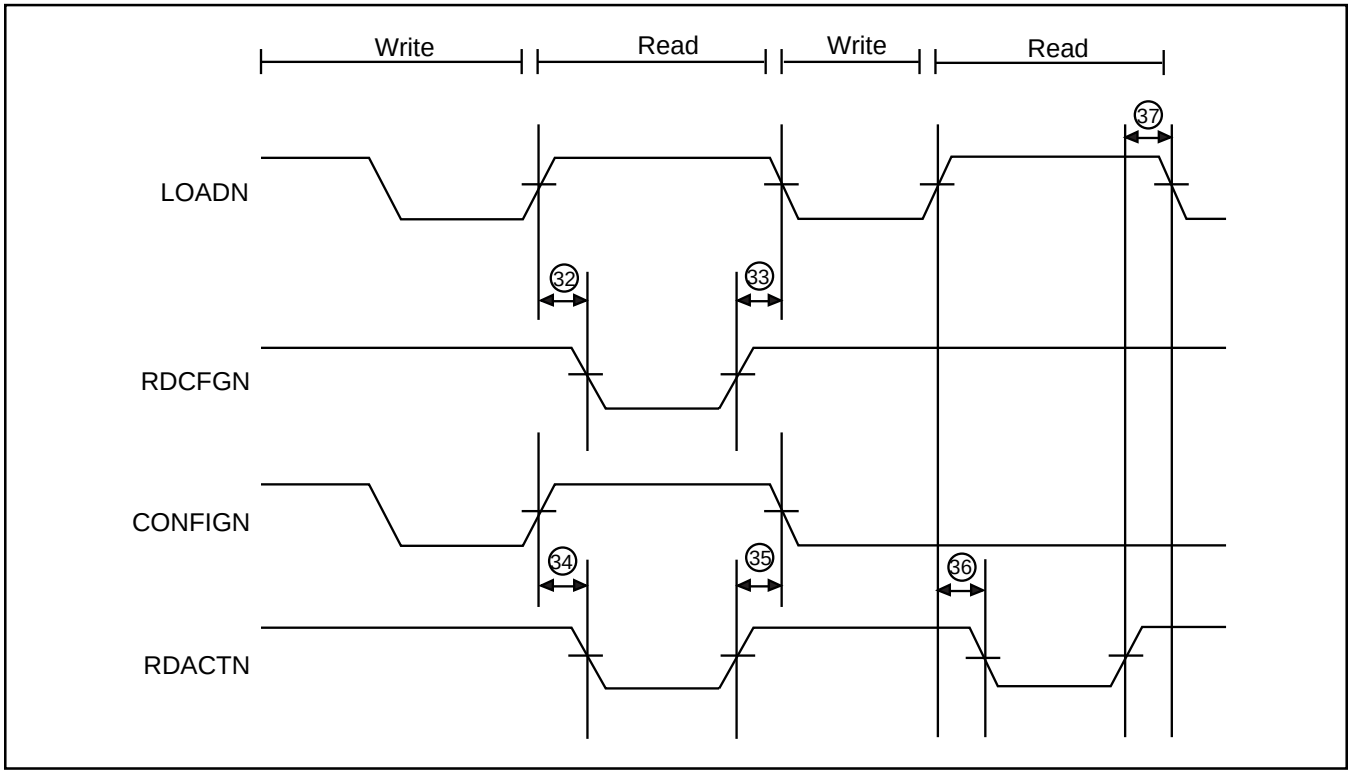
Notes:
1. RDCFGN and RDACTN cannot be Low at the same time.
2. When CSN is inactive or RDCFGN/RDACTN are both inactive, the RDATA[7:0] bus will remain tri-stated.

Figure 8. Parallel Read Waveforms Cycling Through Multiple OADDRs



Notes:
1. RDCFGN and RDACTN cannot be Low at the same time.
2. When CSN is inactive or RDCFGN/RDACTN are both inactive, the RDATA[7:0] bus will remain tri-stated.

Figure 9. Write-to-Read, Read-to-Write Timing



Notes:
1. RDCFGN and RDACTN cannot be Low at the same time.
2. When CSN is inactive or RDCFGN/RDACTN are both inactive, the RDATA[7:0] bus will remain tri-stated.

Table 4. Data Transfer Timing[1,2,3] (+3.3 V supply)

Parameter	Description	Min	Typ	Max	Units	Conditions
t_{DIDO}	Propagation delay from DIN[67:0]P/N to DOUT[68:0]P/N			2.5	ns	
t_{CFDO}	Propagation delay from falling edge of CONFIGN to DOUT[68:0]P/N valid			11	ns	
t_{LDDO}	Propagation delay from falling edge of LOADN to DOUT[68:0]P/N valid (when CONFIGN is held Low)			11	ns	
T_{CSDO}	Propagation delay from falling edge of CSN to DOUT[68:0]P/N valid (when CONFIGN is held Low)			13.5	ns	
F_{MAX}	Data Rate			3.2	Gbps	
T_{JITTER} RMS	Random jitter accumulation, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 1.9 1.9 2.0 2.0	 3.2 3.2 3.2 3.2	 ps ps ps ps	RMS output jitter accumulated with K28.7 code. Tested on a sample basis.
T_{JITTER} DJ	Deterministic jitter accumulation, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 18 18 18 18	 28 28 28 30	 ps ps ps ps	Deterministic output jitter accumulated with K28.5 pattern. Tested on a sample basis. Peak-to-peak.
T_{JITTER} CTK	Deterministic jitter accumulation due to crosstalk, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 2 2 2 4	 4 4 4 6	 ps ps ps ps	Deterministic output jitter accumulated with K28.5 pattern. Tested on a sample basis. Peak-to-peak.
$Skew_{XPT}$	Skew from output to output. Any inputs to any outputs.			140	ps	
$T_{r(out)}$, $T_{f(out)}$	Output Edge Rate (20% to 80%)			120	ps	100 Ω line-to-line.

1. All data transfer timing measured from the crossing point of the differential inputs to the crossing point of the differential outputs.
2. All LVTTL signals measured at the 1.5 V point.
3. All data measured with output setting #3.

Table 5. Reconfiguration Timing[1] (+3.3 V supply)

Parameter	Description	Min	Typ	Max	Units
$t_{SUIA/OE}$	Setup time of IADDR[6:0] and OE before falling edge of LOADN	1			ns
$t_{HIA/OE}$	Hold time of IADDR[6:0] and OE after rising edge of LOADN	4			ns
t_{SUOA}	Setup time of OADDR[6:0] before falling edge of LOADN	2.5			ns
t_{HOA}	Hold time of OADDR[6:0] after rising edge of LOADN	2.5			ns
t_{SULC}	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration	2.5			ns
t_{SUCS}	Setup time of CSN before falling edge of LOADN	2			ns
t_{HCS}	Hold time of CSN after rising edge of LOADN	4			ns
LD_{MPW}	Pulse width Low of LOADN	4			ns
CF_{MPW}	Pulse width Low of CONFIGN	4			ns
$RESETN_{MPW}$	Pulse width Low of RESETN	5			ns
F_{MAX}	LOAD, CONFIGN			100	MHz

1. All reconfiguration timing measured at the 1.5 V point on the LVTTL signals.

Table 6. Data Transfer Timing[1,2,3] (+2.5 V supply)

Parameter	Description	Min	Typ	Max	Units	Conditions
t_{DIDO}	Propagation delay from DIN[67:0]P/N to DOUT[68:0]P/N			2.5	ns	
t_{CFDO}	Propagation delay from falling edge of CONFIGN to DOUT[68:0]P/N valid			11	ns	
t_{LDDO}	Propagation delay from falling edge of LOADN to DOUT[68:0]P/N valid (when CONFIGN is held Low)			11	ns	
t_{CSDO}	Propagation delay from falling edge of CSN to DOUT[68:0]P/N valid (when CONFIGN is held Low)			13.5	ns	
F_{MAX}	Data Rate			3.2	Gbps	
T_{JITTER} RMS	Random Jitter accumulation, any input to any output at : 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 1.9 1.9 2.0 2.0	 3.0 3.0 3.0 3.0	 ps ps ps ps	RMS output jitter accumulated with K28.7 code. Tested on a sample basis.
T_{JITTER} DJ	Deterministic Jitter accumulation, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 19 19 19 19	 35 35 35 35	 ps ps ps ps	Deterministic output jitter accumulated with K28.5 code. Tested on a sample basis. Peak-to-peak.
T_{JITTER} CTK	Deterministic Jitter accumulation due to crosstalk, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 2 2 2 3	 4 4 4 5	 ps ps ps ps	Deterministic output jitter accumulated with K28.5 code. Tested on a sample basis. Peak-to-peak.
$Skew_{XPT}$	Skew from output to output. Any inputs to any outputs.			145	ps	
$T_{r(out)}$, $T_{f(out)}$	Output Edge Rate (20% to 80%)			135	ps	100 Ω line-to-line.

1. All data transfer timing measured from the crossing point of the differential inputs to the crossing point of the differential outputs.
2. All LVTTL signals measured at the 1.5 V point.
3. All data measured with output setting #3.

Table 7. Reconfiguration Timing[1] (+2.5 V supply)

Parameter	Description	Min	Typ	Max	Units
$t_{SUIA/OE}$	Setup time of IADDR[6:0] and OE before falling edge of LOADN	1			ns
$t_{HIA/OE}$	Hold time of IADDR[6:0] and OE after rising edge of LOADN	4			ns
t_{SUOA}	Setup time of OADDR[6:0] before falling edge of LOADN	2.5			ns
t_{HOA}	Hold time of OADDR[6:0] after rising edge of LOADN	2.5			ns
t_{SULC}	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration	2.5			ns
t_{SUCS}	Setup time of CSN before falling edge of LOADN	2			ns
t_{HCS}	Hold time of CSN after rising edge of LOADN	4			ns
LD_{MPW}	Pulse width Low of LOADN	4			ns
CF_{MPW}	Pulse width Low of CONFIGN	4			ns
$RESETN_{MPW}$	Pulse width Low of RESETN	5			ns
F_{MAX}	LOAD, CONFIGN			100	MHz

1. All reconfiguration timing measured at the 1.5 V point on the LVTTL signals.

Table 8. Parallel Read Timing (RDACTN)[1, 2, 3] (Figure 6) (+3.3 V or +2.5 V supply)

Number	Description	Min	Typ	Max	Units
1	Setup time of OADDR[6:0] before falling edge of CSN	6			ns
2	Setup time from CSN falling edge to falling edge of RDACTN	2			ns
3	OADDR[6:0] valid to RDATA[7:0] valid (when RDACTN, CSN are held Low)			20	ns
4	CSN falling edge to RDATA[7:0] valid (when RDACTN is held Low)			10	ns
5	RDACTN falling edge to RDATA[7:0] valid (when CSN is held Low)			10	ns
6	Hold time of CSN after rising edge of RDACTN	2			ns
7	Hold time of OADDR[6:0] after rising edge of CSN	0			ns
8	RDACTN rising edge to RDATA[7:0] invalid			15	ns
9	CSN rising edge to RDATA[7:0] invalid			15	ns
10	Pulse width Low of RDACTN	50			ns
11	RDACTN rising edge (inactive) to RDCFGN falling edge (active)	20			ns
12	RDCFGN rising edge (inactive) to RDACTN falling edge (active)	20			ns

1. All parallel read timing measured at the 1.5 V point on the LVTTL signals where specified.
2. All input control signals are measured from the 1.5 V point to the RDATA level (0.8 or 2.0 V). With +2.5 V power supply, RDATA level (0.8 V or 1.8 V).
3. When CSN is inactive or RDCFGN/RDACTN are both inactive, the RDATA[7:0] bus will remain tri-stated.

Table 9. Parallel Read Timing (RDCFGN)[1, 2, 3] (Figure 7) (+3.3 V or +2.5 V supply)

Number	Description	Min	Typ	Max	Units
13	Setup time of OADDR[6:0] before falling edge of CSN	6			ns
14	Setup time from CSN falling edge to falling edge of RDCFGN	2			ns
15	OADDR[6:0] valid to RDATA[7:0] valid (when RDCFGN, CSN are held Low)			20	ns
16	CSN falling edge to RDATA[7:0] valid (when RDCFGN is held Low)			10	ns
17	RDCFGN falling edge to RDATA[7:0] valid (when CSN is held Low)			10	ns
18	Hold time of CSN after rising edge of RDCFGN	2			ns
19	Hold time of OADDR[6:0] after rising edge of CSN	0			ns
20	RDCFGN rising edge to RDATA[7:0] invalid			15	ns
21	CSN rising edge to RDATA[7:0] invalid			15	ns
22	Pulse width Low of RDCFGN	50			ns

1. All parallel read timing measured at the 1.5 V point on the LVTTL signals where specified.
2. All input control signals are measured from the 1.5 V point to the RDATA level (0.8 or 2.0 V). With +2.5 V power supply, RDATA level (0.8 V or 1.8 V).
3. When CSN is inactive or RDCFGN/RDACTN are both inactive, the RDATA[7:0] bus will remain tri-stated.

Table 10. Parallel Read Timing Cycling Through Multiple OADDRs[1, 2, 3] (Figure 8) (+3.3 V or +2.5 V supply)

Number	Description	Min	Typ	Max	Units
23	Setup time of OADDR[6:0] before falling edge of CSN	6			ns
24	Setup time from CSN falling edge to RDACTN or RDCFGN falling edge	2			ns
25	OADDR[6:0] valid to RDATA[7:0] valid (when RDACTN or RDCFGN and CSN are held Low)			20	ns
26	CSN falling edge to RDATA[7:0] valid			10	ns
27	RDACTN or RDCFGN falling edge to RDATA[7:0] valid			10	ns
28	Hold time of CSN after rising edge of RDACTN or RDCFGN	2			ns
29	Hold time of OADDR[6:0] after rising edge of CSN	0			ns
30	RDACTN or RDCFGN rising edge to RDATA[7:0] invalid			15	ns
31	CSN rising edge to RDATA[7:0] invalid			15	ns
OA_{VALID}	Hold OADDR[6:0] valid	50			ns

1. All parallel read timing measured at the 1.5 V point on the LVTTL signals where specified.
2. All input control signals are measured from the 1.5 V point to the RDATA level (0.8 or 2.0 V). With +2.5 V power supply, RDATA level (0.8 V or 1.8 V).
3. When CSN is inactive or RDCFGN/RDACTN are both inactive, the RDATA[7:0] bus will remain tri-stated.

Table 11. Write-to-Read, Read-to-Write Timing[1,2] (Figure 9) (+3.3 V or +2.5 V supply)

Number	Description	Min	Typ	Max	Units
32	LOADN rising edge to RDCFGN falling edge	5			ns
33	RDCFGN rising edge to LOADN falling edge	5			ns
34	CONFIGN rising edge to RDACTN falling edge	5			ns
35	RDACTN rising edge to CONFIGN falling edge	5			ns
36	LOADN rising edge to RDACTN falling edge (CONFIGN held low)	20			ns
37	RDACTN rising edge to LOADN falling edge	5			ns

1. All parallel read timing measured at the 1.5 V point on the LVTTL signals.
2. CSN must be Low.

Table 12. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DIN67P DIN67N DIN66P DIN66N DIN65P DIN65N DIN64P DIN64N DIN63P DIN63N DIN62P DIN62N DIN61P DIN61N DIN60P DIN60N DIN59P DIN59N DIN58P DIN58N DIN57P DIN57N DIN56P DIN56N DIN55P DIN55N DIN54P DIN54N DIN53P DIN53N DIN52P DIN52N DIN51P DIN51N DIN50P DIN50N DIN49P DIN49N DIN48P DIN48N DIN47P DIN47N DIN46P DIN46N DIN45P DIN45N DIN44P DIN44N DIN43P DIN43N DIN42P DIN42N DIN41P DIN41N DIN40P DIN40N	Diff. LVPECL	I	P4 P5 N2 N3 N5 N6 M1 M2 M4 M5 L2 L3 L5 L6 K1 K2 K4 K5 J2 J3 J5 J6 H1 H2 H4 H5 G2 G3 G5 G6 F1 F2 F4 F5 E2 E3 D1 D2 B3 C3 A4 B4 B5 C5 A6 B6 D6 E6 B7 C7 E7 F7 A8 B8 D8 E8	Input data. Differential. Internally biased and terminated with 100 Ω line to line.

Table 12. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DIN39P DIN39N DIN38P DIN38N DIN37P DIN37N DIN36P DIN36N DIN35P DIN35N DIN34P DIN34N DIN33P DIN33N DIN32P DIN32N DIN31P DIN31N DIN30P DIN30N DIN29P DIN29N DIN28P DIN28N DIN27P DIN27N DIN26P DIN26N DIN25P DIN25N DIN24P DIN24N DIN23P DIN23N DIN22P DIN22N DIN21P DIN21N DIN20P DIN20N DIN19P DIN19N DIN18P DIN18N DIN17P DIN17N DIN16P DIN16N DIN15P DIN15N DIN14P DIN14N DIN13P DIN13N DIN12P DIN12N DIN11P DIN11N	Diff. LVPECL		B9 C9 E9 F9 A10 B10 D10 E10 B11 C11 E11 F11 A12 B12 D12 E12 AE12 AD12 AB12 AA12 AD11 AC11 AA11 Y11 AE10 AD10 AB10 AA10 AD9 AC9 AA9 Y9 AE8 AD8 AB8 AA8 AD7 AC7 AA7 Y7 AE6 AD6 AB6 AA6 AD5 AC5 AE4 AD4 AD3 AC3 AB1 AB2 AA2 AA3 Y1 Y2 Y4 Y5	Input data. Differential. Internally biased and terminated with 100 Ω line to line.

Table 12. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DIN10P DIN10N DIN9P DIN9N DIN8P DIN8N DIN7P DIN7N DIN6P DIN6N DIN5P DIN5N DIN4P DIN4N DIN3P DIN3N DIN2P DIN2N DIN1P DIN1N DIN0P DIN0N	Diff. LVPECL	I	W2 W3 W5 W6 V1 V2 V4 V5 U2 U3 U5 U6 T1 T2 T4 T5 R2 R3 R5 R6 P1 P2	Input data. Differential. Internally biased and terminated with 100 Ω line to line.
OADDR6 OADDR5 OADDR4 OADDR3 OADDR2 OADDR1 OADDR0	LVTTL	I	M10 M9 M8 L11 L10 L9 L8	Output Address. Used to select an output configuration register in the configuration register file. See Table 1.
IADDR6 IADDR5 IADDR4 IADDR3 IADDR2 IADDR1 IADDR0	LVTTL	I	R10 R9 R8 P11 P10 P9 P8	Input Address. IADDR[6:0] selects the input pair to connect to the output pair selected by OADDR[6:0]. See Table 1.
LOADN	LVTTL	I	H9	Load strobe. Active Low. When active, stores the configuration data in IADDR[6:0] into the configuration register file.
CONFIGN	LVTTL	I	H10	Configuration strobe. Active Low. When active, parallel loads the contents of the configuration register file into the active configuration latch.
CSN	LVTTL	I	H8	Chip Select. Active Low. When inactive, the LOADN, CONFIGN, RDCFGN, and RDACTN signals will be ignored. New addresses, configurations, or parallel read backs will not be allowed. When active, the S2090 will operate as specified.

Table 12. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
RESETN	LVTTL	I	J10	Reset. Active Low. Clears the active configuration file of existing data and the configuration register file retains its configuration information. The output drivers are also powered down and need to be enabled for data to be seen on the outputs after a reset. The default configuration will be broadcast on the active configuration file. The configuration register file is not affected by reset.
OE	LVTTL	I	R11	Power Down Output Enable. Active High. When active and loaded into a specified output latch, this signal will allow the output driver of the specified output to become active after it has been passed to the active matrix via the CONFIGN signal. Following the above procedures, when inactive, the output driver of the specified output is powered down.
RDCFGN	LVTTL	I	J8	Read Configuration Register File. Active Low. When active, the user specifies an OADDR[6:0] to the device, which in turn, allows a read back of the data stored in the configuration register file. The data will appear on the RDATA[7:0] bus. RDCFGN and RDACTN cannot be asserted Low at the same time. The device does not allow read/writes to occur simultaneously.
RDACTN	LVTTL	I	J9	Read Active Configuration Latch. Active Low. When active, the user specifies an OADDR[6:0], which in turn, allows a read back of the data stored in the active configuration latch. The data will appear on the RDATA [7:0] bus. RDACTN and RDCFGN cannot be asserted Low at the same time. The device does not allow read/writes to occur simultaneously.
RDATA7 RDATA6 RDATA5 RDATA4 RDATA3 RDATA2 RDATA1 RDATA0	LVTTL	O	V11 V10 V9 V8 U11 U10 U9 U8	Read Data Outputs. This parallel data bus allows the stored data in either the configuration register file or the active configuration latch to be read. RDATA[7] is the power down enable bit, while RDATA[6:0] is the input address, IADDR[6:0].
VCSHIGH1		I	P17	Output Voltage Swing Adjust 1. Tied to VADJUSTx (x = 1,2,3) pin(s) to set the output voltage swing. VADJUST 1,2,3 sets the amplitude of outputs [0:31,67,68]. See Tables 2, 2A and 3, 3A for details.
VADJUST1 VADJUST2 VADJUST3	LVTTL	O	R18 P18 N18	Voltage Adjust. These three pins, selectively tied to VCSHIGH1, create a coded input which sets the output voltage swing. Tables 2, 2A and 3, 3A describe the settings for adjustable output swings at different power supplies.
VCSHIGH2		O	L17	Output Voltage Swing Adjust 2. Tied to VADJUSTx (x = 4,5,6) pin(s) to set the output voltage swing. VADJUST 4,5,6 sets the amplitude of outputs [32:66]. See Tables 2, 2A and 3, 3A for details.
VADJUST4 VADJUST5 VADJUST6	LVTTL	I	M18 L18 K18	Voltage Adjust. These three pins, selectively tied to VCSHIGH2, create a coded input which sets the output voltage swing. Tables 2, 2A and 3, 3A describe the settings for adjustable output swing at different power supplies.

Table 12. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DOUT68P	Diff. CML	O	P22	Output data. Differential.
DOUT68N			P21	
DOUT67P			N24	
DOUT67N			N23	
DOUT66P			N21	
DOUT66N			N20	
DOUT65P			M25	
DOUT65N			M24	
DOUT64P			M22	
DOUT64N			M21	
DOUT63P			L24	
DOUT63N			L23	
DOUT62P			L21	
DOUT62N			L20	
DOUT61P			K25	
DOUT61N			K24	
DOUT60P			K22	
DOUT60N			K21	
DOUT59P			J24	
DOUT59N			J23	
DOUT58P			J21	
DOUT58N			J20	
DOUT57P			H25	
DOUT57N			H24	
DOUT56P			H22	
DOUT56N			H21	
DOUT55P			G24	
DOUT55N			G23	
DOUT54P			G21	
DOUT54N			G20	
DOUT53P			F25	
DOUT53N			F24	
DOUT52P			F22	
DOUT52N			F21	
DOUT51P			E24	
DOUT51N			E23	
DOUT50P			D25	
DOUT50N			D24	
DOUT49P			B23	
DOUT49N			C23	
DOUT48P			A22	
DOUT48N			B22	
DOUT47P			B21	
DOUT47N			C21	
DOUT46P			A20	
DOUT46N			B20	
DOUT45P			D20	
DOUT45N			E20	
DOUT44P			B19	
DOUT44N			C19	
DOUT43P			E19	
DOUT43N			F19	
DOUT42P			A18	
DOUT42N			B18	
DOUT41P			D18	
DOUT41N			E18	
DOUT40P			B17	
DOUT40N			C17	

Table 12. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DOUT39P	Diff. CML	O	E17	Output data. Differential.
DOUT39N			F17	
DOUT38P			A16	
DOUT38N			B16	
DOUT37P			D16	
DOUT37N			E16	
DOUT36P			B15	
DOUT36N			C15	
DOUT35P			E15	
DOUT35N			F15	
DOUT34P			A14	
DOUT34N			B14	
DOUT33P			D14	
DOUT33N			E14	
DOUT32P			F13	
DOUT32N			G13	
DOUT31P			AE14	
DOUT31N			AD14	
DOUT30P			AB14	
DOUT30N			AA14	
DOUT29P			AD15	
DOUT29N			AC15	
DOUT28P			AA15	
DOUT28N			Y15	
DOUT27P			AE16	
DOUT27N			AD16	
DOUT26P			AB16	
DOUT26N			AA16	
DOUT25P			AD17	
DOUT25N			AC17	
DOUT24P			AA17	
DOUT24N			Y17	
DOUT23P			AE18	
DOUT23N			AD18	
DOUT22P			AB18	
DOUT22N			AA18	
DOUT21P			AD19	
DOUT21N			AC19	
DOUT20P			AA19	
DOUT20N			Y19	
DOUT19P			AE20	
DOUT19N			AD20	
DOUT18P			AB20	
DOUT18N			AA20	
DOUT17P			AD21	
DOUT17N			AC21	
DOUT16P			AE22	
DOUT16N			AD22	
DOUT15P			AD23	
DOUT15N			AC23	
DOUT14P			AB25	
DOUT14N			AB24	
DOUT13P			AA24	
DOUT13N			AA23	
DOUT12P			Y25	
DOUT12N			Y24	

Table 12. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DOUT11P	Diff. CML	O	Y22	Output data. Differential.
DOUT11N			Y21	
DOUT10P			W24	
DOUT10N			W23	
DOUT9P			W21	
DOUT9N			W20	
DOUT8P			V25	
DOUT8N			V24	
DOUT7P			V22	
DOUT7N			V21	
DOUT6P			U24	
DOUT6N			U23	
DOUT5P			U21	
DOUT5N			U20	
DOUT4P			T25	
DOUT4N			T24	
DOUT3P			T22	
DOUT3N			T21	
DOUT2P			R24	
DOUT2N			R23	
DOUT1P			R21	
DOUT1N			R20	
DOUT0P			P25	
DOUT0N			P24	

Table 13. Power and Ground Signals

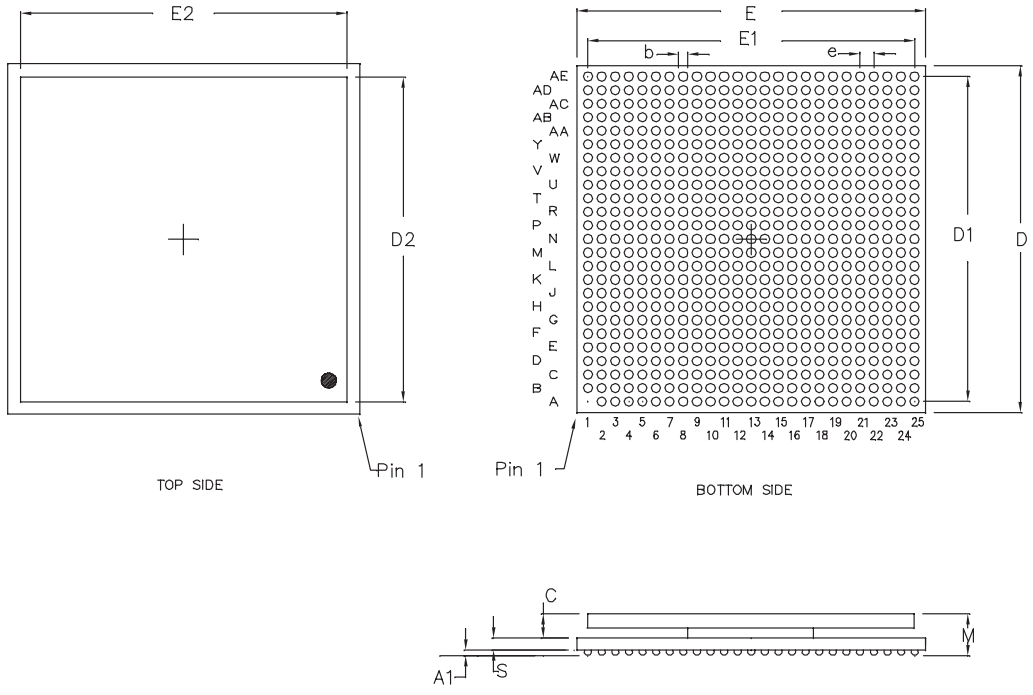
Pin Name	Qty.	Pin #	Description
VCCINPUT	76	B2, C1, C4, C6, C8, C10, C12, C13, D3, E5, F3, F6, F8, F10, F12, H3, H6, H16, H18, J13, J14, J15, J16, J17, K3, K6, K13, K14, K15, K16, K17, M3, M6, M13, M14, M15, M16, M17, P3, P6, P13, P14, P15, P16, T3, T6, T13, T14, T15, T16, T17, U13, U14, U15, U16, U17, V3, V6, V14, V16, V18, Y3, Y6, Y8, Y10, Y12, Y13, AA5, AB3, AC1, AC4, AC6, AC8, AC10, AC12, AD2	+3.3 V or +2.5 V Power supply. Power supply for high-speed circuitry inputs.
GNDINPUT	88	A3, A5, A7, A9, A11, A13, C2, D4, D5, D7, D9, D11, D13, E1, E4, G1, G4, G7, G9, G11, G16, G18, H15, H17, H19, J1, J4, J7, J18, K19, L1, L4, L7, L13, L14, L15, L16, M19, N1, N4, N7, N13, N14, N15, N16, N17, P19, R1, R4, R7, R13, R14, R15, R16, R17, T18, T19, U1, U4, U7, U18, V13, V15, V17, V19, W1, W4, W7, W9, W11, W14, W16, W18, AA1, AA4, AB4, AB5, AB7, AB9, AB11, AB13, AC2, AE3, AE5, AE7, AE9, AE11, AE13	Ground for high-speed circuitry inputs.
VCCOUTPUT	43	B24, C14, C16, C18, C20, C22, C25, D23, E21, F14, F16, F18, F20, F23, G12, H14, H20, H23, K20, K23, M20, M23, P20, P23, T20, T23, V20, V23, Y14, Y16, Y18, Y20, Y23, AA21, AB23, AC13, AC14, AC16, AC18, AC20, AC22, AC25, AD24	+3.3 V or +2.5 V Power supply. Power supply for high-speed circuitry outputs.
GNDOUTPUT	59	A15, A17, A19, A21, A23, B13, C24, D15, D17, D19, D21, D22, E13, E22, E25, G14, G15, G17, G19, G22, G25, H12, H13, J19, J22, J25, L19, L22, L25, N19, N22, N25, R19, R22, R25, U19, U22, U25, W13, W15, W17, W19, W22, W25, AA13, AA22, AA25, AB15, AB17, AB19, AB21, AB22, AC24, AD13, AE15, AE17, AE19, AE21, AE23	Ground for high-speed circuitry outputs.
VCCTTL	13	H11, J11, K8, K10, K12, M11, N8, N10, N12, T8, T10, T12, V12	+3.3 V or +2.5 V Power supply. Power for LVTTL I/O.
GNDTTL	23	G8, G10, H7, J12, K7, K9, K11, L12, M7, M12, N9, N11, P7, P12, R12, T7, T9, T11, U12, V7, W8, W10, W12	Ground for LVTTL I/O.

Figure 10. S2090 Pinout (Top View) (Note: A1 is located at bottom right corner)

	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AE			GND OUTPUT	DOUT16P	GND OUTPUT	DOUT19P	GND OUTPUT	DOUT23P	GND OUTPUT	DOUT27P	GND OUTPUT	DOUT31P	GNDINPUT	DIN31P	GNDINPUT	DIN27P	GNDINPUT	DIN23P	GNDINPUT	DIN19P	GNDINPUT	DIN16P	GNDINPUT		
AD		VCC OUTPUT	DOUT15P	DOUT16N	DOUT17P	DOUT19N	DOUT21P	DOUT23N	DOUT25P	DOUT27N	DOUT29P	DOUT31N	GND OUTPUT	DIN31N	DIN29P	DIN27N	DIN25P	DIN23N	DIN21P	DIN19N	DIN17P	DIN16N	DIN15P	VCCINPUT	
AC	VCC OUTPUT	GND OUTPUT	DOUT15N	VCC OUTPUT	DOUT17N	VCC OUTPUT	DOUT21N	VCC OUTPUT	DOUT25N	VCC OUTPUT	DOUT29N	VCC OUTPUT	VCC OUTPUT	VCCINPUT	DIN29N	VCCINPUT	DIN25N	VCCINPUT	DIN21N	VCCINPUT	DIN17N	VCCINPUT	DIN15N	GNDINPUT	VCCINPUT
AB	DOUT14P	DOUT14N	VCC OUTPUT	GND OUTPUT	GND OUTPUT	DOUT18P	GND OUTPUT	DOUT22P	GND OUTPUT	DOUT26P	GND OUTPUT	DOUT30P	GNDINPUT	DIN30P	GNDINPUT	DIN26P	GNDINPUT	DIN22P	GNDINPUT	DIN18P	GNDINPUT	GNDINPUT	VCCINPUT	DIN14N	DIN14P
AA	GND OUTPUT	DOUT13P	DOUT13N	GND OUTPUT	VCC OUTPUT	DOUT18N	DOUT20P	DOUT22N	DOUT24P	DOUT26N	DOUT28P	DOUT30N	GND OUTPUT	DIN30N	DIN28P	DIN26N	DIN24P	DIN22N	DIN20P	DIN18N	VCCINPUT	GNDINPUT	DIN13N	DIN13P	GNDINPUT
Y	DOUT12P	DOUT12N	VCC OUTPUT	DOUT11P	DOUT11N	VCC OUTPUT	DOUT20N	VCC OUTPUT	DOUT24N	VCC OUTPUT	DOUT28N	VCC OUTPUT	VCCINPUT	VCCINPUT	DIN28N	VCCINPUT	DIN24N	VCCINPUT	DIN20N	VCCINPUT	DIN11N	DIN11P	VCCINPUT	DIN12N	DIN12P
W	GND OUTPUT	DOUT10P	DOUT10N	GND OUTPUT	DOUT9P	DOUT9N	GND OUTPUT	GND INPUT	GND OUTPUT	GND INPUT	GND OUTPUT	GND INPUT	GND OUTPUT	GNDTTL	GNDINPUT	GNDTTL	GNDINPUT	GNDTTL	GNDINPUT	DIN9N	DIN9P	GNDINPUT	DIN10N	DIN10P	GNDINPUT
V	DOUT8P	DOUT8N	VCC OUTPUT	DOUT7P	DOUT7N	VCC OUTPUT	GND INPUT	VCC INPUT	GND INPUT	VCC INPUT	GND INPUT	VCC INPUT	GND INPUT	VCCTTL	RDATA7	RDATA6	RDATA5	RDATA4	GNDTTL	VCCINPUT	DIN7N	DIN7P	VCCINPUT	DIN8N	DIN8P
U	GND OUTPUT	DOUT6P	DOUT6N	GND OUTPUT	DOUT5P	DOUT5N	GND OUTPUT	GND INPUT	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	GNDTTL	RDATA3	RDATA2	RDATA1	RDATA0	GNDINPUT	DIN5N	DIN5P	GNDINPUT	DIN6N	DIN6P	GNDINPUT
T	DOUT4P	DOUT4N	VCC OUTPUT	DOUT3P	DOUT3N	VCC OUTPUT	GND INPUT	GND INPUT	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCINPUT	DIN3N	DIN3P	VCCINPUT	DIN4N	DIN4P
R	GND OUTPUT	DOUT2P	DOUT2N	GND OUTPUT	DOUT1P	DOUT1N	GND OUTPUT	VADJUST1	GND INPUT	GND INPUT	GND INPUT	GND INPUT	GND INPUT	GNDTTL	OE	IADDR6	IADDR5	IADDR4	GNDINPUT	DIN1N	DIN1P	GNDINPUT	DIN2N	DIN2P	GNDINPUT
P	DOUT0P	DOUT0N	VCC OUTPUT	DOUT68P	DOUT68N	VCC OUTPUT	GND INPUT	VADJUST2	VCSHIGH1	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	GNDTTL	IADDR3	IADDR2	IADDR1	IADDR0	GNDTTL	VCCINPUT	DIN67N	DIN67P	VCCINPUT	DIN0N	DIN0P
N	GND OUTPUT	DOUT67P	DOUT67N	GND OUTPUT	DOUT66P	DOUT66N	GND OUTPUT	VADJUST3	GND INPUT	GND INPUT	GND INPUT	GND INPUT	GND INPUT	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCTTL	GNDINPUT	DIN65N	DIN65P	GNDINPUT	DIN66N	DIN66P	GNDINPUT
M	DOUT65P	DOUT65N	VCC OUTPUT	DOUT64P	DOUT64N	VCC OUTPUT	GND INPUT	VADJUST4	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	GNDTTL	VCCTTL	OADDR6	OADDR5	OADDR4	GNDTTL	VCCINPUT	DIN63N	DIN63P	VCCINPUT	DIN64N	DIN64P
L	GND OUTPUT	DOUT63P	DOUT63N	GND OUTPUT	DOUT62P	DOUT62N	GND OUTPUT	VADJUST5	VCSHIGH2	GND INPUT	GND INPUT	GND INPUT	GND INPUT	GNDTTL	OADDR3	OADDR2	OADDR1	OADDR0	GNDINPUT	DIN61N	DIN61P	GNDINPUT	DIN62N	DIN62P	GNDINPUT
K	DOUT61P	DOUT61N	VCC OUTPUT	DOUT60P	DOUT60N	VCC OUTPUT	GND INPUT	VADJUST6	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCINPUT	DIN59N	DIN59P	VCCINPUT	DIN60N	DIN60P
J	GND OUTPUT	DOUT59P	DOUT59N	GND OUTPUT	DOUT58P	DOUT58N	GND OUTPUT	GND INPUT	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	VCC INPUT	GNDTTL	VCCTTL	RESETN	RDACTN	RDCFGN	GNDINPUT	DIN57N	DIN57P	GNDINPUT	DIN58N	DIN58P	GNDINPUT
H	DOUT57P	DOUT57N	VCC OUTPUT	DOUT56P	DOUT56N	VCC OUTPUT	GND INPUT	VCC INPUT	GND INPUT	VCC INPUT	GND INPUT	VCC OUTPUT	GND OUTPUT	GND OUTPUT	VCCTTL	CONFIGN	LOADN	CSN	GNDTTL	VCCINPUT	DIN55N	DIN55P	VCCINPUT	DIN56N	DIN56P
G	GND OUTPUT	DOUT55P	DOUT55N	GND OUTPUT	DOUT54P	DOUT54N	GND OUTPUT	GND INPUT	GND OUTPUT	GND INPUT	GND OUTPUT	GND OUTPUT	DOUT32N	VCC OUTPUT	GNDINPUT	GNDTTL	GNDINPUT	GNDTTL	GNDINPUT	DIN53N	DIN53P	GNDINPUT	DIN54N	DIN54P	GNDINPUT
F	DOUT53P	DOUT53N	VCC OUTPUT	DOUT52P	DOUT52N	VCC OUTPUT	DOUT43N	VCC OUTPUT	DOUT39N	VCC OUTPUT	DOUT35N	VCC OUTPUT	DOUT32P	VCCINPUT	DIN34N	VCCINPUT	DIN38N	VCCINPUT	DIN42N	VCCINPUT	DIN51N	DIN51P	VCCINPUT	DIN52N	DIN52P
E	GND OUTPUT	DOUT51P	DOUT51N	GND OUTPUT	VCC OUTPUT	DOUT45N	DOUT43P	DOUT41N	DOUT39P	DOUT37N	DOUT35P	DOUT33N	GND OUTPUT	DIN32N	DIN34P	DIN36N	DIN38P	DIN40N	DIN42P	DIN44N	VCCINPUT	GNDINPUT	DIN50N	DIN50P	GNDINPUT
D	DOUT50P	DOUT50N	VCC OUTPUT	GND OUTPUT	GND OUTPUT	DOUT45P	GND OUTPUT	DOUT41P	GND OUTPUT	DOUT37P	GND OUTPUT	DOUT33P	GNDINPUT	DIN32P	GNDINPUT	DIN36P	GNDINPUT	DIN40P	GNDINPUT	DIN44P	GNDINPUT	GNDINPUT	VCCINPUT	DIN49N	DIN49P
C	VCC OUTPUT	GND OUTPUT	DOUT49N	VCC OUTPUT	DOUT47N	VCC OUTPUT	DOUT44N	VCC OUTPUT	DOUT40N	VCC OUTPUT	DOUT36N	VCC OUTPUT	VCCINPUT	VCCINPUT	DIN35N	VCCINPUT	DIN39N	VCCINPUT	DIN43N	VCCINPUT	DIN46N	VCCINPUT	DIN48N	GNDINPUT	VCCINPUT
B		VCC OUTPUT	DOUT49P	DOUT48N	DOUT47P	DOUT46N	DOUT44P	DOUT42N	DOUT40P	DOUT38N	DOUT36P	DOUT34N	GND OUTPUT	DIN33N	DIN35P	DIN37N	DIN39P	DIN41N	DIN43P	DIN45N	DIN46P	DIN47N	DIN48P	VCCINPUT	
A			GND OUTPUT	DOUT48P	GND OUTPUT	DOUT46P	GND OUTPUT	DOUT42P	GND OUTPUT	DOUT38P	GND OUTPUT	DOUT34P	GNDINPUT	DIN33P	GNDINPUT	DIN37P	GNDINPUT	DIN41P	GNDINPUT	DIN45P	GNDINPUT	DIN47P	GNDINPUT		

Figure 11. Compact 32.5 mm x 32.5 mm 624 Pin CBGA Package

DW0032-58 624 CERAMIC BALL GRID ARRAY



DIMENSIONS (are in millimeters)

UNIT	A_1	S	C	M	D	D_1	D_2	E	E_1	E_2	b	e
MIN	0.80	1.40	2.60		32.30	30.28	30.25	32.30	30.28	30.25		1.27 BASIC
NOM	0.90		2.75		32.50	30.48	30.50	32.50	30.48	30.50	0.89	
MAX	1.00	2.90	2.90	6.80	32.70	30.68	30.75	32.70	30.68	30.75		

THERMAL MANAGEMENT

The S2090 requires thermal management. An example is provided on how to select the proper heat sink for specific system requirements (see page 29). The heat sink used in the example is available from:

Name: Aavid/Thermalloy
Address: 2021 W. Valley View Lane
City, State Zip: Dallas, TX 75234

Phone: (858) 271-0333
Fax: (949) 888-3321
Email: jaldridge@englishsales.com
Web: www.englishsales.com

Airflow requirement is determined by:

$Pd = (T_{j\ max} - T_{a\ max}) / \theta_{ja}$, $\theta_{ja} = \theta_{jc} + \theta_{ca}$

$\theta_{sa\ (required)} = \theta_{ja} - \theta_{jc} - \theta_{cs}$

where $T_{j\ max}$ is the maximum junction temperature
$T_{a\ max}$ is the maximum ambient temperature
θ_{ja} is the thermal resistance from junction to ambient
θ_{jc} is the thermal resistance from junction to case
θ_{ca} is the thermal resistance from case to ambient (if a heat sink is used, this is θ_{sa} - sink to ambient)
θ_{cs} is the thermal resistance from case to sink.
θ_{sa} is the thermal resistance from sink to ambient.

Tables 14 and 15 show the max package power vs. airlfow (with and without heat sink), calculated using the equation above with $T_{j\ max}$ = 125˚C and $T_{a\ max}$ = 70˚C. In order to successfully use the S2090, the max package power must exceed the specified max power dissipation of the device, which is determined by the output swing setting (see Tables 17 and 18). The dimensions of the heat sink are provided in Table 15.

Table 14. S2090 Package Power Dissipation vs. Air Flow, No Heat Sink

Max Package Power (W)	Air Flow (LFPM)	θ_{ja} (°C/W)	θ_{jc} (°C/W)
4.66	0	11.8	0.47
5.19	100	10.6	0.47
5.85	200	9.4	0.47
6.47	300	8.5	0.47
7.14	400	7.7	0.47
8.21	600	6.7	0.47

A sample of system requirements given:
Possibly will use output settings #1 or #2: max power dissipations at +2.5 V power supply are 10.31 W or 11.44 W, respectively.

Ambient temperature: 70˚C

Dimensions of heat sink: less than 35 mm x 35 mm

Heat sink height: less than 0.50 inches

Eg. for output setting # 1

θ_{jc} = 0.47˚C/W
θ_{cs} = 0.54˚C/W (Ther-A-Grip 1070; assumption)
θ_{ja} (required) = ($T_{j\ max}$ - $T_{a\ max}$)/Pd = θ_{ja}
125 - 70/10.31 = 5.33˚C/W
θ_{sa} (required) = θ_{ja} - θ_{jc} - θ_{cs}
5.33 - 0.47 - 0.54 = 4.32˚C/W

Table 15 provides the θ_{sa} for different airflows for the Aavid/Thermalloy 2338B Heat sink.

Table 15. S2090 Power Dissipation vs. Air Flow, # 2338B Heat Sink (31.37 mm x 33.02 mm x 12.45 mm)

Max Device Power (W)	Air Flow (LFPM)	θ_{ja} (required)	θ_{sa} (required)	θ_{sa} (# 2338B) (°C/W)
10.31 (Output Setting #1)	300	5.33	4.32	4.0
11.44 (Output Setting #2)	400	4.81	3.8	3.2

Table 16. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	°C
Voltage on any Power Pin w.r.t. GND	-0.5		5	V
Voltage on any LVTTL Input Pin	-0.5		V_{CC} +0.5	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
High Speed CML Output Source Current			30	mA

Electrostatic Discharge (ESD) Ratings

The S2090 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at 1500 V.

Table 17. Recommended Operating Conditions (+3.3 V supply)

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	°C
Junction Temperature Under Bias			125	°C
Voltage on any Power Pin w.r.t. GND	3.13	3.3	3.47	V
Voltage on any LVTTL Input Pin	0		3.47	V
Voltage on any LVPECL Input Pin	1.9		V_{CC} -0.3	V
I_{CC} Supply Current (with output setting #1)		3.9	4.74	A
I_{CC} Supply Current (with output setting #2)		4.2	5.04	A
I_{CC} Supply Current (with output setting #3)		4.4	5.35	A
I_{CC} Supply Current (with output setting #4)		4.6	5.64	A
I_{CC} Supply Current (with output setting #5)		4.9	5.93	A
I_{CC} Supply Current (with output setting #6)		5.2	6.20	A
Power Dissipation (with output setting #1)		13.04	16.45	W
Power Dissipation (with output setting #2)		13.87	17.51	W
Power Dissipation (with output setting #3)		14.71	18.57	W
Power Dissipation (with output setting #4)		15.50	19.56	W
Power Dissipation (with output setting #5)		16.31	20.58	W
Power Dissipation (with output setting #6)		17.06	21.52	W

Table 18. Recommended Operating Conditions (+2.5 V supply)

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	°C
Junction Temperature Under Bias			125	°C
Voltage on any Power Pin w.r.t. GND	2.38	2.5	2.63	V
Voltage on any LVTTL Input Pin	0		V_{CC}	V
Voltage on any LVPECL Input Pin	1.9		V_{CC} -0.3	V
I_{CC} Supply Current (with output setting #1)		3.18	3.92	A
I_{CC} Supply Current (with output setting #2)		3.40	4.35	A
I_{CC} Supply Current (with output setting #3)		3.62	4.79	A
I_{CC} Supply Current (with output setting #4)		3.83	5.22	A
I_{CC} Supply Current (with output setting #5)		4.0	5.62	A
I_{CC} Supply Current (with output setting #6)		4.2	6.01	A
Power Dissipation (with output setting #1)		7.94	10.31	W
Power Dissipation (with output setting #2)		8.50	11.44	W
Power Dissipation (with output setting #3)		9.05	12.6	W
Power Dissipation (with output setting #4)		9.57	13.73	W
Power Dissipation (with output setting #5)		10.08	14.78	W
Power Dissipation (with output setting #6)		10.53	15.81	W

Table 19. Power Down Savings Per Output (+3.3 V supply)

Parameter	Min	Typ	Max	Units
Power Savings (with output setting #1)		39	48	mW
Power Savings (with output setting #2)		56	73	mW
Power Savings (with output setting #3)		75	96	mW
Power Savings (with output setting #4)		92	117	mW
Power Savings (with output setting #5)		110	140	mW
Power Savings (with output setting #6)		127	163	mW

Note: The number of outputs powered down multiplied by the power savings at specified output amplitude equals total power savings.

Table 20. Power Down Savings Per Output (+2.5 V supply)

Parameter	Min	Typ	Max	Units
Power Savings (with output setting #1)		24	32	mW
Power Savings (with output setting #2)		36	48	mW
Power Savings (with output setting #3)		49	60	mW
Power Savings (with output setting #4)		59	77	mW
Power Savings (with output setting #5)		66	90	mW
Power Savings (with output setting #6)		77	104	mW

Note: The number of outputs powered down multiplied by the power savings at specified output amplitude equals total power savings.

Table 21. Input/Output Characteristics (+3.3 V supply)

Parameter	Description	Min	Typ	Max	Units	Conditions
LVTTL Inputs						
V_{IH}	Input High Voltage	2		3.47	V	V_{CC} = Max
V_{IL}	Input Low Voltage	0		0.8	V	V_{CC} = Max
I_{IH}	Input High Current			10	µA	VIN = 2.4 V
I_{IL}	Input Low Current	-100			µA	VIN = 0.5 V
ΔV_{HYST}	Magnitude of hysteresis		120		mV	
LVTTL Outputs[1]						
V_{OH}	Output High Voltage	2.4	2.8	V_{CC}	V	Max I_{OH} = –2 mA
V_{OL}	Output Low Voltage	GND	0.025	0.5	V	Min I_{OL} = +2 mA
T_R, T_F	LVTTL Output Rise and Fall Time		2	5	ns	See Note 1. See Figure 14.
LVPECL Inputs						
V_{ID}	Differential Input Voltage Swing	200		1600	mV	See Figure 12.
V_I	Input Voltage Range	1.9		V_{CC} -0.3	V	See Figure 16. Only used when DC coupling to the inputs.
$V_{INOFFSET}$	Inherent DC offset voltage between the P and N of each input.		11		mV	
I_{IH}	Input High Current			15	mA	V_{ID} = Max
I_{IL}	Input Low Current	-15			mA	V_{ID} = Max
R_{DIFF}	Differential Input Resistance	90	119	150	Ω	
CML Outputs						
V_{OH}	CML Output High Voltage (with output setting #1)	V_{CC} -0.22		V_{CC} -0.013	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #1)	V_{CC} -0.60		V_{CC} -0.037	V	100 Ω line to line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #2)	V_{CC} -0.30		V_{CC} -0.051	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #2)	V_{CC} -0.82		V_{CC} -0.13	V	100 Ω line to line. (Without AC coupling caps.)

1. LVTTL AC timing measurements are assumed to have an output load of 10 pF.

Table 21. Input/Output Characteristics (+3.3 V supply) (Continued)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	CML Output High Voltage (with output setting #3)	V_{CC} -0.37		V_{CC} -0.083	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #3)	V_{CC} -0.98		V_{CC} -0.24	V	100 Ω line to line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #4)	V_{CC} -0.44		V_{CC} -0.11	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #4)	V_{CC} -1.175		V_{CC} -0.32	V	100 Ω line to line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #5)	V_{CC} -0.52		V_{CC} -0.13	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #5)	V_{CC} -1.43		V_{CC} -0.34	V	100 Ω line to line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #6)	V_{CC} -0.58		V_{CC} -0.17	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #6)	V_{CC} -1.62		V_{CC} -0.42	V	100 Ω line to line. (Without AC coupling caps.)
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #1)	300	380	455	mV	100 Ω line to line. See Figure 13. See Tables 2 and 2A for output swing settings. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #2)	435	550	655	mV	100 Ω line to line. See Figure 13. See Tables 2 and 2A for output swing settings. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #3)	570	715	860	mV	100 Ω line to line. See Figure 13. See Tables 2 and 2A for output swing settings. Peak-to-peak.

Table 21. Input/Output Characteristics (+3.3 V supply) (Continued)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #4)	700	870	1050	mV	100 Ω line to line. See Figure 13. See Tables 2 and 2A for output swing settings. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #5)	825	1030	1240	mV	100 Ω line to line. See Figure 13. See Tables 2 and 2A for output swing settings. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #6)	940	1180	1420	mV	100 Ω line to line. See Figure 13. See Tables 2 and 2A for output swing settings. Peak-to-peak.
R_O	Output Impedance (Single Ended)	45	57	70	Ω	

Table 22. Input/Output Characteristics (+2.5 V supply)

Parameter	Description	Min	Typ	Max	Units	Conditions
LVTTL Inputs						
V_{IH}	Input High Voltage	2		V_{CC}	V	V_{CC} = Max
V_{IL}	Input Low Voltage	0		0.8	V	V_{CC} = Max
I_{IH}	Input High Current			10	µA	VIN = 2.4 V
I_{IL}	Input Low Current	-100			µA	VIN = 0.5 V
ΔV_{HYST}	Magnitude of hysteresis		120		mV	
LVTTL Outputs[1]						
V_{OH}	Output High Voltage	1.8	2.0	V_{CC}	V	Max I_{OH} = –2 mA. Buffer required to meet 2.0 V LVTTL V_{IH} specification. See pg. 7, "User note (Parallel Read Back)" section to meet LVTTL V_{IH}. This reduced V_{OH} only occurs when using +2.5 V power supply.
V_{OL}	Output Low Voltage	GND	0.025	0.5	V	Min I_{OL} = +2 mA
T_R, T_F	LVTTL Output Rise and Fall Time		2	6	ns	See Note 1. See Figure 14.
LVPECL Inputs						
V_{ID}	Differential Input Voltage Swing	200		1600	mV	See Figure 12.
V_I	Input Voltage Range	1.9		V_{CC} -0.3	V	See Figure 16. Only used when DC coupling to the inputs.
$V_{INOFFSET}$	Inherent DC offset voltage between the P and N of each input		8		mV	
I_{IH}	Input High Current			15	mA	V_{ID} = Max
I_{IL}	Input Low Current	-15			mA	V_{ID} = Max
R_{DIFF}	Differential Input Resistance	90	119	150	Ω	
CML Outputs						
V_{OH}	CML Output High Voltage (with output setting #1)	V_{CC} -0.22		V_{CC} -0.013	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #1)	V_{CC} -0.60		V_{CC} -0.037	V	100 Ω line to line. (Without AC coupling caps.)

1. LVTTL AC timing measurements are assumed to have an output load of 10 pF.

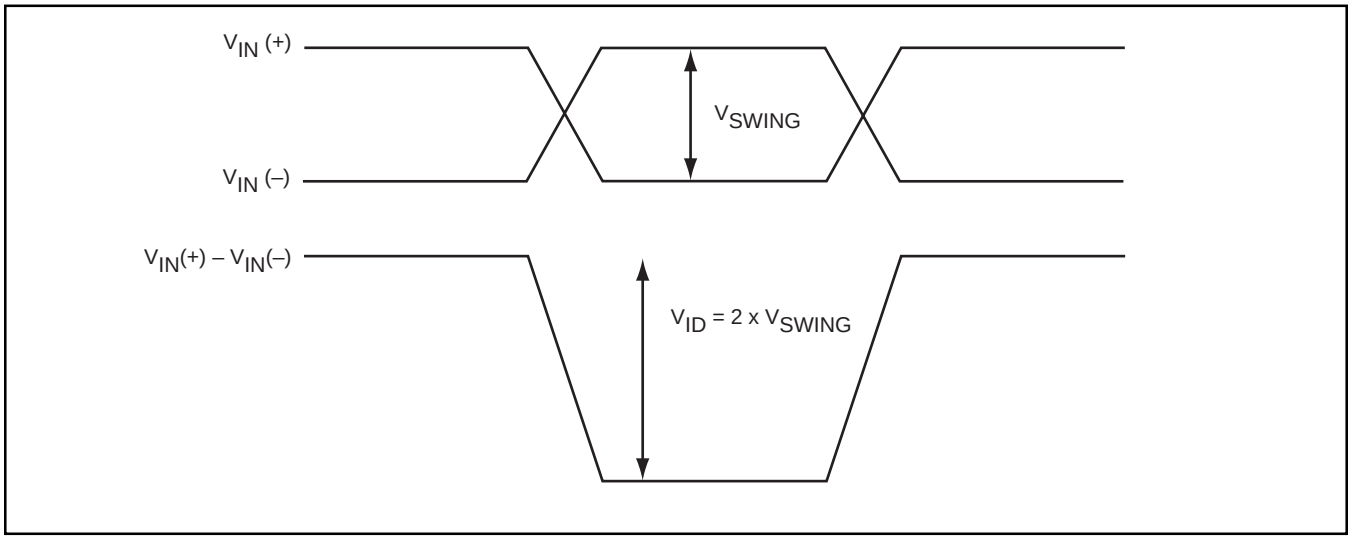
Table 22. Input/Output Characteristics (+2.5 V supply) (Continued)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	CML Output High Voltage (with output setting #2)	V_{CC} -0.30		V_{CC} -0.051	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #2)	V_{CC} -0.82		V_{CC} -0.13	V	100 Ω line to line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #3)	V_{CC} -0.37		V_{CC} -0.083	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #3)	V_{CC} -0.98		V_{CC} -0.24	V	100 Ω line to line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #4)	V_{CC} -0.44		V_{CC} -0.11	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #4)	V_{CC} -1.175		V_{CC} -0.32	V	100 Ω line to line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #5)	V_{CC} -0.52		V_{CC} -0.13	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #5)	V_{CC} -1.43		V_{CC} -0.34	V	100 Ω line to line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #6)	V_{CC} -0.58		V_{CC} -0.17	V	100 Ω line to line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #6)	V_{CC} -1.62		V_{CC} -0.42	V	100 Ω line to line. (Without AC coupling caps.)
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #1)	210	300	390	mV	100 Ω line to line. See Figure 13. See Tables 3 and 3A for output swing settings. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #2)	310	440	540	mV	100 Ω line to line. See Figure 13. See Tables 3 and 3A for output swing settings. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #3)	385	570	715	mV	100 Ω line to line. See Figure 13. See Tables 3 and 3A for output swing settings. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #4)	440	685	870	mV	100 Ω line to line. See Figure 13. See Tables 3 and 3A for output swing settings. Peak-to-peak.

Table 22. Input/Output Characteristics (+2.5 V supply) (Continued)

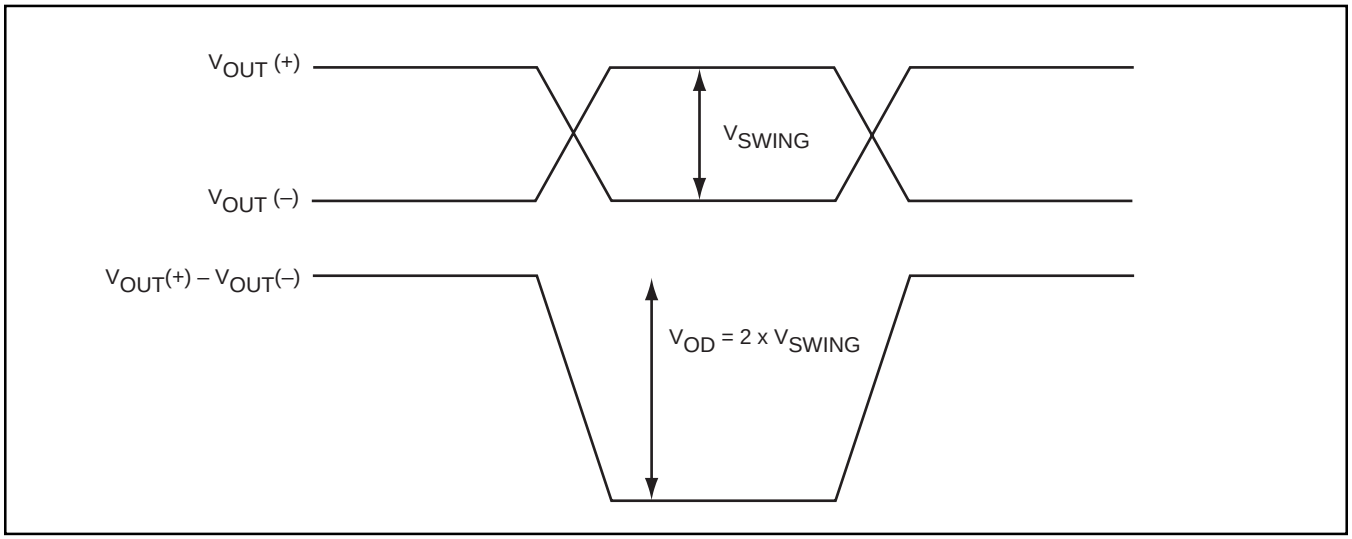
Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #5)	465	774	1046	mV	100 Ω line to line. See Figure 13. See Tables 3 and 3A for output swing settings. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (with output setting #6)	582	898	1213	mV	100 Ω line to line. See Figure 13. See Tables 3 and 3A for output swing settings. Peak-to-peak.
R_O	Output Impedance (Single Ended)	45	57	70	Ω	

Figure 12. Differential Input Voltage



Note: $V_{IN}(+) – V_{IN}(-)$ is the algebraic difference of the input signals.

Figure 13. Differential Output Voltage



Note: $V_{OUT}(+) – V_{OUT}(-)$ is the algebraic difference of the input signals.

Figure 14. LVTTL Input/Output Rise and Fall Time

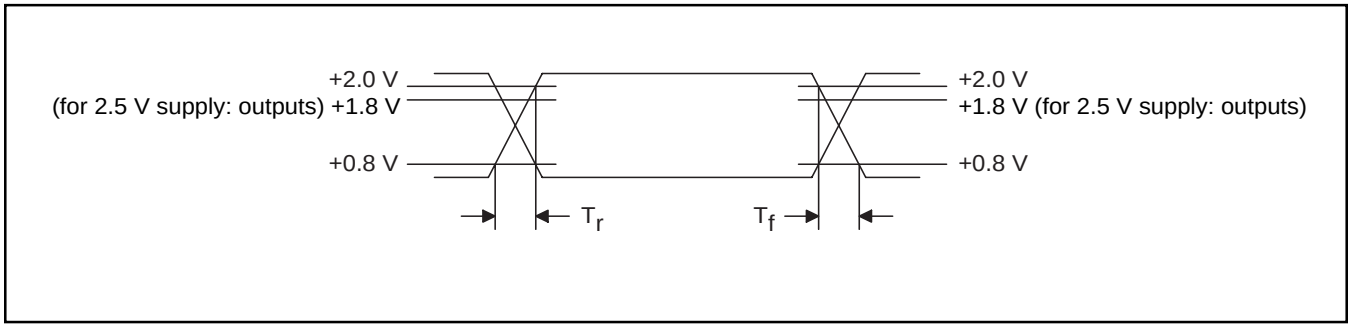


Figure 15. Differential CML Output to +3.3 V or +2.5 V PECL Input AC Coupled Termination

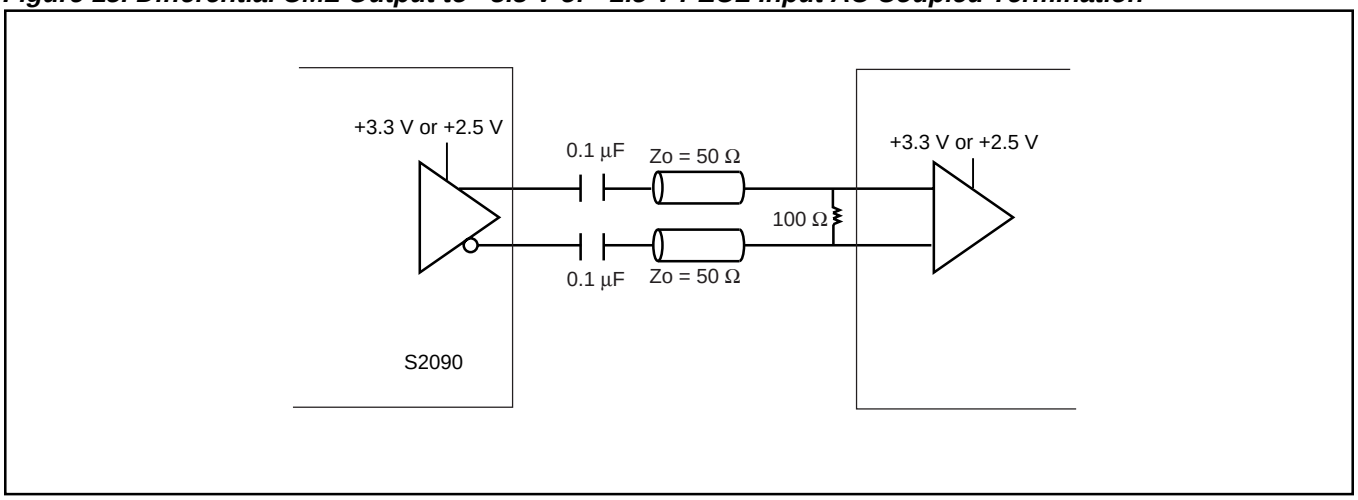


Figure 16. S2090 Output DC Coupled to S2090 Input

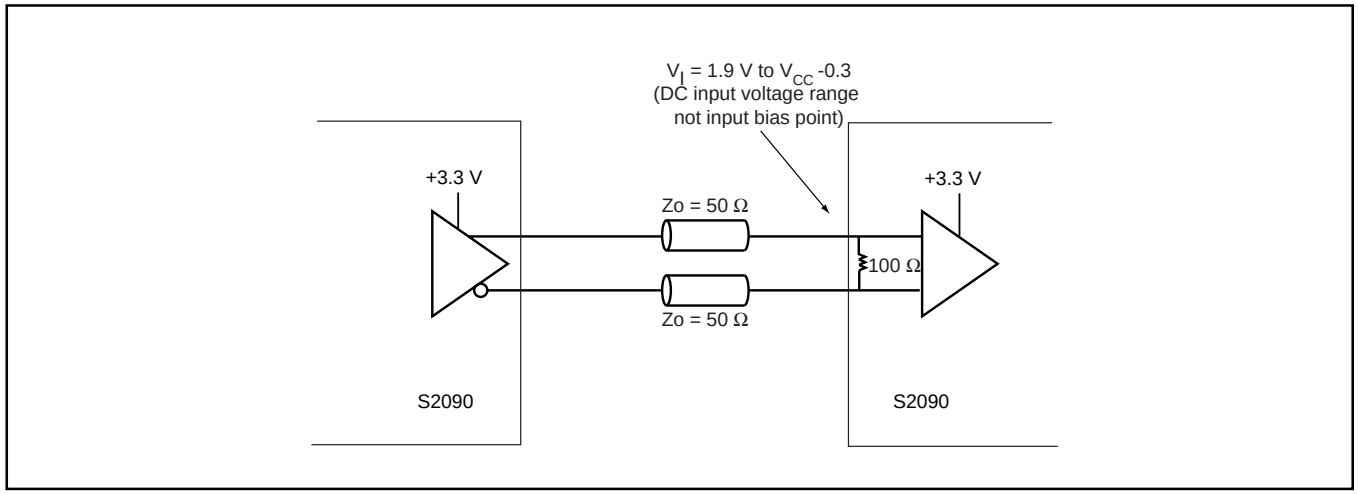


Figure 17. S2080 Output DC Coupled to S2090 Input

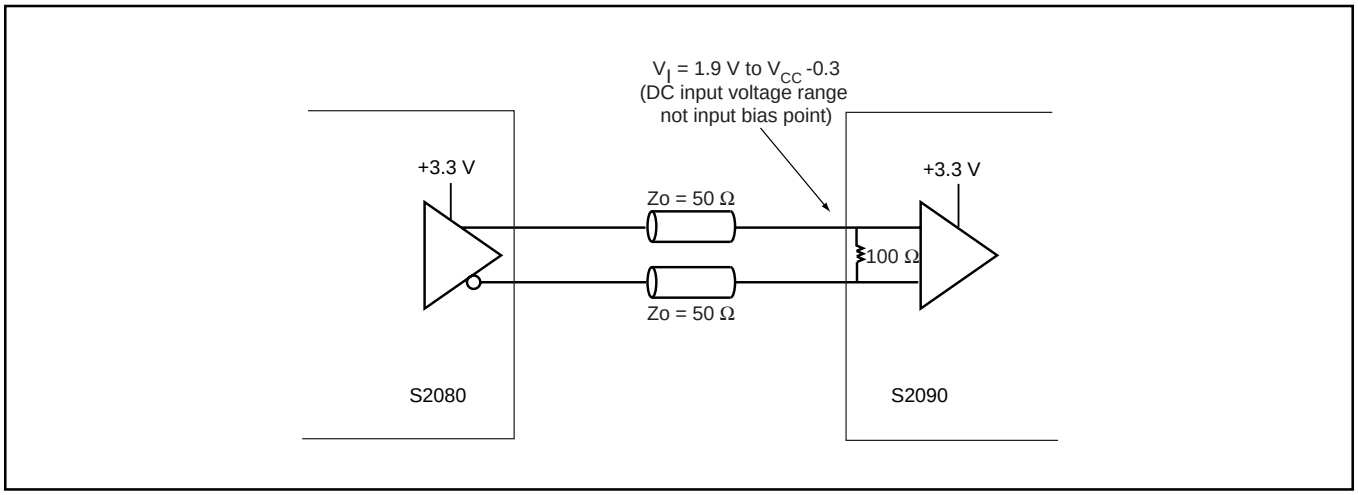


Figure 18. S2090 Output DC Coupled to S2080 Input

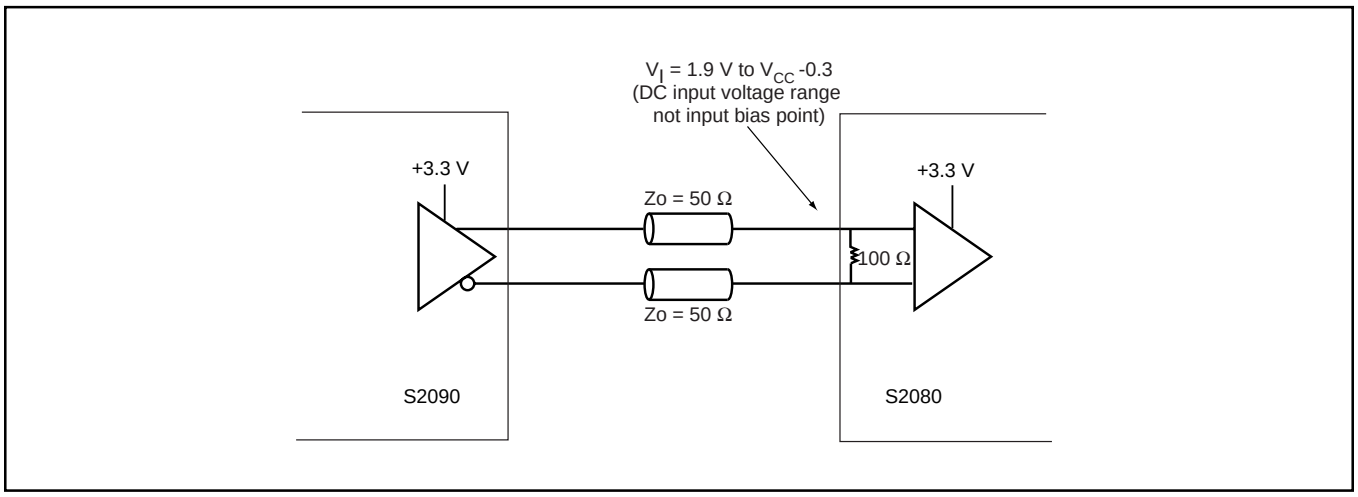
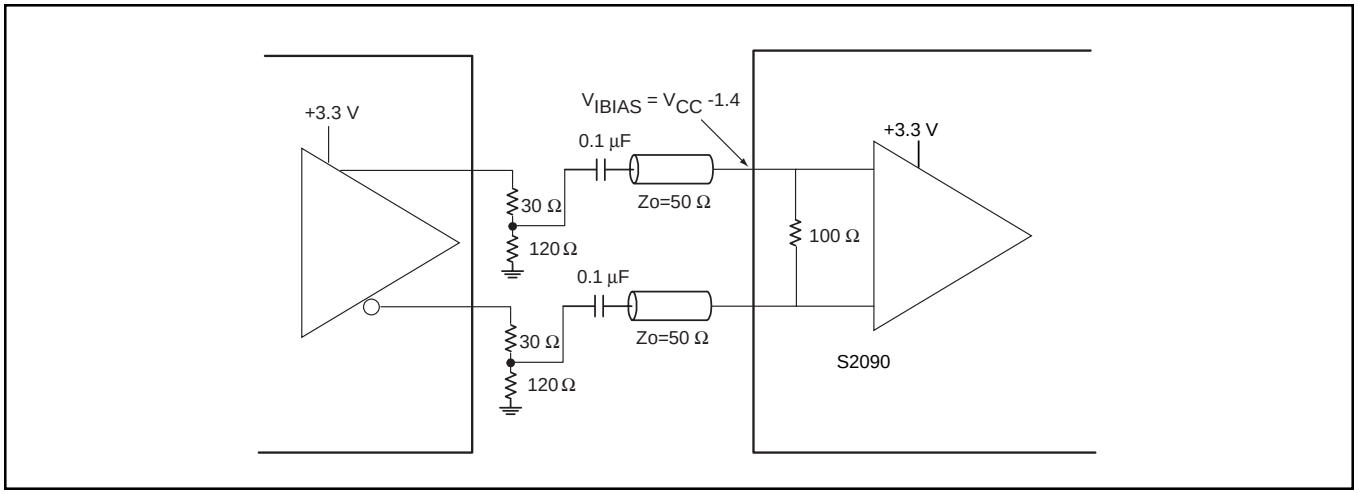


Figure 19. Differential LVPECL Inputs



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	2090	CB – 624 CBGA

X Prefix XXXX Device XX Package

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