Document Title

256Kx72 Double Late Write SigmaRAM™

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial document.	November 2, 2000	Preliminary
0.1	1. Preliminary	March 30, 2001	Preliminary
0.2	1. Add scan order information	May 16, 2001	Preliminary
0.3	1. Part name change from K7N167285A to K7Z167285A	July 18, 2001	Preliminary

16Mb NtRAM(Flow Through / Pipelined) / Sigma x72 Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
1Mx18	K7M161825A-Q(H/F)C(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns	Q : 100TQFP H : 119BGA F: 165FBGA	C (Commercial Temperature Range) I (Industrial Temperature Range)
	K7N161801A-Q(H/F)C(I)16/13	Pipelined	3.3	167/133MHz		
	K7N161809A-Q(H/F)C(I)25/22/20	Pipelined	3.3	250/225/200MHz		
	K7N161845A-Q(H/F)C(I)16/13	Pipelined	2.5	167/133MHz		
	K7N161849A-Q(H/F)C(I)25/22/20	Pipelined	2.5	250/225/200MHz		
512Kx32	K7M163225A-QC(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns		
	K7N163201A-QC(I)16/13	Pipelined	3.3	167/133MHz		
	K7N163209A-QC(I)25/22/20	Pipelined	3.3	250/225/200MHz		
	K7N163245A-QC(I)16/13	Pipelined	2.5	167/133MHz		
	K7N163249A-QC(I)25/22/20	Pipelined	2.5	250/225/200MHz		
512Kx36	K7M163625A-Q(H/F)C(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5ns		
	K7N163601A-Q(H/F)C(I)16/13	Pipelined	3.3	167/133MHz		
	K7N163609A-Q(H/F)C(I)25/22/20	Pipelined	3.3	250/225/200MHz		
	K7N163645A-Q(H/F)C(I)16/13	Pipelined	2.5	167/133MHz		
	K7N163649A-Q(H/F)C(I)25/22/20	Pipelined	2.5	250/225/200MHz		
256Kx72	K7N167245A-HC16/13	Pipelined (Normal Type)	2.5	167/133MHz	H : 209BGA	
	K7N167249A-HC25/22/20	Pipelined (Normal Type)	2.5	250/225/200MHz		
	K7Z167285A-HC30/27/25	Pipelined (Sigma Type)	1.8	300/275/250MHz		

256Kx72-Bit Pipelined SigmaRAM™

FEATURES

- Double Late Write mode , Pipelined Read mode.
- 1.8V+150/-100 mV Power Supply.
- 1.8V I/O supply.
- Byte Writable Function.
- Single $\overline{R}$EAD/WRITE control pin.
- Self-Timed Write Cycle.
- Complement echo clock outputs
- Selectable impedance output buffer
- 2 User programmable chip enable inputs for easy depth expansion.(EP2, EP3)
- Supports linear burst mode only.
- Slow Down Function.
- IEEE 1149.1 JTAG Compatible Boundary Scan
- 209 bump, 14mm x 22mm, 1mm bump pitch BGA package
- 209BGA(11x19 Ball Grid Array Package).

GENERAL DESCRIPTION

The K7Z167285A is 18,874,368-bits Synchronous Static SRAMs. The double late write SigmaRAM utilizes all the bandwidth in any combination of operating cycles.

Address, data inputs, and all control signals except EP2, EP3, and $\overline{SD}$ are synchronized to input clock.

Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

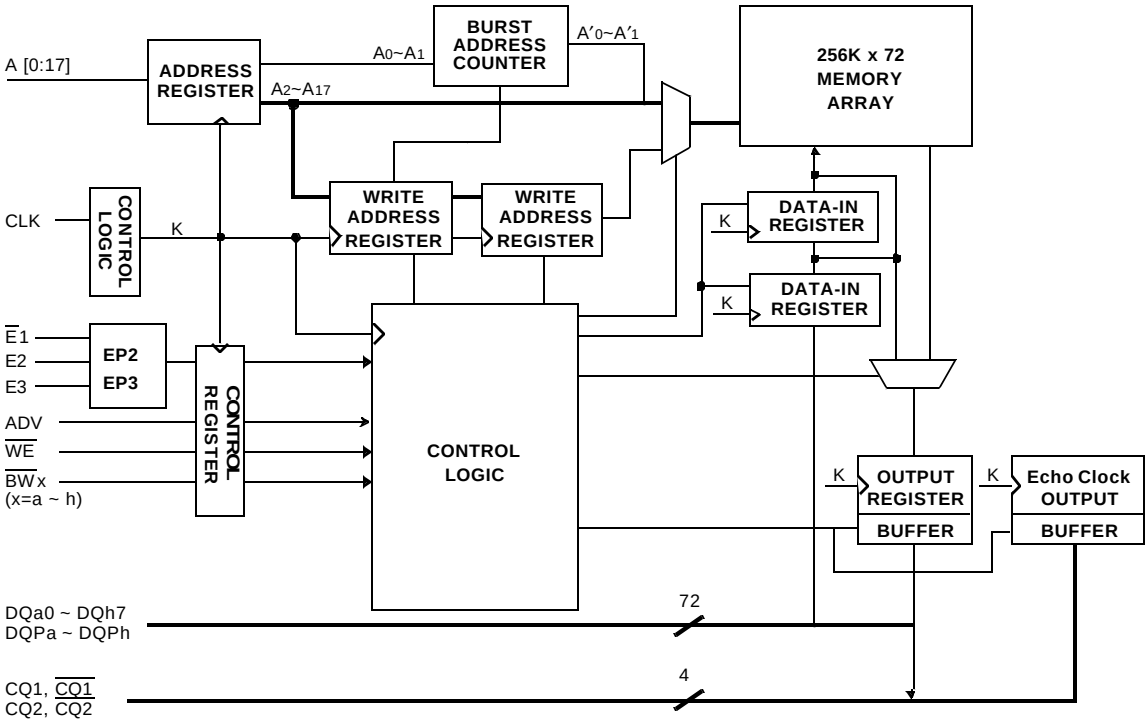
For read cycles,the SRAM output data is temporarily stored by an edge triggered output register and then released to the output buffers at the next rising edge of clock.

The K7Z167285A are implemented with SAMSUNG′s high performance CMOS technology and is available in 209BGA packages. Multiple power and ground pins minimize ground bounce.

FAST ACCESS TIMES

PARAMETER	Symbol	-30	-27	-25	Unit
Cycle Time	t_{CYC}	3.3	3.6	4.0	ns
Clock Access Time	t_{CD}	1.8	2.0	2.1	ns

LOGIC BLOCK DIAGRAM



209BGA PACKAGE PIN CONFIGURATIONS (TOP VIEW)

256Kx72 Common I/O-Top View

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	E2	A	ADV	A	E3	A	DQb	DQb
B	DQg	DQg	$\overline{BW}$c	$\overline{BW}$g	NC	$\overline{WE}$	A	$\overline{BW}$b	$\overline{BW}$f	DQb	DQb
C	DQg	DQg	$\overline{BW}$h	$\overline{BW}$d	NC(128M)	$\overline{E1}$	NC	$\overline{BW}$e	$\overline{BW}$a	DQb	DQb
D	DQg	DQg	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	DQb	DQb
E	DQPg	DQPc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPf	DQPb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
K	CQ2	$\overline{CQ2}$	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ1}$	CQ1
L	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	$\overline{SD}$	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQPd	DQPh	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPa	DQPe
T	DQd	DQd	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	DQe	DQe
U	DQd	DQd	NC	A	NC(64M)	A	NC(32M)	A	NC	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

Pin Description Table

Pin Name	Description	Type	Comments
A	Address	Input	-
ADV	Advance	Input	Active High
$\overline{BW}$x(x=a ~ h)	Byte Write Enable	Input	Active Low
CK	Clock	Input	Active High
DQ	Data I/O	Input/Output	-
CQ	Echo Clock Outputs	Output	Active High
$\overline{CQ}$	Echo Clock Outputs	Output	Active Low
$\overline{E1}$	Chip Enable	Input	Active Low
E2 & E3	Chip Enable	Input	Programmable Active High or Low
EP2 & EP3	Chip Enable Program Pin	Input	-
$\overline{SD}$	Slow Down Input	Input	Active Low
TCK	Test Clock	Input	Active High
TDI	Test Data In	Input	-
TDO	Test Data Out	Output	-
TMS	Test Mode Select	Input	-
MCH	Must Connect High	Input	Active High
MCL	Must Connect Low	Input	Active Low
NC	No Connect	-	Not connected to die
$\overline{WE}$	Write	Input	Active Low
V_{DD}	Core Power Supply	Input	1.8V Nominal
V_{DDQ}	Output Driver Power Supply	Input	1.8V Nominal
V_{SS}	Ground	Input	-

FUNCTION DESCRIPTION

The K7Z167285A is Pipelined SigmaRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa.
Because a Pipelined SigmaRAM is a synchronous device, address, data Inputs, and read/write control inputs are captured on the rising edge of the input clock. EP2 , EP3 and $\overline{SD}$ are asynchronous control input.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, all three chip enables($\overline{E1}$, E2, E3) are active, the write enable input signals $\overline{WE}$ are driven high, and ADV driven low.The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM.

Write operation occurs when $\overline{WE}$ is driven low at the rising edge of the clock. $\overline{BW}$x[h:a] can be used for byte write operation. The pipelined Pipelined SigmaRAM uses a double-late write cycle to utilize 100% of the bandwidth.
At the first rising edge of the clock, $\overline{WE}$ and address are registered, and the data associated with that address is required two cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst seguence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

Pipelined SigmaRAM supports linear burst sequence only.

BURST SEQUENCE TABLE (Linear Burst Order)

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Slow Down Function

$\overline{SD}$ is helpful to prevent to bus contention in read operation after write operation , especially high frequency application.
When $\overline{SD}$ is Low, the SRAM is operated in a slow down mode. In a slow down mode, the enable/disable timings of output data become slower , which are defined as tKHQV,tKHQZ,tKHQX,tKHQX1/tKHCH and tKLCL.
The valid data window in slow down mode is same with normal operation mode , so it will be helpful in read operation after write operation
When $\overline{SD}$ is High , the SRAM returns to normal operation node.
The state of $\overline{SD}$ must be fixed before operation , and it can not be changed during operation.

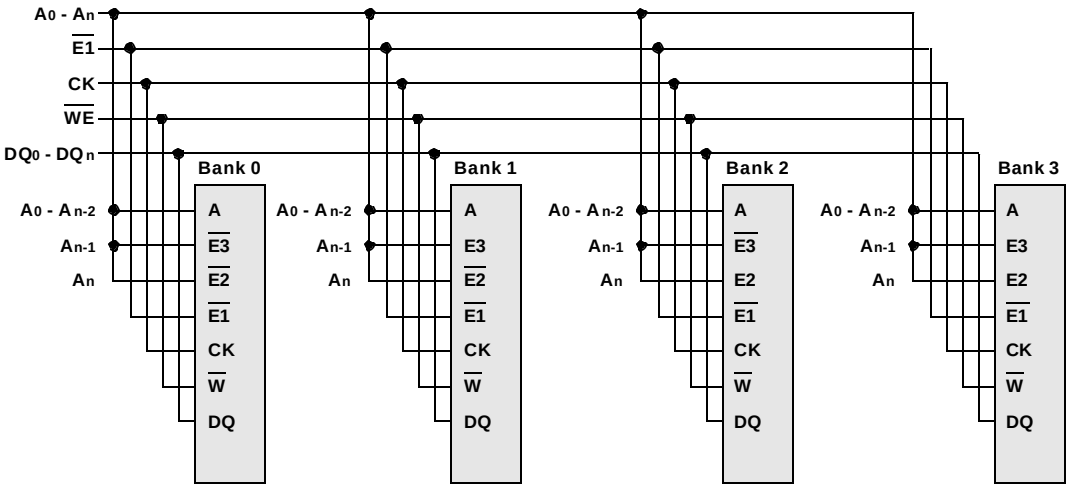
Programmable Enables

Double Late Write SigmaRAM features two user programmable chip enable inputs, E2 and E3. The sense of the inputs, whether they function as active low or active high inputs, is determined by the state of the programming inputs, EP2 and EP3. For example, if EP2 is held at V_{DD}, E2 functions as an active high enable. If EP2 is held to VSS, E2 functions as an active low chip enable input.

Programmability of E2 and E3 allows four banks of depth expansion to be accomplished with no additional logic. By programming the enable inputs of four ΣRAMs in binary sequence(00, 01, 10, 11)and driving the enable inputs with two address inputs. Four Pipelined SigmaRAM can be made to look like one larger RAM to the system.

Deselection of the RAM via $\overline{E1}$ does not deactive the Echo Clocks.

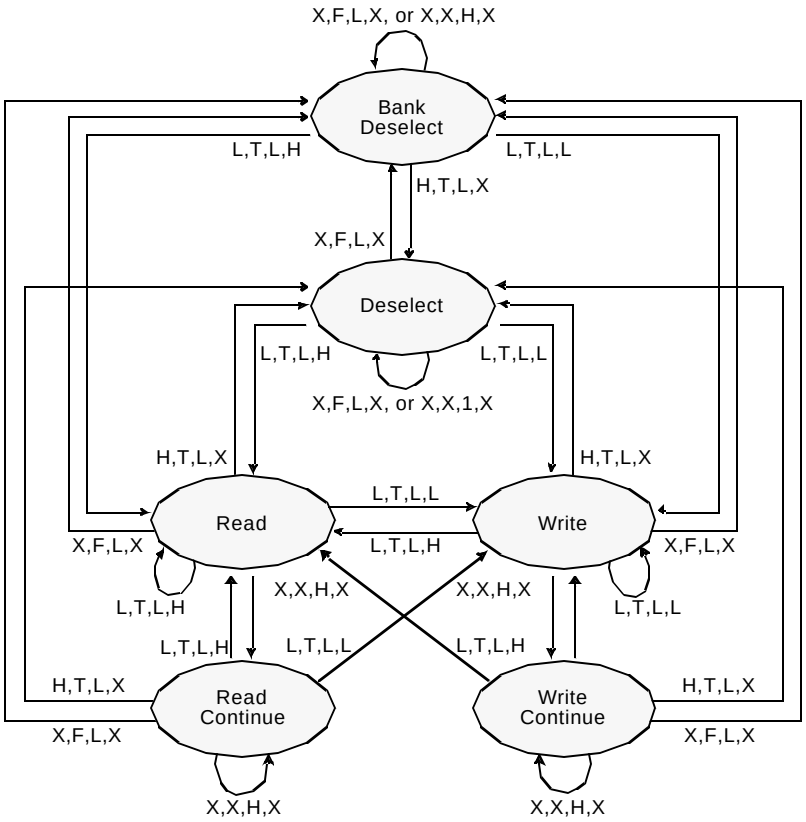
Example Four Bank Depth Expansion Schematic



Bank Enable Truth Table

	EP2	EP3	E2	E3
Bank 0	V_{SS}	V_{SS}	Active Low	Active Low
Bank 1	V_{SS}	V_{DD}	Active Low	Active High
Bank 2	V_{DD}	V_{SS}	Active High	Active Low
Bank 3	V_{DD}	V_{DD}	Active High	Active High

STATE DIAGRAM FOR Pipelined SigmaRAM™



Notes:
1. The notation "X,X,X,X" controlling the state transitions above indicate the states of inputs $\overline{E1}$,E,ADV, and $\overline{WE}$ respectively.
2. If (E2=EP2 and E3=EP3) then E="T" else E="F".
3. "H"=input "high"; "L"=input"low"; "X"=input"don't care"; "T"=input "true"; "F"=input "false".

TRUTH TABLES

Previous Cycle	Input Type	$\overline{E}_1$ (tn)	E (tn)	ADV (tn)	$\overline{WE}$ (tn)	$\overline{BW}$x (tn)	Current Operation	Address	DQ/CQ (tn)	DQ/CQ (tn+1)	Notes
N/A	D	H	T	L	X	X	Deselect Cycle	None	*	Hi-Z/CQ	4
Deselect	C	X	X	H	X	X	Deselect Cycle, Continue	Next	Hi-Z/CQ	Hi-Z/CQ	4
N/A	D	X	F	L	X	X	Bank Deselect Cycle	None	*	Hi-Z	4, 5
Bank Deselect	C	X	X	H	X	X	Bank Deselect Cycle, Continue	Next	Hi-Z	Hi-Z	4 , 5
N/A	R	L	T	L	H	X	Read Cycle, Begin Burst	External	*	Q/CQ	2
Read	C	X	X	H	X	X	Read Cycle, Continue Burst	Next	Q/CQ	Q/CQ	
N/A	W	L	T	L	L	X	Write Cycle, Begin Burst	External	*	D/CQ	2, 3
N/A	W	L	T	L	L	F	Non-Write Cycle, Begin Burst	External	*	*	2, 3
Write	C	X	X	H	X	T	Write Cycle, Continue Burst	Next	D/CQ	D/CQ	3
Write	C	X	X	H	X	F	Non-Write Cycle, Continue Burst	Next	*	D/CQ	3, 4, 5

Note:
1. X=Don't Care, H=High, L=Low.
2. E=T(True) if E2=active and E3=active; E=F(False) if E2=inactive or E3=inactive.
3. "*" indicates that the DQ input requirement / output state and CQ output state are determined by the previous operation.
4. BWx= F(False) if all Byte Write Enable pins are high. BWx=T(True) if any one Byte Write Enable pin is low.
5. DQs are tri-state in response to Bank Deselect, Deselect, and Write commands.
6. Deassertion of E1 does not deactive the echo clock outputs(CQ1,$\overline{CQ1}$, CQ2, $\overline{CQ2}$).

   Echo clock outputs are tri-stated in response to Bank Deselect Commands only.

WRITE TRUTH TABLE

$\overline{WE}$	$\overline{BW}$a	$\overline{BW}$b	$\overline{BW}$c	$\overline{BW}$d	$\overline{BW}$e	$\overline{BW}$f	$\overline{BW}$g	$\overline{BW}$h	OPERATION
H	X	X	X	X	X	X	X	X	READ
L	L	H	H	H	H	H	H	H	WRITE BYTE a
L	H	L	H	H	H	H	H	H	WRITE BYTE b
L	H	H	L	H	H	H	H	H	WRITE BYTE c
L	H	H	H	L	H	H	H	H	WRITE BYTE d
L	H	H	H	H	L	H	H	H	WRITE BYTE e
L	H	H	H	H	H	L	H	H	WRITE BYTE f
L	H	H	H	H	H	H	L	H	WRITE BYTE g
L	H	H	H	H	H	H	H	L	WRITE BYTE h
L	L	L	L	L	L	L	L	L	WRITE ALL BYTEs
L	H	H	H	H	H	H	H	H	WRITE ABORT/NOP

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 2.5	V
Voltage on Any Other Pin Relative to V_{SS}	V_{IN}	-0.3 to VDD+0.3	V
Power Dissipation	P_D	1.6	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

***Note** : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS($0°C \le T_A \le 70°C$)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	1.7	1.8	1.95	V
	V_{DDQ}	1.7	1.8	1.95	V
Ground	V_{SS}	0	0	0	V

***Note** : V_{DD} and V_{DDQ} must be supplied with identical voltage levels.

Selectable Impedance Output Driver DC ELECTRICAL CHARACTERISTICS

The K7N167285A is supplied with selectable (high or low) impedance output buffers.

ZQ=VDDQ

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Low Drive Output Low Voltage	V_{OLL}	I_{OL}=4.0mA	-	0.4	V
Low Drive Output High Voltage	V_{OHL}	I_{OH}=-4.0mA	V_{DDQ} - 0.4	-	V

ZQ=0V

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
High Drive Output Low Voltage	V_{OLH}	I_{OL}= 8.0mA	-	0.4	V
High Drive Output High Voltage	V_{OHH}	I_{OH}=-8.0mA	V_{DDQ} - 0.4	-	V

***Note** : The ZQ level supplied with selectable impedance allows selection between high drive strength (ZQ=Low) and low drive strength (ZQ=High).

CAPACITANCE*(T_A=25°C, f=1MHz)

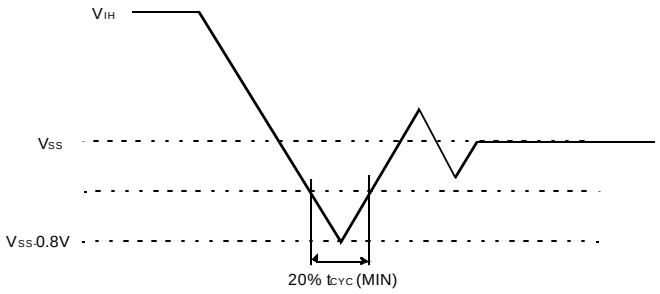
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***Note** : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS (V_{DD}=1.8V + 150/-100mV, T_A=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT	NOTES
Input Leakage Current	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled,		-2	+2	µA	
Operating Current	I_{CC}	V_{DD}=Max , I_{OUT}=0mA Cycle Time ≥ t_{CYC} Min	-30	-	720	mA	1,2
			-27	-	670		
			-25	-	620		
Standby Current	I_{SB1}	E2 or E3 False, I_{OUT}=0mA , f=Max All Inputs≤V_{IL} or ≥V_{IH}		-	120	mA	
	I_{SB2}	$\overline{E1}$ ≥V_{IH}, I_{OUT}=0mA, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	150	mA	
	I_{SB3}	Device deselected, I_{OUT}=0mA, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	50	mA	
Input Low Voltage	V_{IL}			-0.3	0.3*V_{DDQ}	V	3
Input Low Voltage for EP2,EP3,$\overline{SD}$	V_{IL1}			-0.3	0.3	V	
Input High Voltage	V_{IH}			0.7*V_{DDQ}	V_{DD}+0.3	V	3
Input High Voltage for EP2,EP3,$\overline{SD}$	V_{IH1}			V_{DD} - 0.3	V_{DD}+0.3	V	

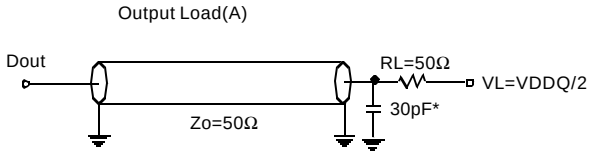
Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V
4. The EP2, EP3 pins must not be changed during operation.



TEST CONDITIONS (T_A=0 to 70°C, V_{DD}=1.8V + 150/-100mV, unless otherwise specified)

PARAMETER	VALUE
Input Pulse Level	0 to 1.8V
Input Rise and Fall Time(Measured at 20% to 80%)	2.0V/ns
Input and Output Timing Reference Levels	0.9V
Output Load	See Fig. 1

AC Test Load Diagram



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS when /SD=VDD (V_{DD}=1.8V + 150/-100mV, T_A=0 to 70°C)

PARAMETER	SYMBOL	-30		-27		-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{KHKH}	3.3	-	3.6	-	4.0	-	ns
Clock High to Output Valid	t_{KHQV}	-	1.8	-	2.0	-	2.1	ns
Clock High to Output High-Z	t_{KHQZ}	0.5	1.8	0.5	2.0	0.5	2.1	ns
Output Hold from Clock High	t_{KHQX}	0.5	-	0.5	-	0.5	-	ns
Clock High to Output Low-Z	t_{KHQX1}	0.5	-	0.5	-	0.5	-	ns
Clock High to CQ High	t_{KHCH}	0.5	1.7	0.5	1.9	0.5	2.0	ns
Clock Low to CQ Low	t_{KLCL}	0.5	1.9	0.5	2.0	0.5	2.3	ns
Output Hold from CQ High	t_{CHQX}	-0.4	-	-0.4	-	-0.5	-	ns
CQ High to Output Low-Z	t_{CHQX1}	-0.4	-	-0.4	-	-0.5	-	ns
CQ High to Output Valid	t_{CHQV}	-	0.4	-	0.4	-	0.5	ns
Clock High to CQ Low-Z	t_{KHCX1}	0.5	-	0.5	-	0.5	-	ns
Clock High to CQ High-Z	t_{KHCZ}	0.5	1.7	0.5	1.9	0.5	2.0	ns
Clock High Pulse Width	t_{KHKL}	1.3	-	1.4	-	1.5	-	ns
Clock Low Pulse Width	t_{KLKH}	1.3	-	1.4	-	1.5	-	ns
Address Setup to Clock High	t_{AVKH}	0.7	-	0.7	-	0.8	-	ns
Chip Enable Setup to Clock High	t_{EVKH}	0.7	-	0.7	-	0.8	-	ns
Write Setup to Clock High($\overline{WE}$, $\overline{BW}$x)	t_{WVKH}	0.7	-	0.7	-	0.8	-	ns
Data Setup to Clock High	t_{DVKH}	0.7	-	0.7	-	0.8	-	ns
Address Advance Setup to Clock High	t_{advVKH}	0.7	-	0.7	-	0.8	-	ns
Address Hold from Clock High	t_{KHAX}	0.4	-	0.4	-	0.5	-	ns
Chip Enable Hold from Clock High	t_{KHEX}	0.4	-	0.4	-	0.5	-	ns
Write Hold from Clock High($\overline{WE}$, $\overline{BW}$x)	t_{KHWX}	0.4	-	0.4	-	0.5	-	ns
Data Hold from Clock High	t_{KHDX}	0.4	-	0.4	-	0.5	-	ns
Address Advance Hold from Clock High	t_{KHadvX}	0.4		0.4		0.5	-	ns

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{E1}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
3. A write cycle is defined by WE low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{WE}$ High with ADV Low, Both cases must meet setup and hold times.
4. To avoid bus contention, At a given voltage and temperature t_{KHQX1} is more than t_{KHQZ}.
The specs as shown do not imply bus contention because t_{KHQX1} is a Min. parameter that is worst case at totally different test conditions (0°C,1.95V) than t_{KHQZ}, which is a Max. parameter(worst case at 70°C,1.7V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

AC TIMING CHARACTERISTICS when /SD=VSS (V_{DD}=1.8V + 150/-100mV, T_A=0 to 70°C)

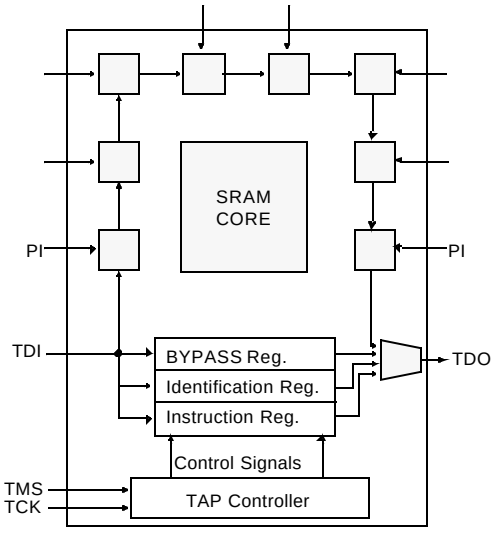
PARAMETER	SYMBOL	-30		-27		-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{KHKH}	3.3	-	3.6	-	4.0	-	ns
Clock High to Output Valid	t_{KHQV}	-	2.7	-	2.9	-	3.0	ns
Clock High to Output High-Z	t_{KHQZ}	1.4	2.7	1.4	2.9	1.4	3.0	ns
Output Hold from Clock High	t_{KHQX}	1.4	-	1.4	-	1.4	-	ns
Clock High to Output Low-Z	t_{KHQX1}	1.4	-	1.4	-	1.4	-	ns
Clock High to CQ High	t_{KHCH}	1.4	2.6	1.4	2.8	1.4	2.9	ns
Clock Low to CQ Low	t_{KLCL}	1.4	2.8	1.4	2.9	1.4	3.2	ns
Output Hold from CQ High	t_{CHQX}	-0.4	-	-0.4	-	-0.5	-	ns
CQ High to Output Low-Z	t_{CHQX1}	-0.4	-	-0.4	-	-0.5	-	ns
CQ High to Output Valid	t_{CHQV}	-	0.4	-	0.4	-	0.5	ns
Clock High to CQ Low-Z	t_{KHCX1}	1.4	-	1.4	-	1.4	-	ns
Clock High to CQ High-Z	t_{KHCZ}	1.4	2.6	1.4	2.8	1.4	2.9	ns
Clock High Pulse Width	t_{KHKL}	1.3	-	1.4	-	1.5	-	ns
Clock Low Pulse Width	t_{KLKH}	1.3	-	1.4	-	1.5	-	ns
Address Setup to Clock High	t_{AVKH}	0.7	-	0.7	-	0.8	-	ns
Chip Enable Setup to Clock High	t_{EVKH}	0.7	-	0.7	-	0.8	-	ns
Write Setup to Clock High($\overline{W}$, $\overline{BW}$x)	t_{WVKH}	0.7	-	0.7	-	0.8	-	ns
Data Setup to Clock High	t_{DVKH}	0.7	-	0.7	-	0.8	-	ns
Address Advance Setup to Clock High	t_{advVKH}	0.7	-	0.7	-	0.8	-	ns
Address Hold from Clock High	t_{KHAX}	0.4	-	0.4	-	0.5	-	ns
Chip Enable Hold from Clock High	t_{KHEX}	0.4	-	0.4	-	0.5	-	ns
Write Hold from Clock High($\overline{W}$, $\overline{BW}$x)	t_{KHWX}	0.4	-	0.4	-	0.5	-	ns
Data Hold from Clock High	t_{KHDX}	0.4	-	0.4	-	0.5	-	ns
Address Advance Hold from Clock High	t_{KHadvX}	0.4		0.4		0.5	-	ns

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and $\overline{E1}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
3. A write cycle is defined by W low having been registered into the device at ADV Low, A Read cycle is defined by $\overline{W}$ High with ADV Low, Both cases must meet setup and hold times.
4. To avoid bus contention, At a given voltage and temperature t_{KHQX1} is more than t_{KHQZ}.
The specs as shown do not imply bus contention because t_{KHQX1} is a Min. parameter that is worst case at totally different test conditions (0°C,1.95V) than t_{KHQZ}, which is a Max. parameter(worst case at 70°C,1.7V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



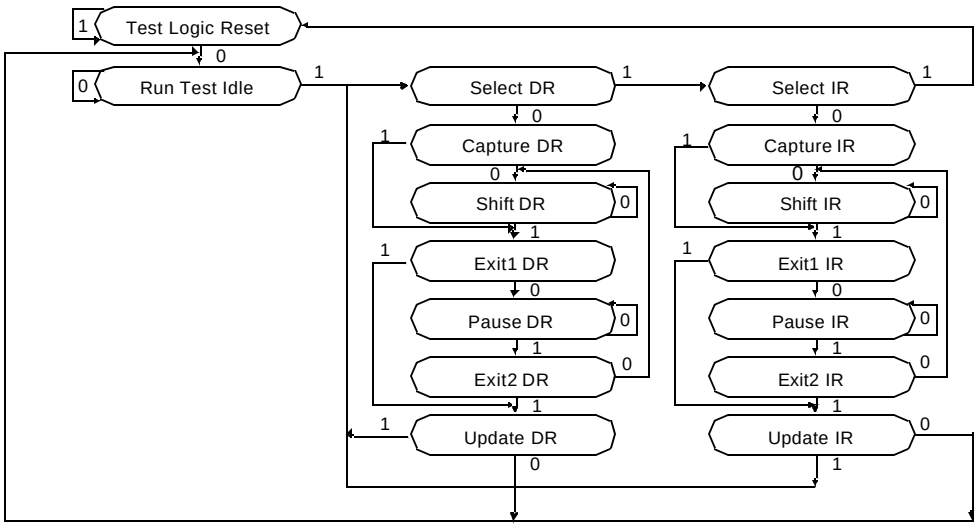
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	RFU	Reserved for future use	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	RFU	Reserved for future use	3
1	1	0	RFU	Reserved for future use	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
256Kx72	3 bits	1 bits	32 bits	119 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
256Kx72	0000	00110 00101	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER(x72)

1	6W	A0		DQf	11H	36
2	6V	A1		DQf	10H	37
3	6U	A		DQf	10G	38
4	7V	A		DQf	11G	39
5	7U	NC		DQf	11F	40
6	7W	A		DQf	10F	41
7	8U	A		DQPf	10E	42
8	8V	A		DQPb	11E	43
9	9V	A		DQb	11D	44
10	10W	DQe		DQb	10D	45
11	11W	DQe		DQb	10C	46
12	11V	DQe		DQb	11C	47
13	10V	DQe		DQb	11B	48
14	10U	DQe		DQb	10B	49
15	11U	DQe		DQb	10A	50
16	11T	DQe		DQb	11A	51
17	10T	DQe		$\overline{BW}$a	9C	52
18	11R	DQPe		$\overline{BW}$f	9B	53
19	10R	DQPa		A	9A	54
20	10P	DQa		$\overline{BW}$e	8C	55
21	11P	DQa		$\overline{BW}$b	8B	56
22	11N	DQa		E3	8A	57
23	10N	DQa		A	7B	58
24	10M	DQa		A	7A	59
25	11M	DQa		EP3	6H	60
26	11L	DQa		EP2	6G	61
27	10L	DQa		NC	6D	62
28	11K	CQ1		$\overline{E1}$	6C	63
29	6M	NC		$\overline{WE}$	6B	64
30	6L	NC		ADV	6A	65
31	6J	NC		NC	5C	66
32	6F	ZQ		A	5A	67
33	10K	$\overline{CQ}$1		$\overline{BW}$d	4C	68
34	10J	DQf		$\overline{BW}$g	4B	69
35	11J	DQf		E2	4A	70

71	3C	$\overline{BW}$h		DQd	1T	106
72	3B	$\overline{BW}$c		DQd	2T	107
73	3A	A		DQd	2U	108
74	2A	DQg		DQd	1U	109
75	1A	DQg		DQd	1V	110
76	1B	DQg		DQd	2V	111
77	2B	DQg		DQd	2W	112
78	2C	DQg		DQd	1W	113
79	1C	DQg		A	3V	114
80	1D	DQg		A	4V	115
81	2D	DQg		A	4U	116
82	1E	DQPg		NC	5U	117
83	2E	DQPc		A	5V	118
84	2F	DQc		A	5W	119
85	1F	DQc				
86	1G	DQc				
87	2G	DQc				
88	2H	DQc				
89	1H	DQc				
90	1J	DQc				
91	2J	DQc				
92	1K	CQ2				
93	3K	CK				
94	4K	NC				
95	2K	$\overline{CQ2}$				
96	2L	DQh				
97	1L	DQh				
98	1M	DQh				
99	2M	DQh				
100	2N	DQh				
101	1N	DQh				
102	1P	DQh				
103	2P	DQh				
104	2R	DQPh				
105	1R	DQPd				

NOTE, NC ; Don't Care

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	1.8	1.95	V	
Input High Level	V_{IH}	1.05	-	V_{DD}+0.3	V	1
Input Low Level	V_{IL}	-0.3	-	0.7	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	1.5	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.45	V	

***Note** : 1. In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}$+0.3V

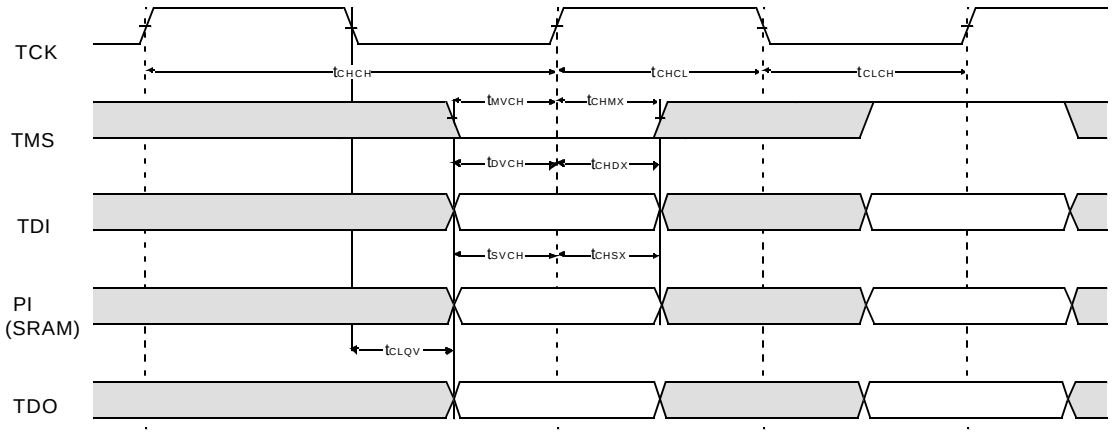
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.8/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		0.9	V	

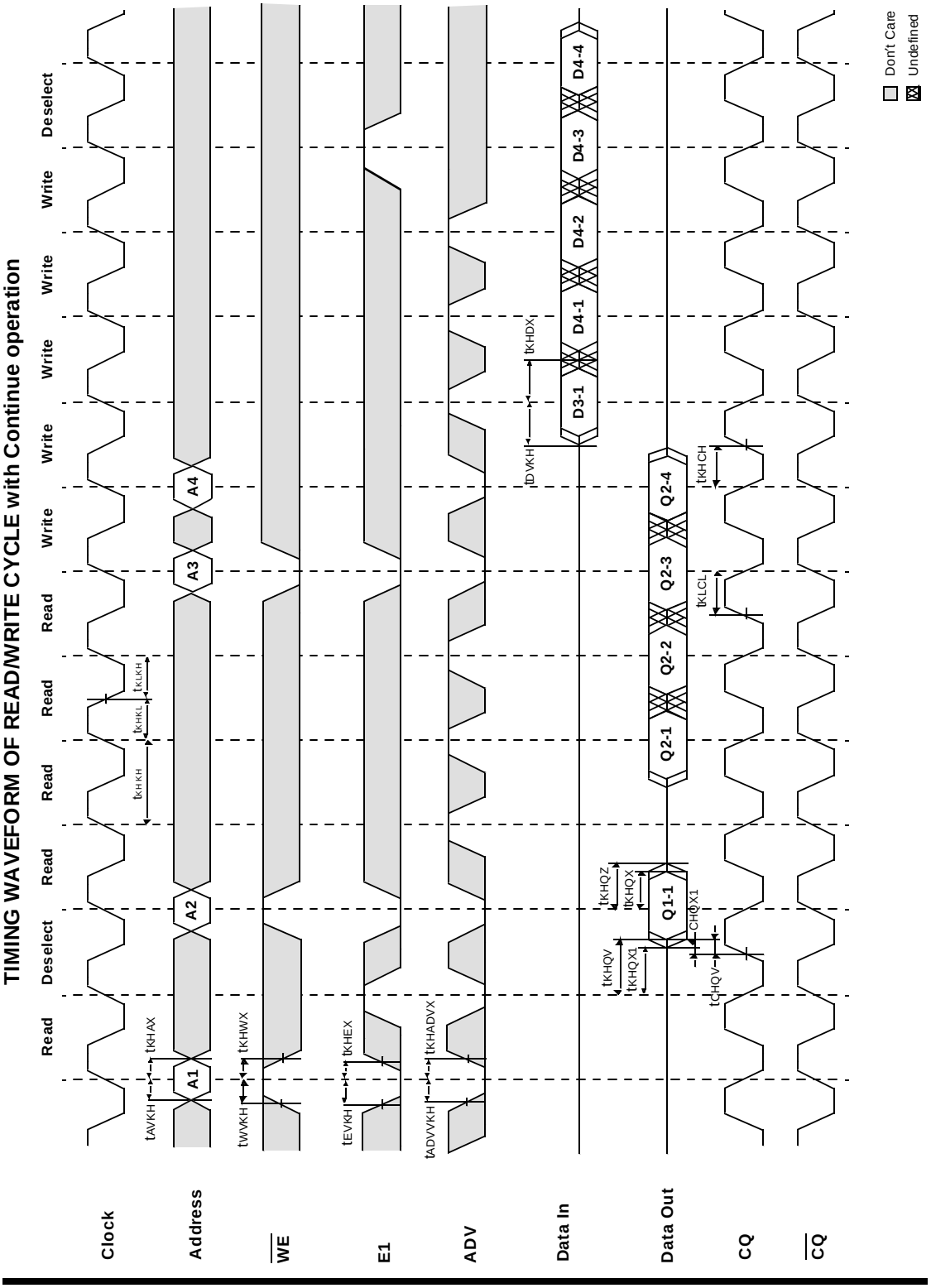
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	20	-	ns	
TCK High Pulse Width	t_{CHCL}	10	-	ns	
TCK Low Pulse Width	t_{CLCH}	10	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

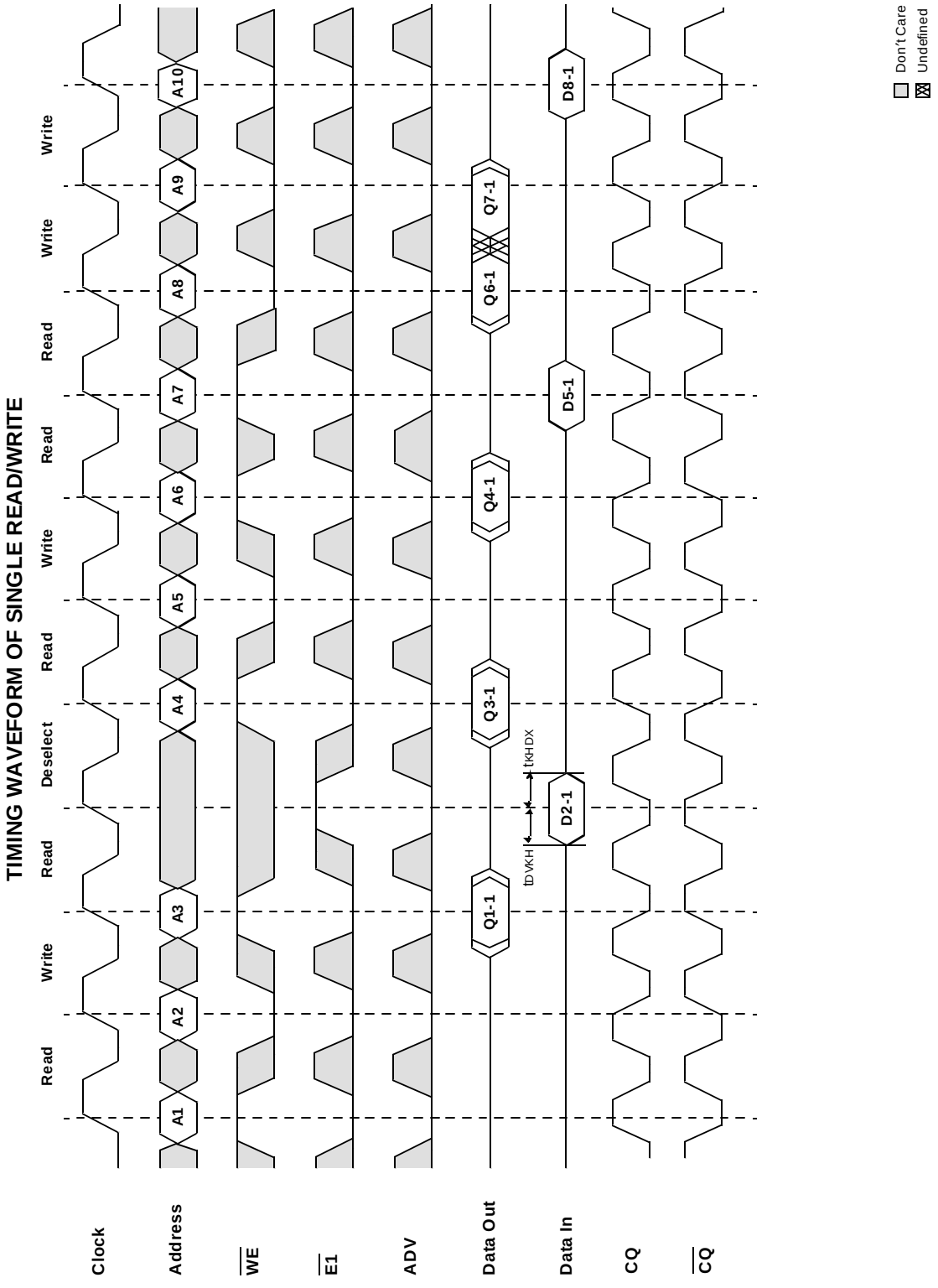
JTAG TIMING DIAGRAM



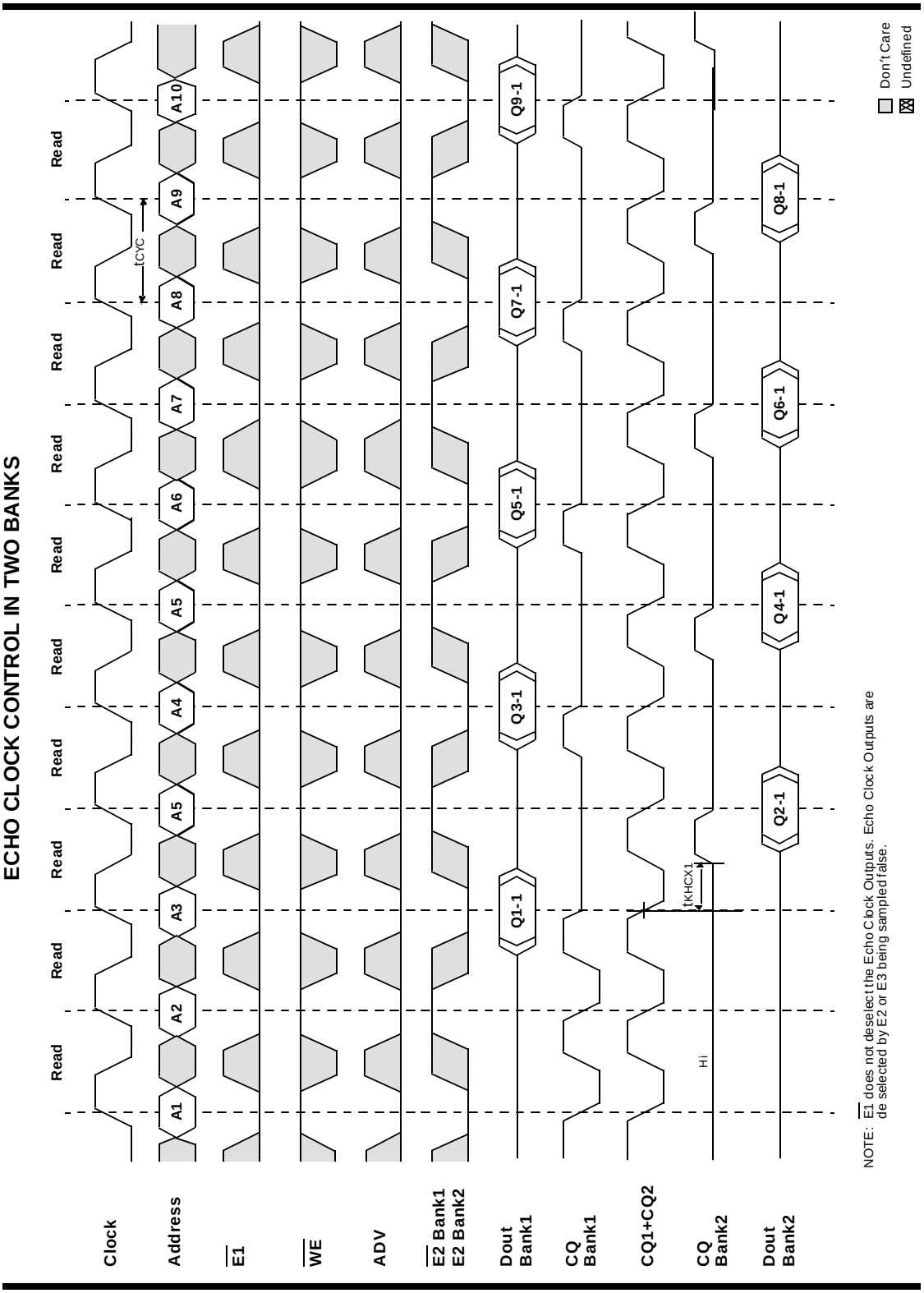
TIMING WAVEFORM OF READ/WRITE CYCLE with Continue operation



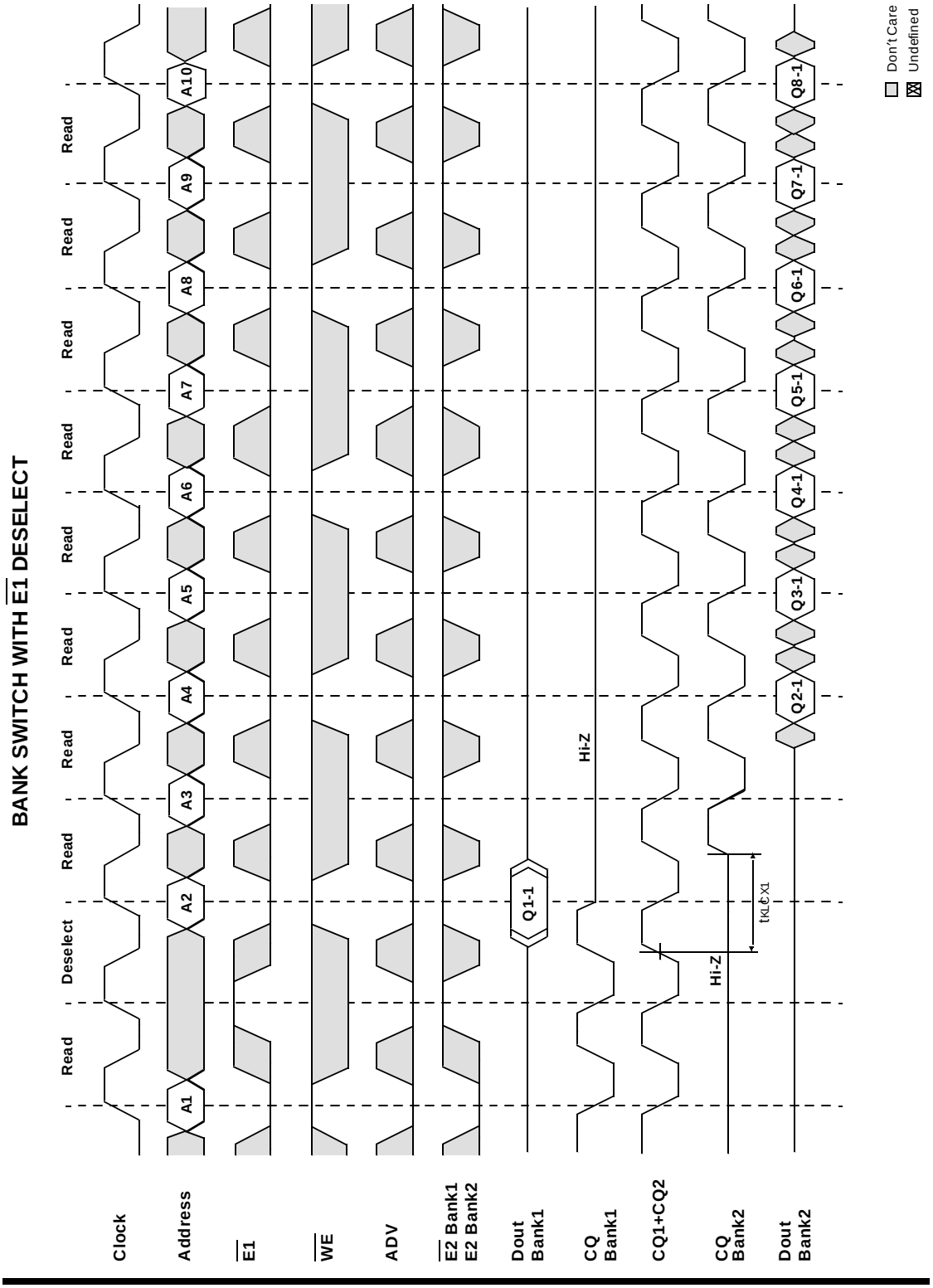
TIMING WAVEFORM OF SINGLE READ/WRITE



ECHO CLOCK CONTROL IN TWO BANKS

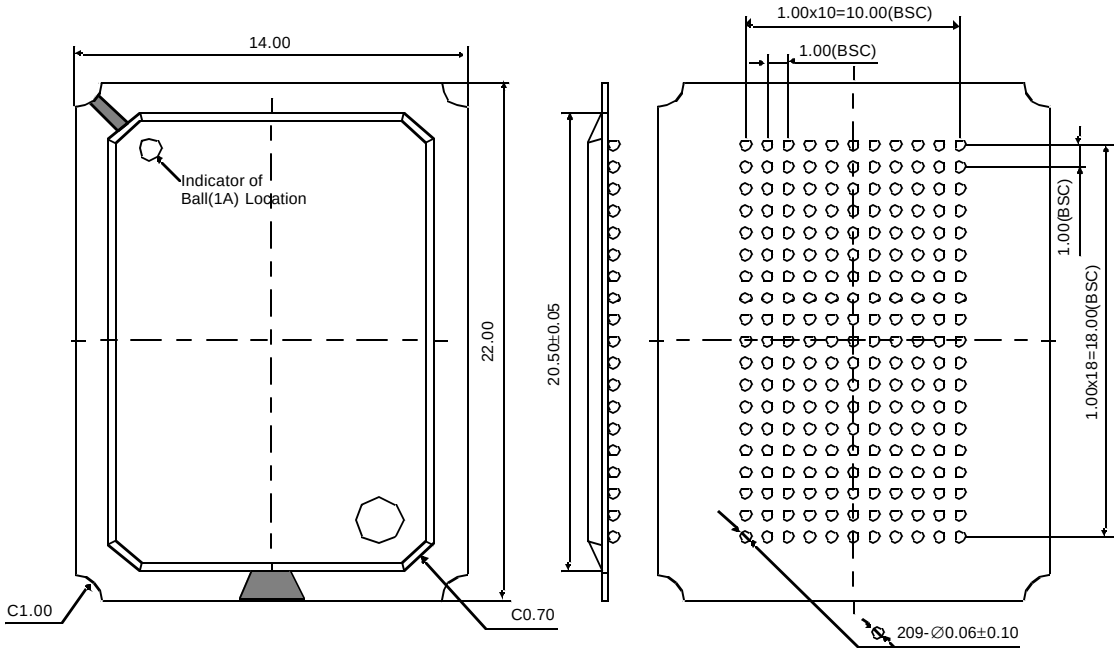


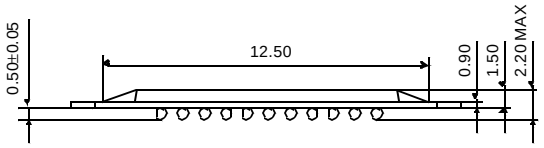
BANK SWITCH WITH $\overline{E1}$ DESELECT



209 Bump BGA PACKAGE DIMENSIONS

14mm x 22mm Body, 1.0mm Bump Pitch, 11x19 Bump Array





NOTE:

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset: 0.10 MAX.
3. PCB to Cavity Offset: 0.10 MAX.