μPD7520x/7521x/75CG2xx/75P216A 4-Bit Microcomputers With FIP (VF) Controller/Driver

Description

The μPD7520x/7521x is a family of single-chip CMOS microcomputers containing CPU, ROM, RAM, I/O ports, several timer/counters, vectored interrupts, a FIP® controller/driver, subsystem clock, and serial interface.

The instruction set allows the user to manipulate RAM data and I/O ports in 1-, 4-, and 8-bit units. The devices are ideally suited for controlling VCRs, microwave ovens, electronic stoves, washing machines, electronic cash registers, audio equipment, and meters.

Both EPROM and OTP versions are available. Refer to the ordering information.

Features

- 136 instructions
  - Bit manipulation
  - 4-bit and 8-bit transfer, arithmetic, logical comparison, and increment/decrement instructions
  - 1-byte relative branch
  - GETI instruction, to convert one 2-byte or 3-byte or two 1-byte instructions into a single 1-byte instruction
- Fast execution time (@ 4.19 MHz)
  - High-speed cycle: 0.95 μs
  - Lower-voltage cycles: 1.91 and 15.3 μs
- Program ROM
  - μPD75206: 6016 bytes
  - μPD75208/CG208A: 8064 bytes
  - μPD75212A: 12160 bytes
  - μPD75216A/CG216A/P216A: 16256 bytes
- Data memory (RAM)
  - μPD75206: 369 x 4 bits
  - μPD75208/CG208A: 497 x 4 bits
  - μPD75212A/216A/CG216A/P216A: 512 x 4 bits
  - Allows operation on 1, 4, or 8 bits
- Four banks of eight 4-bit registers
- Accumulators
  - 1-bit (CY)
  - 4-bit (A)
  - 8-bit (XA)
- 28 port lines
  - 20 I/O lines; 8 outputs directly drive LEDs (I_{sink} = 15 mA rms)
  - 8 input-only lines
- One external event input
- Four timers
  - 8-bit basic interval timer
  - 8-bit timer/event counter
  - 14-bit watch timer with buzzer output
  - 14-bit PWM timer
- Programmable FIP controller/driver with memory area
  - Up to 16 segments
  - Up to 16 digits
  - Eight dimming levels
  - Key scan interrupt generation
- 8-bit serial interface
  - Data transfer can be full duplex or receive only, and can be MSB or LSB first
- Vectored interrupts
  - Two-level nesting
  - Three external interrupts
  - Five internal interrupts
  - One input which generates an interrupt request
- Standby modes
  - HALT mode: stops CPU only
  - STOP mode: stops main system clock
- Operates with crystal or ceramic resonator
- CMOS operation with V_{DD} from 2.7 to 6.0 V
- Low current (V_{DD} = 5 V; f_{xx} = 4.19 MHz)
  - Normal operation: 3.0 mA typical
  - HALT mode: 0.6 mA typical
  - STOP mode: 0.1 μA typical
- Mask options
  - Power-on reset circuit and power-on flag (always in μPD75CG208A, μPD75CG216A, μPD75P216A)
  - Port 6 input pull-down resistor
  - FIP output pins have pull-down resistor
- Programmable versions
  - Piggyback ROM: μPD75CG208A/CG216A
  - OTP: μPD75P216A
- Available in 64-pin SDIP or QFP

FIP is a registered trademark of NEC Corporation

Ordering Information

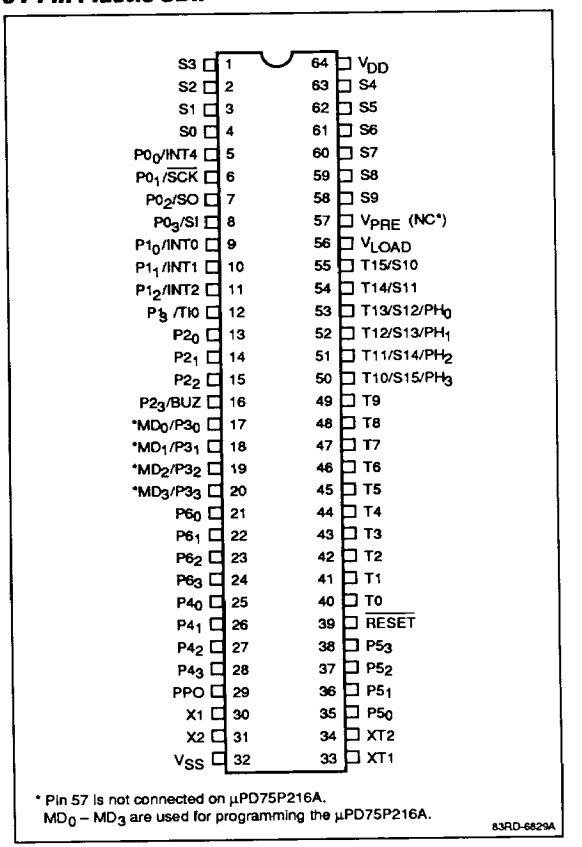
Part Number	Package Type	ROM Type
μPD75206CW-xxx	64-pin plastic SDIP	Mask ROM
μPD75206G-xxx-1B	64-pin plastic QFP (resin thickness 2.05 mm)	
μPD75206GF-xxx-3BE	64-pin plastic QFP (resin thickness 2.7 mm)	
μPD75208CW-xxx	64-pin plastic SDIP	Mask ROM
μPD75208G-xxx-1B	64-pin plastic QFP (resin thickness 2.05 mm)	
μPD75208GF-xxx-3BE	64-pin plastic QFP (resin thickness 2.7 mm)	
μPD75CG208E	64-pin ceramic SDIP	Piggyback EPROM
μPD75CG208EA	64-pin ceramic QFP	
μPD75212ACW-xxx	64-pin plastic SDIP	Mask ROM
μPD75212AGF-xxx-3BE	64-pin plastic QFP	
μPD75216ACW-xxx	64-pin plastic SDIP	
μPD75216AGF-xxx-3BE	64-pin plastic QFP	
μPD75CG216AE	64-pin ceramic SDIP	Piggyback EPROM
μPD75CG216AEA	64-pin ceramic QFP	
μPD75P216ACW	64-pin plastic SDIP	OTP

Notes:

(1) xxx indicates ROM code suffix

Pin Configurations

64-Pin Plastic SDIP

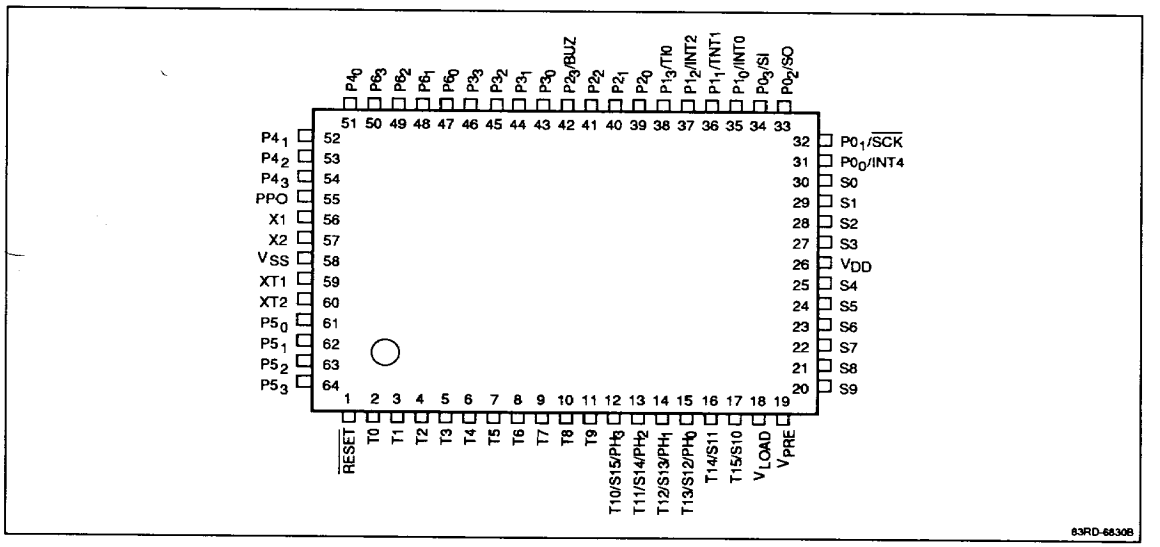


* Pin 57 is not connected on μPD75P216A.
MD_0 – MD_3 are used for programming the μPD75P216A.

83RD-6629A

Pin Configurations (cont)

64-Pin Plastic QFP



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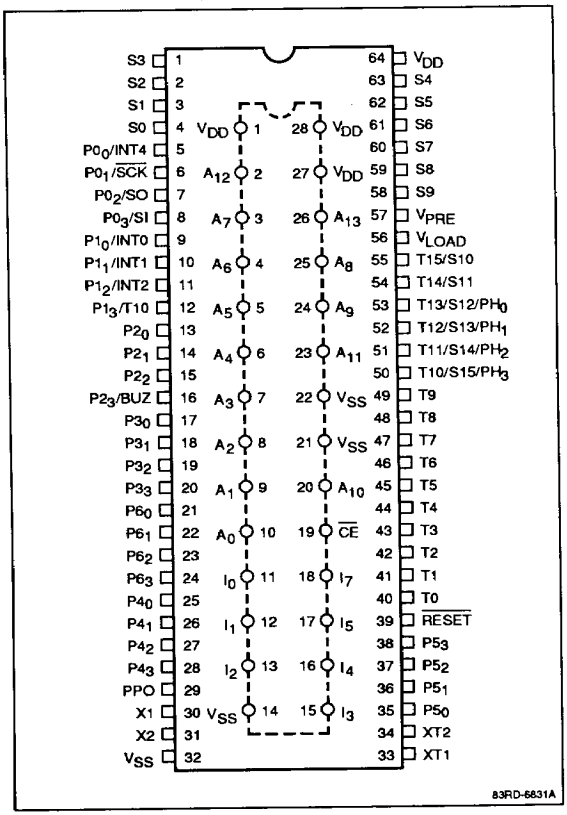
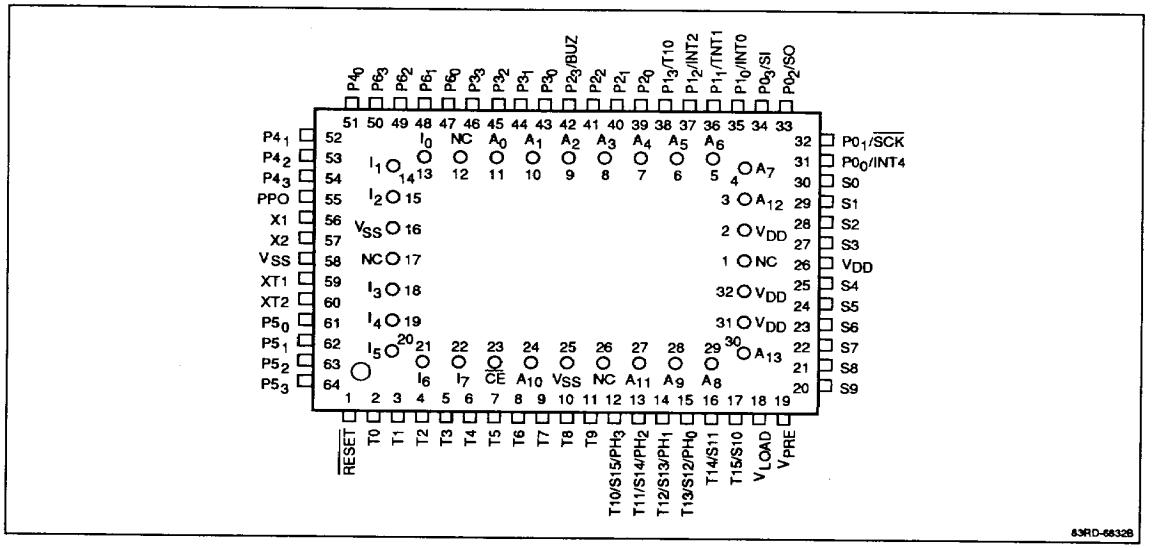
Pin Configurations (cont)

64-Pin Ceramic Piggyback SDIP



Pin Configurations (cont)

64-Pin Ceramic Piggyback QFP



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Pin Identification

Symbol	Function
$P0_0$/INT4	Port 0 input; interrupt 4
$P0_1$/$\overline{SCK}$	Port 0 input; serial clock
$P0_2$/SO	Port 0 input; serial out
$P0_3$/SI	Port 0 input; serial in
$P1_0$/INT0	Port 1 input; interrupt 0
$P1_1$/INT1	Port 1 input; interrupt 1
$P1_2$/INT2	Port 1 input; interrupt 2
$P1_3$/TI0	Port 1 input; timer 0 input
$P2_0$-$P2_2$	Port 2 I/O
$P2_3$/BUZ	Port 2 I/O; buzzer output
$P3_0$-$P3_3$/MD0-MD3	Port 3 I/O; OTP operation mode (μPD75P216A)
$P4_0$-$P4_3$	Port 4 I/O
$P5_0$-$P5_3$	Port 5 I/O
$P6_0$-$P6_3$	Port 6 I/O
PH_0/T13/S12	Port H output; digit select line; segment line
PH_1/T12/S13	Port H output; digit select line; segment line
PH_2/T11/S14	Port H output; digit select line; segment line
PH_3/T10/S15	Port H output; digit select line; segment line
PPO	Pulse output
$\overline{RESET}$	Reset input
S0-S9	FIP segment outputs
T0-T9	FIP digit select outputs
T14/S11 T15/S10	Digit selects T14 and T15; segment lines S10 and S11
V_{DD}	Positive power supply
V_{LOAD}	FIP high-voltage negative supply voltage
V_{PRE}	FIP predriver negative supply voltage
V_{SS}	Ground
X1, X2	Main clock inputs
XT1, XT2	Subsystem clock inputs

PIN FUNCTIONS

$P0_0$-$P0_3$, INT4, $\overline{SCK}$, SO, SI (Port 0, Interrupt 4, Serial Clock, Serial In/Out)

These pins can be used as 4-bit input port 0. $P0_0$ can also be used for vectored interrupt 4, which interrupts on either the leading edge or the trailing edge of the signal. $P0_1$-$P0_3$ may also be used for the serial interface under the control of the SIOM register. SI is the serial input, SO is the serial output, and $\overline{SCK}$ is the serial clock. Reset causes these pins to default to the port 0 input mode.

$P1_0$-$P1_3$, INT0-INT2, TI0 (Port 1, Interrupts, Timer Input)

These pins can be used as 4-bit input port 1. $P1_0$ and $P1_1$ can also be used for edge-triggered interrupts INT0 and INT1. $P1_2$ can be used for INT2, which is also an edge-triggered input, but one which generates an interrupt request and does not cause an interrupt. $P1_3$ can be used as an input clock to the timer/event counter to count external events. Reset causes these pins to default to the port 1 input mode.

$P2_0$-$P2_3$, BUZ (Port 2, Buzzer Output)

These pins can be used as 4-bit I/O port 2. When used as an output the data is latched. When used as an input port the port outputs are three-state. $P2_3$ can also be used to output square waves for a buzzer. Reset causes these pins to default to the port 2 input mode.

$P3_0$-$P3_3$ (MD0-MD3) (Port 3)

These pins are used for input/output port 3. Each bit in this port can be independently programmed to be either an input or output. This port has latched outputs. MD0 through MD3 are used for the μPD75P216A OTP program memory write and verify mode to select the operation mode. A reset causes this port to be in the input mode.

$P4_0$-$P4_3$ (Port 4)

These pins are used for input/output port 4; this port has latched outputs. Port 4 outputs can directly drive an LED. Ports 4 and 5 can be paired together to function as one 8-bit port. A reset causes this port to be in the input mode.

$P5_0$-$P5_3$ (Port 5)

These pins are used for input/output port 5; this port has latched outputs and its outputs can directly drive an LED. Ports 4 and 5 can be paired together to function as one 8-bit port. A reset causes this port to be in the input mode.

$P6_0$-$P6_3$ (Port 6)

Port 6 is a 4-bit I/O port. Outputs are latched, and each bit can be independently programmed to be either an input or an output. Port 6 can have pull-down resistors added as a mask option. A reset signal causes this port to default to the input mode.

PH_0-PH_3, T10-T13, S12-S15 (Port H, Digit Select, Segment Lines)

Port H is a 4-bit output-only port, with P-channel open-drain outputs capable of directly driving LEDs. Pull-down resistors can be selected as a mask-option. Alternatively, these pins can be used as high voltage digit/segment outputs. A reset signal causes this port to default to the high-impedance state; if mask-option resistors are present the output goes low.

S0-S9 (Segment Lines)

These are high-voltage outputs used as FIP controller segment lines. Pull-down resistors can be selected as a mask-option. A reset signal sets these pins to the high-impedance state; if mask-option resistors are present the outputs go low.

T0-T9 (FIP Digit Select)

These are high-voltage outputs used as FIP controller digit select timing signals. Pull-down resistors can be selected as a mask-option. A reset signal sets these pins to the high-impedance state; if mask-option resistors are present the outputs go low.

T14/S11, T15/S10 (Digit Select/Segment Lines)

These two pins provide additional digit select or segment lines. When not used for the display they can be used as static outputs. Internal pull-down resistors are available as a mask option.

PPO (Timer/Pulse Generator Output)

This is an output signal from the timer/pulse generator, and can be either PWM (Pulse Width Modulated) or a square wave. This pin can also be used as a 1-bit output port. Pin assumes a high impedance state upon reset.

X1, X2 (System Clock Inputs)

These pins are the main system clock inputs. The clock can be either a ceramic or crystal resonator; an external logic signal may also be used as a clock source.

XT1, XT2 (Subsystem Clock Inputs)

These pins are the subsystem clock inputs. The clock can be either a ceramic or crystal resonator; an external logic signal may also be used as a clock source.

$\overline{\text{RESET}}$ (Reset)

This is the reset input, and it is active low.

V_{PRE} (Predriver Power)

This is the power supply for the predrivers of the FIP controller/driver.

V_{LOAD} (FIP Power Supply)

This pin is used to supply power to the output drivers for the segment lines and digit select pins of the FIP controller/driver.

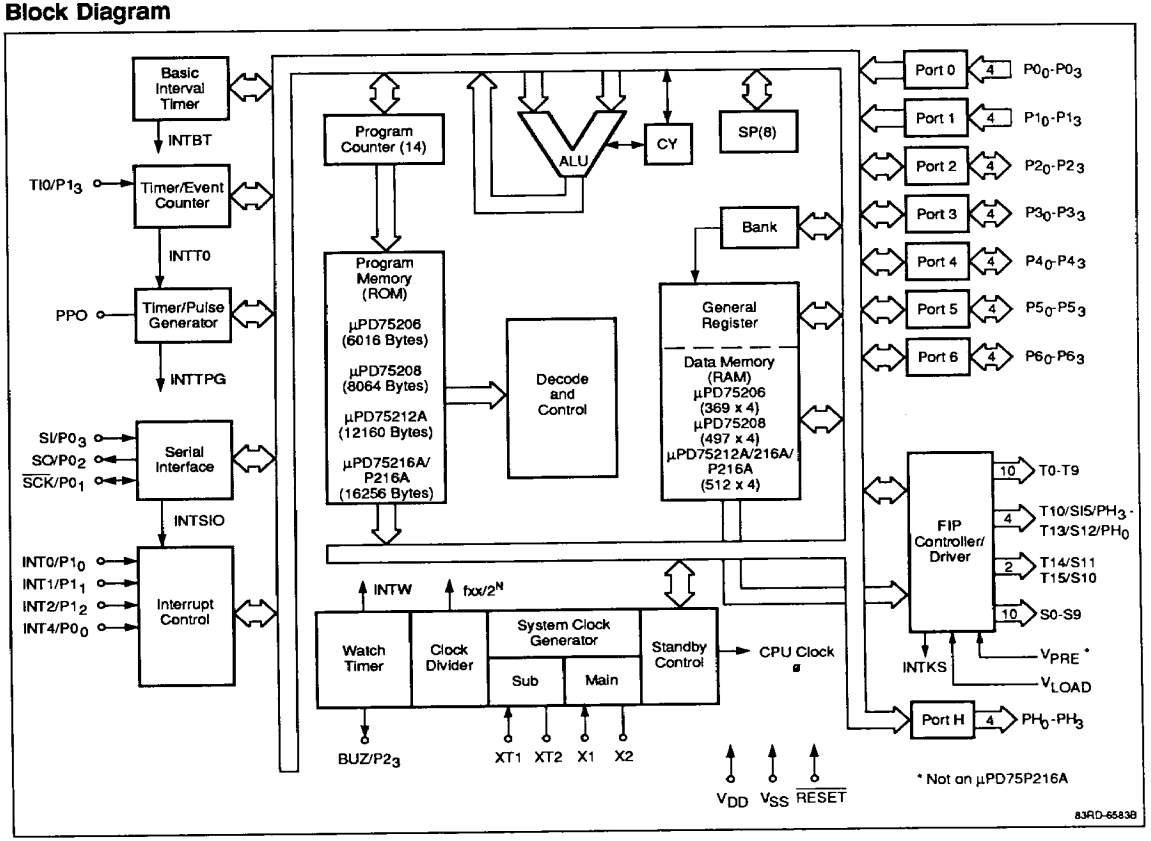
V_{DD} (Power Supply)

The system positive power supply pin.

V_{SS} (Ground)

System ground.

Block Diagram



Product Comparison

Item	μPD75CG208	μPD75CG216A	μPD75206	μPD75208	μPD75212A	μPD75216A	μPD75P216A
Program memory (ROM)	Piggyback EPROM 0000H–1FFFH 8192 x 8 bits	Piggyback EPROM 0000H–3FFFH 16384 x 8 bits	Mask ROM 0000H–177FH 6016 x 8 bits	Mask ROM 0000H–1F7FH 8064 x 8 bits	Mask ROM 0000H–2F7FH 12160 x 8 bits	Mask ROM 0000H–3F7FH 16256 x 8 bits	OTP 000H-3F7FH 16256 x 8 bits
Data memory (RAM)	497 x 4 bits	512 x 4 bits	369 x 4 bits	497 x 4 bits	512 x 4 bits	512 x 4 bits	512 x 4 bits
Port 6 pull-down resistor	None	None	Mask option (each bit)	Mask option (each bit)	Mask option (each bit)	Mask option (each bit)	None
S0-S8, T0-T9	On-chip pull-down resistor		Each bit can be mask programmed either for a pull-down resistor or as an open drain output				On-chip pull-down resistor
S9, T10-T15	Open drain	Open drain	Each bit can be mask programmed either for a pull-down resistor or as an open drain output				Open drain
Number of FIP segments	19 - 12	9 - 16	9 - 12	9 - 12	9 - 16	9 - 16	9-16
Power-on reset circuitry	On-chip	On-chip	Mask option	Mask option	Mask option	Mask option	None
Low-power data retention	Not provided	Not provided	2 volts	2 volts	2 volts	2 volts	Not provided
Operating voltage range	5 V ± 10%	5 V ± 10 %	2.7 to 6.0 V	2.7 to 6.0 V	2.7 to 6.0 V	2.7 to 6.0 V	5 V ±10%
Package	64-pin piggyback ceramic shrink DIP with window. 64-pin piggyback ceramic QFP with window.		64-pin plastic shrink DIP 64-pin plastic QFP				64-pin plastic shrink DIP

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (All Parts)

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Supply voltage, V_{LOAD}	V_{DD}−40 to V_{DD}+0.3 V
Supply voltage, V_{PRE} (Note 1)	V_{DD}−12 to V_{DD}+0.3 V
Supply voltage, V_{PP} (Note 2)	−0.3 to +13.5 V
Input voltage, V_I	−0.3 to V_{DD} + 0.3 V
Output voltage, V_O (other than display)	−0.3 to V_{DD} + 0.3 V
Output voltage, V_{OD} (display pins)	V_{DD}−40 to V_{DD}+0.3 V
High-level output current, I_{OH} (single pin; other than display)	−15 mA
High-level output current, I_{OH} (single pin; S0-S9)	−15 mA
High-level output current, I_{OH} (single pin; T0-T15)	−30 mA
High-level output current, I_{OH} (total of all pins other than display)	−20 mA
High-level output current, I_{OH} (total of all display outputs)	−120 mA
Low-level output current, I_{OL} (single pin)	17 mA
Low-level output current, I_{OL} (total of all pins)	60 mA
Power dissipation, P_T (Plastic QFP)	450 mW
Power dissipation, P_T (Plastic SDIP)	600 mW
Storage temperature, t_{STG}	−65 to + 150°C
Operating temperature, t_{OPT} (Note 3)	−40 to +85°C
Operating temperature, t_{OPT} (Note 4)	−10 to +70°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Notes:

(1) Does not apply to μPD75P216A.

(2) For μPD75P216A only.

(3) For mask ROM parts.

(4) For μPD75CG208/CG216A/P216A.

Capacitance (All Parts)

V_{DD} = 0 V; T_A = 25°C

Parameter	Symbol	Max	Unit	Conditions
Input capacitance	C_{IN}	15	pF	f = 1 MHz; all unmeasured pins returned to ground
Output capacitance; other than display	C_{OUT1}	15	pF	
Output capacitance; display only	C_{OUT2}	35	pF	
I/O capacitance	C_{IO}	15	pF	

Operating Supply Voltage

Mask ROM parts: T_A = −40 to +85°C

Programmable parts: T_A = −10 to +70°C

Parameter	Min	Max	Unit	Conditions
CPU (Note 2)	(Note 3)	6.0	V	(Note 4)
	4.5	5.5	V	μPD75CG208/CG216A and μPD75P216A only
Display controller	4.5	6.0	V	(Note 4)
	4.5	5.5	V	μPD75CG208/CG216A, μPD75P216A only
Timer/pulse generator	4.5	6.0	V	(Note 4)
	4.5	5.5	V	μPD75CG208/CG216A and μPD75P216A only
Other hardware (Note 2)	2.7	6.0	V	(Note 4)
	4.5	5.5	V	μPD75CG208/CG216A and μPD75P216A only

Notes:

(1) Care must be taken when designing the microcomputer that the total power dissipation does not exceed the maximum allowable. Power is dissipated in three areas:
   a. At the CPU. PD is calculated by the product of V_{DD} (max) and I_{DD1} (max).
   b. By the output pins. Total power dissipation is the sum of the values for each pin when maximum current is applied.
   c. By the pull-down resistors.

(2) The CPU does not include the system clock oscillator, the display controller, or the timer/pulse generator.

(3) Varies according to the cycle time. See AC Characteristics.

(4) Mask ROM parts only.

Main System Clock Oscillator Characteristics

Mask ROM parts: $T_A = -40$ to $+85°C$; $V_{DD} = 2.7$ to 6.0 V
Programmable parts: $T_A = -10$ to $+70°C$; $V_{DD} = 4.5$ to 5.5 V

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Ceramic resonator (Figure 1A)	Oscillation frequency (Note 1)	f_{XX}	2.0		5.0	MHz	(Note 5)
	Oscillation stabilization time (Note 2)				4 (Note 3)	ms	After V_{DD} reaches the minimum oscillation voltage
Crystal resonator (Figure 1A)	Oscillation frequency (Note 1)	f_{XX}	2.0	4.19	5.0	MHz	(Note 5)
	Oscillation stabilization time (Note 2)				10 (Note 3)	ms	(Note 4)
					30 (Note 3)	ms	(Note 5)
External clock (Figure 1B)	X1 input frequency (Note 1)	f_{XX}	2.0		5.0	MHz	(Note 5)
	X1 input low- and high-level width	t_{XH}, t_{XL}	100		250	ns	

Notes:

(1) The oscillation frequency and X1 input frequency are included only to show the characteristics of the oscillators. Refer to the AC Characteristics table for actual instruction execution times.

(2) The oscillation stabilization time is the time required for the oscillator to stabilize after voltage V_{DD} is applied and reaches the V_{DD} spec or the STOP mode is released.

(3) Values shown are for the recommended resonators. Values for resonators not shown in this data sheet should be obtained from the manufacturer's specification sheets.

(4) $V_{DD} = 4.5$ to 6.0 V for mask ROM parts and $V_{DD} = 4.5$ to 5.5 V for programmable parts.

(5) $V_{DD} = 2.7$ to 6.0 V for mask ROM parts and $V_{DD} = 4.5$ to 5.5 V for programmable parts.

Subsystem Clock Oscillator Characteristics

Mask ROM parts: $T_A = -40$ to $+85°C$; $V_{DD} = 2.7$ to 6.0 V
Programmable parts: $T_A = -10$ to $+70°C$; $V_{DD} = 4.5$ to 5.5 V

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal resonator (Figure 2A)	Oscillation frequency	f_{XT}	32	32.768	35	kHz	(Note 1)
	Oscillation stabilization time (Note 2)			1.0	2	s	(Note 3)
					10	s	(Note 4)
External clock (Figure 2B)	XT1 input frequency	f_{XT}	32		100	kHz	(Note 4)
	XT1 input high/low level width	t_{XTH}, t_{XTL}	10		32	μs	

Notes:

(1) The oscillator frequency and input frequency indicates only the oscillator characteristics. Refer to the AC Characteristics for the instruction execution times.

(2) The oscillation stabilization time is the time required for the oscillation to stabilize after V_{DD} is applied and reaches the V_{DD} spec or after STOP mode is released.

(3) $V_{DD} = 4.5$ to 6.0 V for mask ROM parts and 4.5 to 5.5 V for programmable parts.

(4) $V_{DD} = 2.7$ to 6.0 V for mask ROM parts and 4.5 to 5.5 V for programmable parts.

Figure 1. Main System Clock Configurations

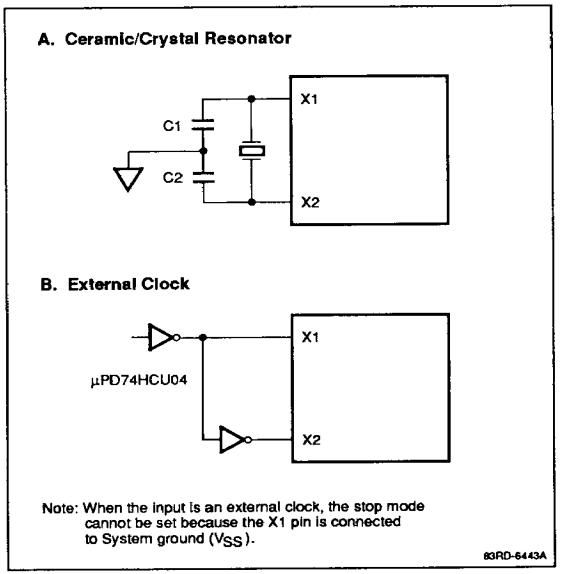
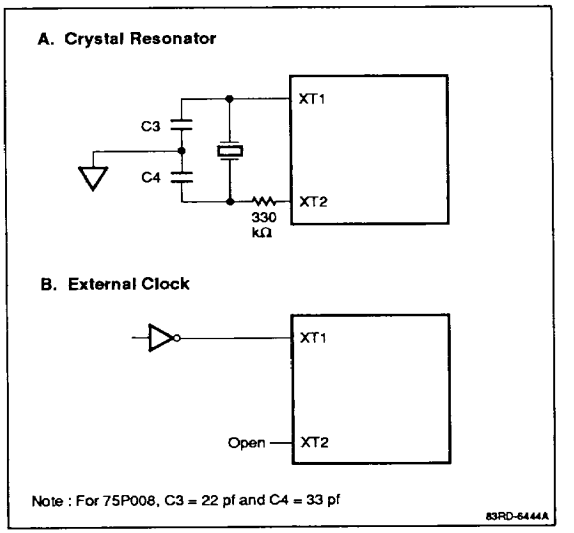


Figure 2. Subsystem Clock Configurations



Recommended Main System Clock Oscillator Circuit Constants (Mask ROM Parts and μPD75CG216A)

Main system clock = Ceramic; T_A = −40 to +85°C (for mask ROM parts) and −10 to +70°C (for μPD75CG216A)

Manufacturer	Product name (Note 1)	C1 (pF)	C2 (pF)	Remarks
Murata	CSA 2.00MG	30	30	
	CSA 4.19MG	30	30	
	CSA 4.91MG	30	30	
	CAT 2.00MG	None	None	C on-chip type
	CST 4.19MG	None	None	C on-chip type
	CST 4.91MG	None	None	C on-chip type
Kyocera	KBR-2.0 MS	47	47	For mask ROM parts only
	KBR-4.0MS	33	33	
	KBR-4.19MS	33	33	
	KBR-4.91MS	33	33	
TDK	FCR-3.58M2	30	30	
	FCR-4.00M2	30	30	
	FCR-4.19M2	30	30	
	FCR-4.19MC	None	None	C on-chip type

Notes:

(1) Oscillation voltage range = 4.0 to 6.0 V for mask ROM parts and V_{DD} = 4.5 to 5.5 V for μPD75CG216A

Recommended Main System Clock Oscillator Circuit Constants (Mask ROM Parts and μPD75CG216A)

Main system clock = Crystal; T_A = −40 to +85°C (for mask ROM parts) and −10 to +70°C (for μPD75CG216A)

Manufacturer	Frequency (MHz)	Retainer	Load Capacitance C_L (pF)	C1 (pF)	C2 (pF)	Oscillator Voltage Range Min (V)	Oscillator Voltage Range Max (V)
Kinseki	2.00	HC-18/U	16	20	20	4.5	(Note 1)
	4.19	HC-49/U	16	20	20	4.5	(Note 1)
	4.91	HC-43/U	16	20	20	4.5	(Note 1)

Notes:

(1) Oscillation voltage range max = 6.0 V for mask ROM parts and 5.5 V for μPD75CG216A.

Recommended Subsystem Clock Oscillator Circuit Constants (Mask ROM Parts and μPD75CG216A)

Subsystem clock = Crystal; T_A = −10 to +60°C (for the mask ROM parts) and −10 to +70°C (for the μPD75CG216A)

Manufacturer	Type	Load Capacitance C_L (pF)	C3 (pF)	C4 (pF)	R (kΩ)	Oscillator Voltage Range Min (V)	Oscillator Voltage Range Max (V)
Kinseki	P-3	12	22	22	330	(Note 1)	(Note 1)
Citizen	CFS-308	14	22	33	330	(Note 1)	(Note 1)

Notes:

(1) Oscillation voltage range is 2.7 to 6.0 V for the mask ROM parts and 4.5 to 5.5 V for the μPD75CG216A.

Recommended Main System Clock Ceramic Resonators (μPD75CG208)

Manufacturer	Product name	External Capacitors C1 (pF)	External Capacitors C2 (pF)	V_{DD} Range Min (V)	V_{DD} Range Max (V)
Murata	CSA 4.19 MG	30	60	4.5	5.5
Kyocera	KBR-2.09 MS	68	68	4.5	5.5
	KBR-3.58 MS	33	33	4.5	5.5
	KBR-4.19 MS	33	33	4.5	5.5
	KBR-4.9 M	33	33	4.5	5.5

Recommended Main System Clock Crystal Resonators (μPD75CG208)

Manufacturer (Note 1)	Product name	External Capacitors C1 (pF) (Note 2)	External Capacitors C2 (pF)	V_{DD} Range Min (V)	V_{DD} Range Max (V)
Kinseki	HC-49/U	15	15	4.5	5.5

Notes:

(1) Equivalent series resistance of a crystal must be lower than 80 Ω.

(2) Variable range of C1 for frequency trimming should be 10 to 33 (pF).

Power-on Reset Characteristics (Note 1)

T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 (Mask ROM parts); T_A = −10 to +70°C, V_{DD} = 5 V ±10% (μPD75CG208 and μPD75CG216A)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
POR high-level operating voltage	V_{DDH}	4.5		6.0	V	
POR low-level operating voltage	V_{DDL}	0		0.2	V	
Supply voltage rise time	t_r	10		(Note 2)	μs	
Supply voltage OFF time	t_{off}	1			s	
POR circuit current dissipation (Note 3)	I_{DDPR}		10	100	μA	V_{DD} = 5 V ± 10%; (μPD752xx only)
			10	200	μA	V_{DD} = 5 V ±10% (μPD75CG208/CG216A only)
			2	20	μA	V_{DD} = 2.7 V (μPD752xx only)

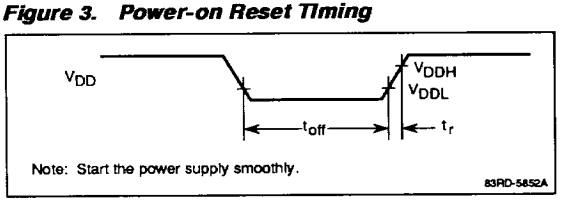
Notes:

(1) This circuit is present on the μPD75CG208 and μPD75CG216. It is a mask option on mask ROM parts and is not available on the μPD75P216A.

(2) $2^{17}/f_{XX}$ (31.3 ms at f_{XX} = 4.19 MHz).

(3) Current which flows when the internal reset circuit and power-on flag are used.

Figure 3. Power-on Reset Timing



DC Characteristics

T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V (Mask ROM parts); T_A = −10 to +70°C; V_{DD} = 4.5 to 5.5 V (Programmable Parts)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	All except ports 0, 1, 6; X1, X2, XT1, $\overline{RESET}$
	V_{IH2}	0.75 V_{DD}		V_{DD}	V	Ports 0 and 1; $\overline{RESET}$
	V_{IH3}	V_{DD}−0.4		V_{DD}	V	X1, X2, XT1
	V_{IH4}	0.65 V_{DD}		V_{DD}	V	Port 6; V_{DD} = 4.5 to 6.0 V (μPD752xx only); 5 V ±10% (programmable parts)
		0.7 V_{DD}		V_{DD}	V	Port 6; V_{DD} = 2.7 to 6.0 V (μPD752xx only)
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	All except ports 0, 1, 6; X1, X2, XT1, $\overline{RESET}$
	V_{IL2}	0		0.2 V_{DD}	V	Ports 0, 1, and 6; $\overline{RESET}$
	V_{IL3}	0		0.4	V	X1, X2, XT1
High-level output voltage	V_{OH}	V_{DD}−1.0			V	All outputs; I_{OH} = −1 mA (Note 10)
		V_{DD}−0.5			V	All outputs; I_{OH} = −100 μA (Note 11)
Low-level current	I_{IL}		−300	−800	μA	I_0-I_7; V_{IN} = 0 V; (μPD75CG208/G216A only)
Low-level output voltage	V_{OL}		0.4	2.0	V	Ports 4 and 5; I_{OL} = 15 mA (Note 10)
				0.4	V	All output pins; I_{OL} = 1.6 mA (Note 10)
				0.5	V	All output pins; I_{OL} = 400 μA (μPD752xx only)
High-level input leakage current	I_{LIH1}			3	μA	All except X1, X2, and XT1; V_{IN} = V_{DD}
	I_{LIH2}			20	μA	X1, X2, and XT1; V_{IN} = V_{DD}
Low-level input leakage current	I_{LIL1}			−3	μA	All except X1, X2, and XT1; V_{IN} = 0 V
	I_{LIL2}			−20	μA	X1, X2, and XT1; V_{IN} = 0 V
High-level output leakage current	I_{LOH}			3	μA	All output pins; V_{OUT} = V_{DD}
Low-level output leakage current	I_{LOL1}			−3	μA	All except display output pins; V_{OUT} = 0 V
	I_{LOL2}			−10	μA	Display output pins; V_{OUT} = V_{LOAD} = V_{DD}−35 V
Display output current	I_{OD}	−3	−5.5		mA	S0-S9 (Note 1) see Recommended External Circuit
		−3	−5.5		mA	S0-S9; V_{DD} = 4.5 to 6.0 V; V_{OD} = V_{DD} −2 V (μPD75P216A only)
		−1.5	−3.5		mA	S0-S9; All except μPD75P216A (Note 2)
		−15	−22		mA	T0-T15 (Note 1) see Recommended External Circuit
		−15	−22		mA	T0-T15; V_{DD} = 4.5 to 6.0 V; V_{OD} = V_{DD} −2 V (μPD75P216A only)
		−7	−15		mA	T0-T15; All except μPD75P216A (Note 2)
Internal pull-down resistor (mask option)	R_{P6}	30	80	200	kΩ	Port 6; V_{DD} = 4.5 to 6.0 V (μPD75206/208)
		20	80	200	kΩ	Port 6; V_{DD} = 4.5 to 6.0 V (μPD75212A/216A only); V_{IN} = V_{DD}
		30		1000	kΩ	Port 6; V_{DD} = 2.7 to 6.0 V (μPD75206/208)
		20		1000	kΩ	Port 6; V_{DD} = 2.7 to 6.0 V (μPD75212A/216A only); V_{IN} = V_{DD}
	R_L	25	70	135	kΩ	Display output pins; V_{DD}-V_{LOAD} = 35 V (μPD75212A/216A/P216A)
		40	70	120	kΩ	Display output pins; V_{DD}-V_{LOAD} = 35 V (μPD75206/208/CG208/CG216A)

DC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply current (Note 6)	I_{DD1} (Note 3)		3.0	9.0	mA	V_{DD} = 5 V ± 10% (Note 4)
			0.55	1.5	mA	V_{DD} = 3 V ± 10% (Note 5; μPD752xx only)
	I_{DD2} (Note 3)		600	1800	μA	HALT mode; V_{DD} = 5 V ± 10% (Note 12)
			200	600	μA	HALT mode; V_{DD} = 3 V ± 10% (μPD752xx only)
	I_{DD3}		40	120	μA	V_{DD} = 3 V ± 10% (Notes 7, 8; μPD752xx only)
			100	300	μA	(Note 7; μPD75CG208/CG216A and μPD75P216A only)
	I_{DD4}		5	15	μA	HALT mode; V_{DD} = 3 V ± 10% (Notes 7, 8; μPD752xx only)
			40	100	μA	HALT mode (Notes 7, 8; μPD75CG208/CG216A and μPD75P216A only)
	I_{DD5}		0.5	20	μA	STOP mode; XT1 = 0 V; V_{DD} = 5 V ± 10 %; μPD752xx only (Note 6)
			0.1	10	μA	STOP mode; XT1 = 0 V; V_{DD} = 3 V ± 10 %; μPD752xx only (Note 6)
			10	200	μA	STOP mode; XT1 = 0 V; (Note 9; μPD75CG208 and μPD75CG216A only)
			0.5	200	μA	STOP mode; XT1 = 0 V (μPD75P216A only)

Notes:

(1) V_{DD} = 4.5 to 6.0 V for mask ROM parts and V_{DD} = 4.5 to 5.5 V for programmable parts; $V_{OD} = V_{DD} - 2$ V; $V_{PRE} = V_{DD} - 9 \pm 1$ V.

(2) V_{DD} = 4.5 to 6.0 V for mask ROM parts and V_{DD} = 4.5 to 5.5 V for programmable parts; $V_{OD} = V_{DD} - 2$ V; V_{PRE} = 0 V.

(3) 4.19 MHz crystal oscillator; C1 = C2 = 15 pF.

(4) Value during high-speed operation and the processor control clock (PCC) is set to 0011.

(5) Value during low-speed operation and the processor control clock (PCC) is set to 0000.

(6) Does not include pull-down resistor current for S0-S8 and T0-T9. In the mask ROM parts, the current for the power-on reset circuit (mask option) is not included. In the μPD75CG208/CG216A, the current for the piggyback EPROM and the current in the on-chip pull-up resistors for I0-I7 is not included.

(7) 32 kHz crystal oscillator.

(8) Value when the system clock control register (SCC) is set to 1001, generation of the main system clock pulse is stopped, and the CPU is operated by the subsystem clock pulse.

(9) With the $\overline{CE}$ or $\overline{OE}$ of the piggybacked EPROM set high.

(10) V_{DD} = 4.5 to 6.0 V for mask ROM parts and V_{DD} = 4.5 to 5.5 V for programmable parts.

(11) V_{DD} = 2.7 to 6.0 V for mask ROM parts and V_{DD} = 4.5 to 5.5 V for programmable parts.

(12) For the μPD75CG208/CG216A, the $\overline{CE}$ or $\overline{OE}$ pin of the piggyback EPROM is set to a high level.

(13) No subsystem clock.

AC Characteristics

Mask ROM parts: T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V
Programmable parts: T_A = −10 to +70°C; V_{DD} = 5 V ±10%

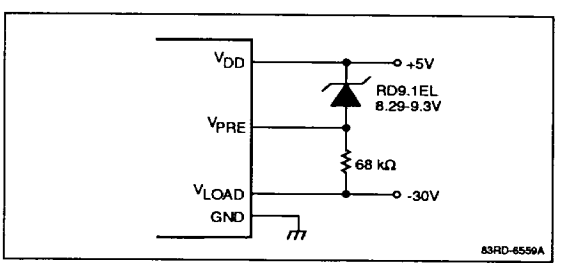
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Cycle time: minimum instruction execution time (Note 1)	t_{CY}	0.95		32	μs	Main system clock; V_{DD} = 4.5 to V_{DD} max
		3.8		32	μs	Main system clock; V_{DD} = 2.7 to 6.0 V; (μPD752xx only)
		114	122	125	μs	Subsystem clock
TI0 input frequency	f_{TI}	0		0.6	MHz	V_{DD} = 4.5 to V_{DD} max (μPD752xx/P216A)
		0		165	kHz	V_{DD} = 2.7 to 6.0 V (μPD752xx only)
		0		1	MHz	(μPD75CG208/CG216A only)
TI0 input low- and high-level width	t_{IL}, t_{IH}	0.83			μs	V_{DD} = 4.5 to V_{DD} max (μPD752xx and μPD75P216A only)
		3			μs	V_{DD} = 2.7 to 6.0 V (μPD752xx only)
		0.48			μs	(μPD75CG208/CG216A only)
$\overline{SCK}$ cycle time	t_{KCY}	0.8			μs	Input; V_{DD} = 4.5 to V_{DD} max
		0.95			μs	Output; V_{DD} = 4.5 to V_{DD} max
		3.2			μs	Input; V_{DD} = 2.7 to 6.0 V (μPD752xx only)
		3.8			μs	Output; V_{DD} = 2.7 to 6.0 V (μPD752xx only)
$\overline{SCK}$ low- and high-level width	t_{KL}, t_{KH}	0.4			μs	Input; V_{DD} = 4.5 to V_{DD} max
		0.5 t_{KCY} − 50			ns	Output; V_{DD} = 4.5 to V_{DD} max
		1.6			μs	Input; V_{DD} = 2.7 to 6.0 V (μPD752xx only)
		0.5 t_{KCY} − 150			ns	Output; V_{DD} = 2.7 V to 6.0 V (μPD752xx only)
SI vs. $\overline{SCK}$ ↑ setup time	t_{SIK}	100			ns	
SI vs. $\overline{SCK}$ ↑ hold time	t_{KSI}	400			ns	
$\overline{SCK}$ ↓ → SO output delay time	t_{KSO}			300	ns	V_{DD} = 4.5 to V_{DD} max
				1000	ns	V_{DD} = 2.7 to 6.0 V (μPD752xx only)
Interrupt inputs low- and high-level width	t_{INTL}, t_{INTH}	(Note 2)			μs	INT0
		2 t_{CY}			μs	INT1
		10			μs	INT2, INT4
$\overline{RESET}$ low-level width	t_{RSL}	10			μs	

Notes:

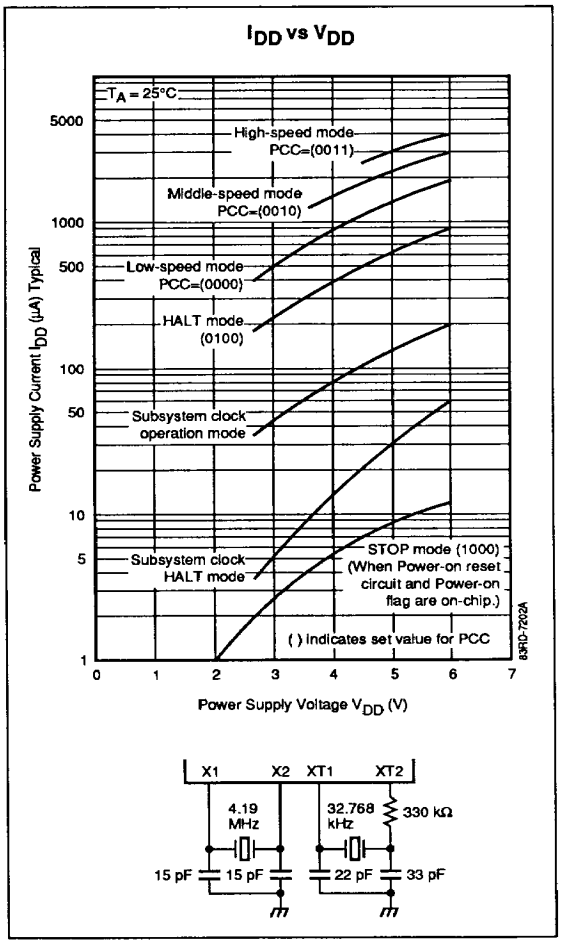
(1) Cycle time is determined by the frequency of the oscillator connected to the microcomputer, system clock control register (SCC), V_{DD}, and the processor clock control (PCC). See the graph depicting the supply voltage vs. The cycle time when the microcomputer is operating on the main system clock.

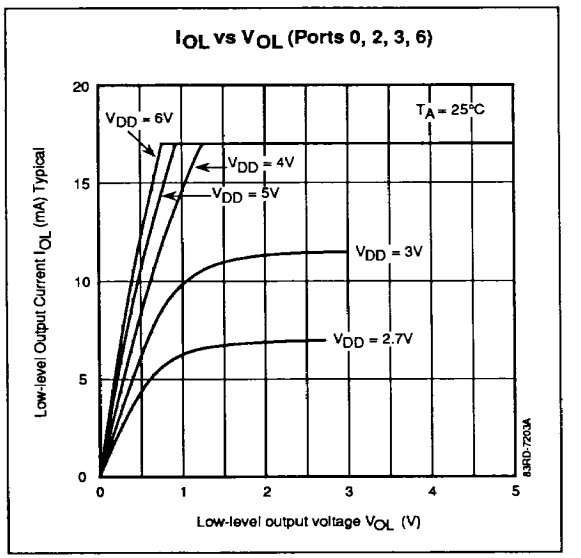
(2) $2t_{CY}$ or $128/f_{XX}$, depending on the setting of the interrupt mode register (IM0).

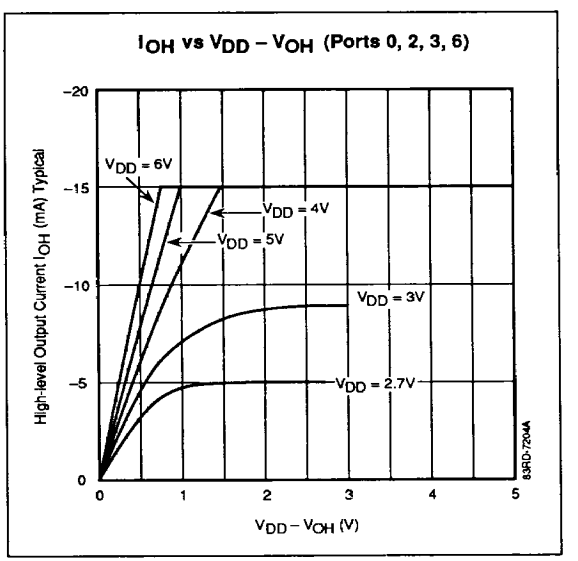
Recommended External Circuit



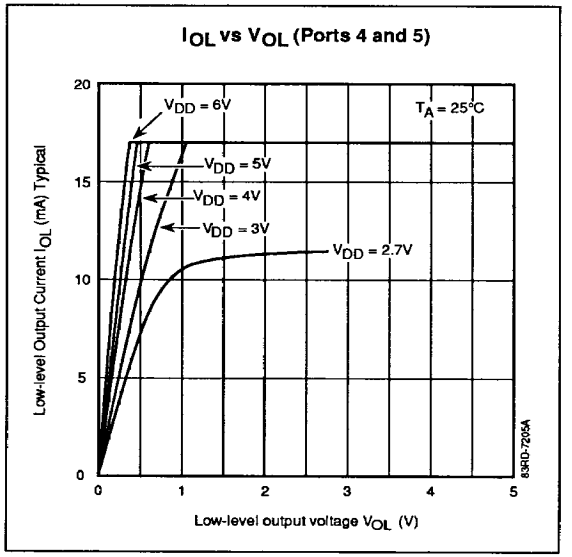
DC Characteristics (μPD752xx only)

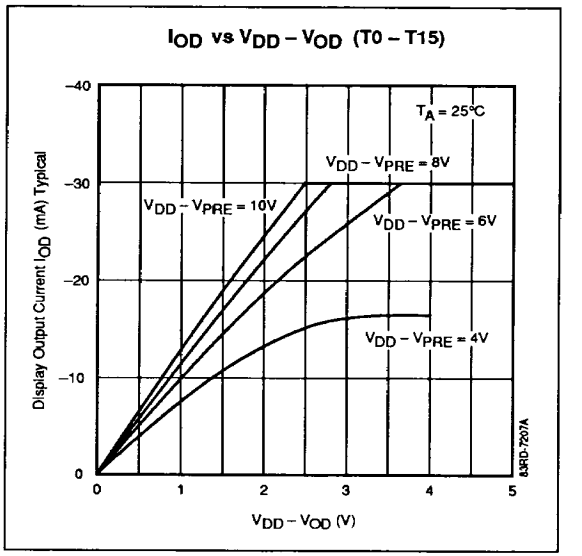


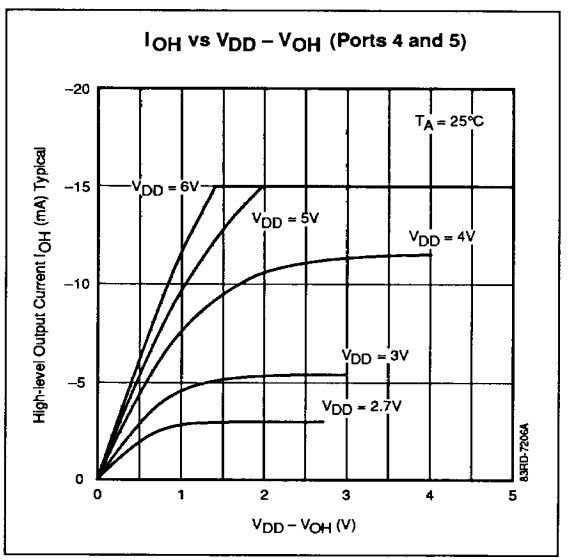




DC Characteristics (μPD752xx only) (cont)







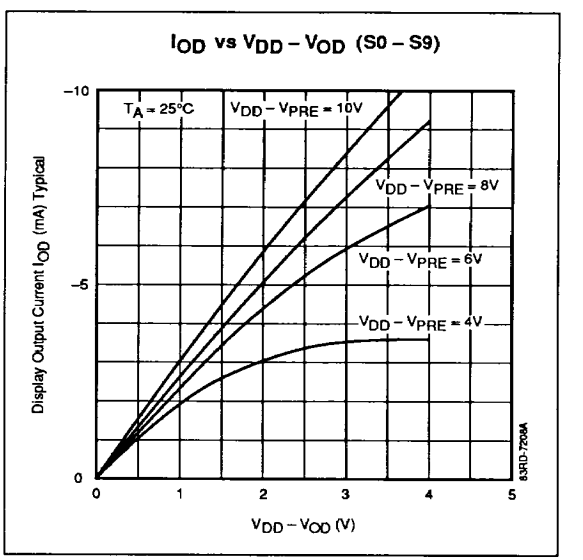


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Figure 4. Guaranteed Operating Range

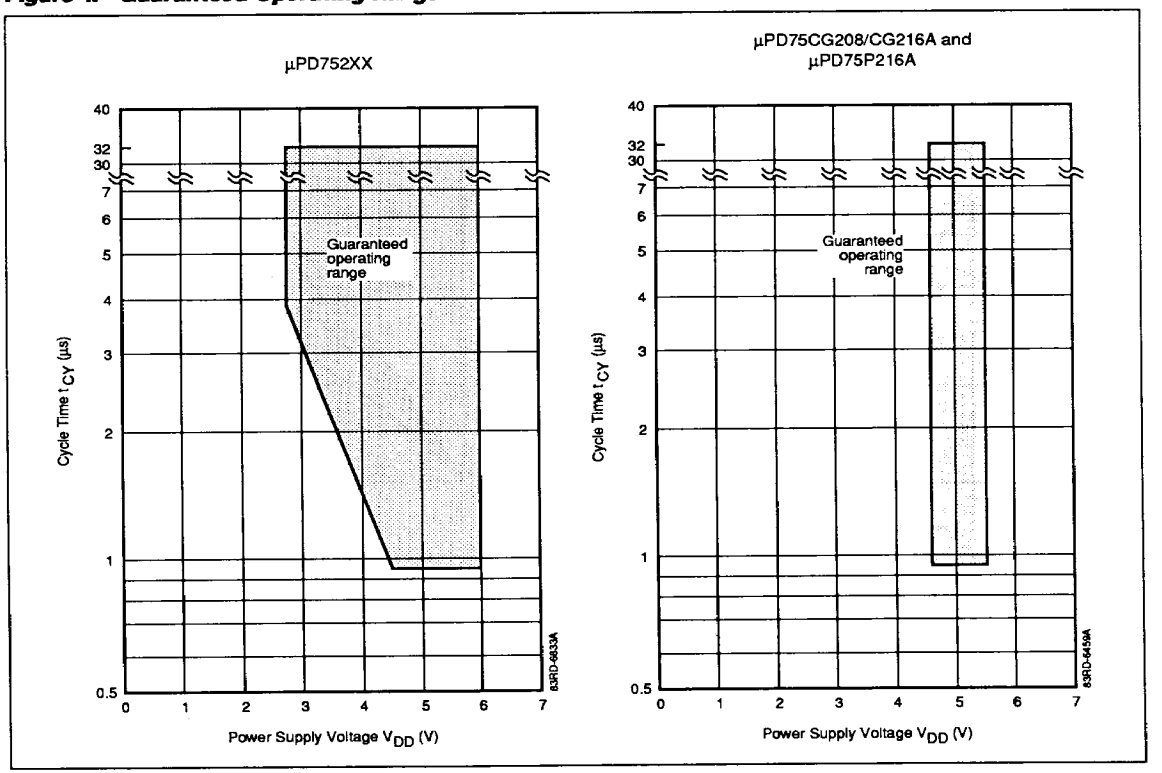


Figure 5. AC Timing Measurement Points

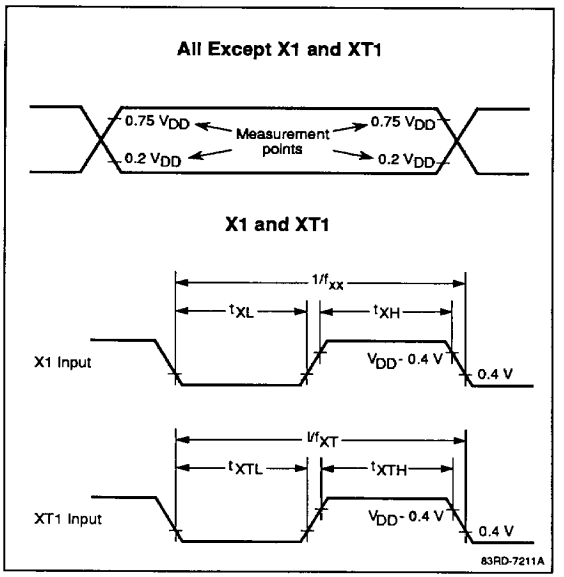


Figure 6. TI0 Timing

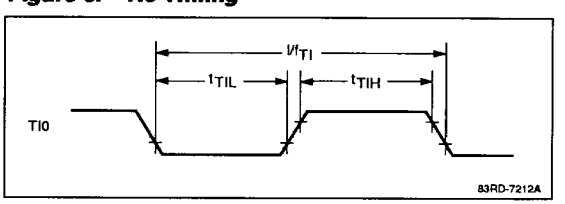


Figure 7. Serial Transfer Timing

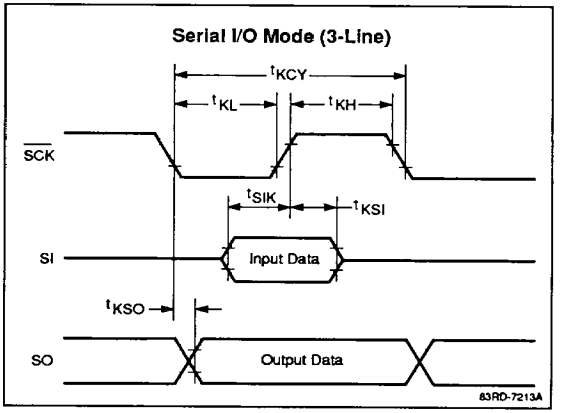


Figure 8. Interrupt Input Timing

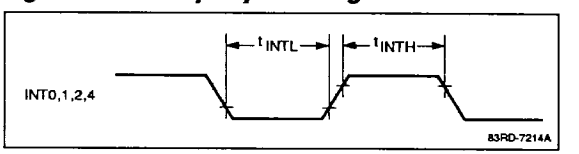
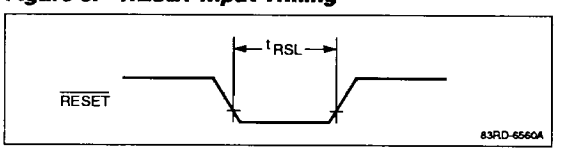


Figure 9. RESET Input Timing



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Data Memory STOP Mode Low Voltage Data Retention Characteristics

Mask ROM parts: T_A = −40 to +85°C
Programmable parts: T_A = −10 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.0		V_{DD} max	V	
Data retention current (Note 1)	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2.0 V (μPD752xx and μPD75P216A)
			10	200	μA	V_{DDDR} = 2.0 V (μPD75CG208/CG216A)
Release signal SET time	t_{SREL}	0			μs	
Oscillation stabilization time (Note 2)	t_{WAIT}		2^{17}/fx		ms	Release by $\overline{\text{RESET}}$ input
			(Note 3)		ms	Release by interrupt request

Notes:

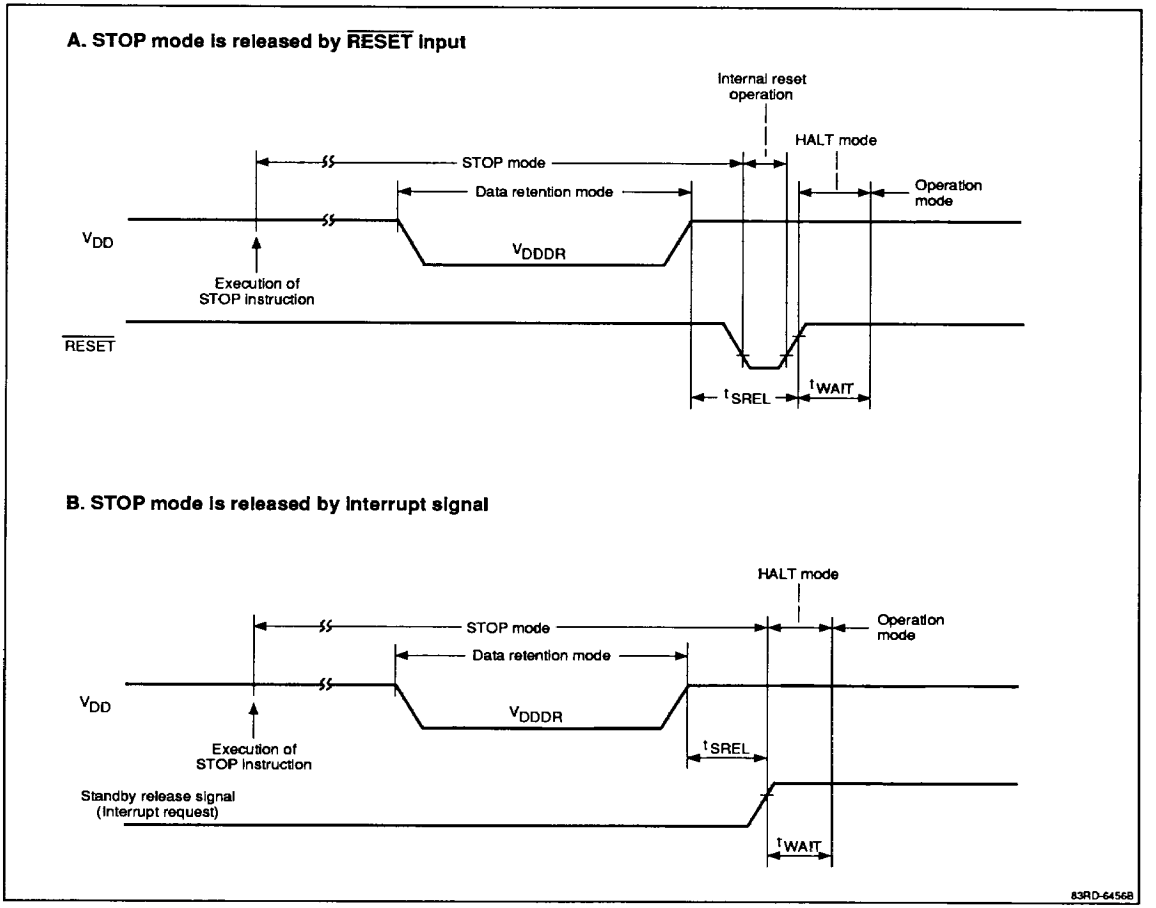
(1) Excludes the on-chip pull-down resistor and power-on reset circuit (mask option) in the mask ROM parts.

(2) Consult the vendor's resonator specification for this value.

(3) Oscillation stabilization WAIT time is the time during which the CPU is stopped and the crystal is stabilizing. This time is required to prevent unstable operation while the oscillation is started. The interval timer can be used to delay the CPU from executing instructions using the setting of the basic interval timer mode register (BTM) according to the following table:

BTM3	BTM2	BTM1	BTM0	WAIT time (f_{XX} = 4.19 MHz)
–	0	0	0	$2^{20}/f_{XX}$ (Approx 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (Approx 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (Approx 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (Approx 1.95 ms)

Figure 10. Data Retention Timing



DC Programming Characteristics (μPD75P216A only)

T_A = 25 ± 5°C; V_{DD} = 6.0 ± 0.25 V; V_{PP} = 12.5 ± 0.3 V; V_{SS} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	All except X1, X2
	V_{IH2}	V_{DD}–0.5		V_{DD}	V	X1, X2
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	All except X1, X2
	V_{IL2}	0		0.4	V	X1, X2
Input leakage current	I_{IL}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-level output voltage	V_{OH}	V_{DD}–1.0			V	I_{OH} = –1 mA
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} supply current	I_{DD}			30	mA	
V_{PP} supply current	I_{PP}			30	mA	MD0 = V_{IL}; MD1 = V_{IH}

Notes:

(1) V_{PP} must not exceed +22.0 V, including overshoot.

(2) V_{DD} is to be applied prior to V_{PP} and to be removed after V_{PP} is removed.

AC Programming Characteristics (μPD75P216A only)

T_A = 25 ± 5°C; V_{DD} = 6.0 ± 0.25 V; V_{PP} = 12.5 ± 0.3 V; V_{SS} = 0 V

Parameter	Symbol	EPROM Symbol (Note 1)	Min	Typ	Max	Unit	Conditions
Address setup time (Note 2)	t_{AS}	t_{AS}	2			μs	
MD1 to MD0 ↓ setup	t_{M1S}	t_{OES}	2			μs	
Data to MD0 ↓ setup	t_{DS}	t_{DS}	2			μs	
Address hold from MD0 ↑ (Note 2)	t_{AH}	t_{AH}	2			μs	
Data hold from MD0 ↑	t_{DH}	t_{DH}	2			μs	
Data output float delay from MD0 ↑	t_{DF}	t_{DF}	0		130	ns	
V_{PP} setup to MD3 ↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} setup to MD3 ↑	t_{VDS}	t_{VCS}	2			μs	
Initialized program pulse width	t_{PW}	t_{PW}	0.95	1	1.05	ms	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95		21	ms	
MD0 setup to MD1 ↑	t_{MOS}	t_{CES}	2			μs	
Data output delay from MD0 ↓	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 hold to MD0 ↑	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 recovery from MD0 ↓	t_{M1R}	t_{OR}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
Program counter reset	t_{PCR}	–	10			μs	
X1 input high/low level width	t_{XH}, t_{XL}	–	0.125			μs	
X1 input frequency	f_{XX}	–			4.19	MHz	
Initial mode set	t_I	–	2			μs	
MD3 Setup to MD1 ↑	t_{M3S}	–	2			μs	
MD3 hold to MD1 ↓	t_{M3H}	–	2			μs	
MD3 setup to MD0 ↓	t_{M3SR}	–	2			μs	During program read cycle
Address → data output delay time (Note 2)	t_{DAD}	t_{ACC}	2			μs	
Address → data output hold time (Note 2)	t_{HAD}	t_{OH}	0		130	ns	
MD3 output hold from MD0 ↑	t_{M3HR}	–	2			μs	
Data output float delay from MD3 ↓	t_{DFR}	–	2			μs	

Notes:

(1) These symbols correspond to those of the μPD27C256 EPROM.

(2) The internal address signal is incremented by the rising edge of the fourth X1 pulse; it is not connected to an external pin.

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Figure 11. OTP Memory Write Timing (Programmable)

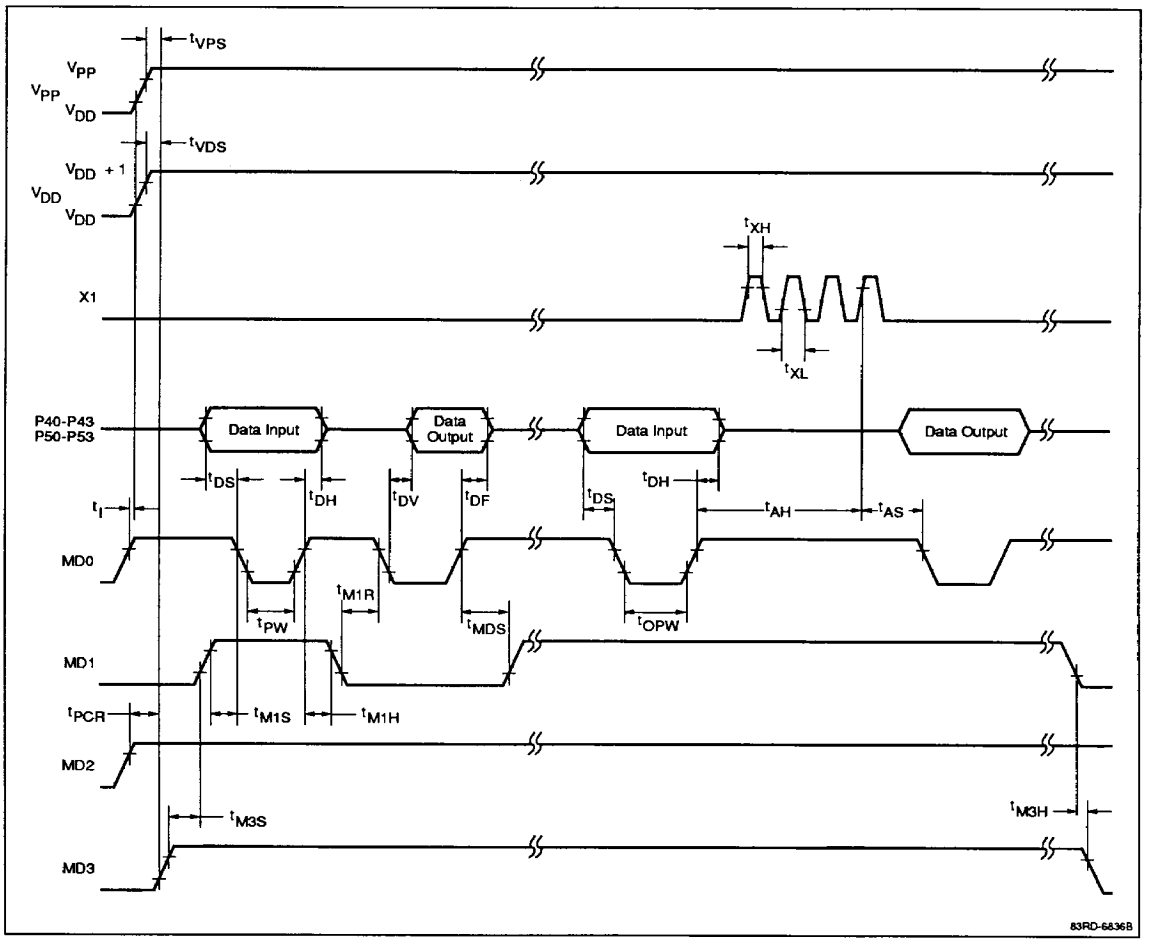
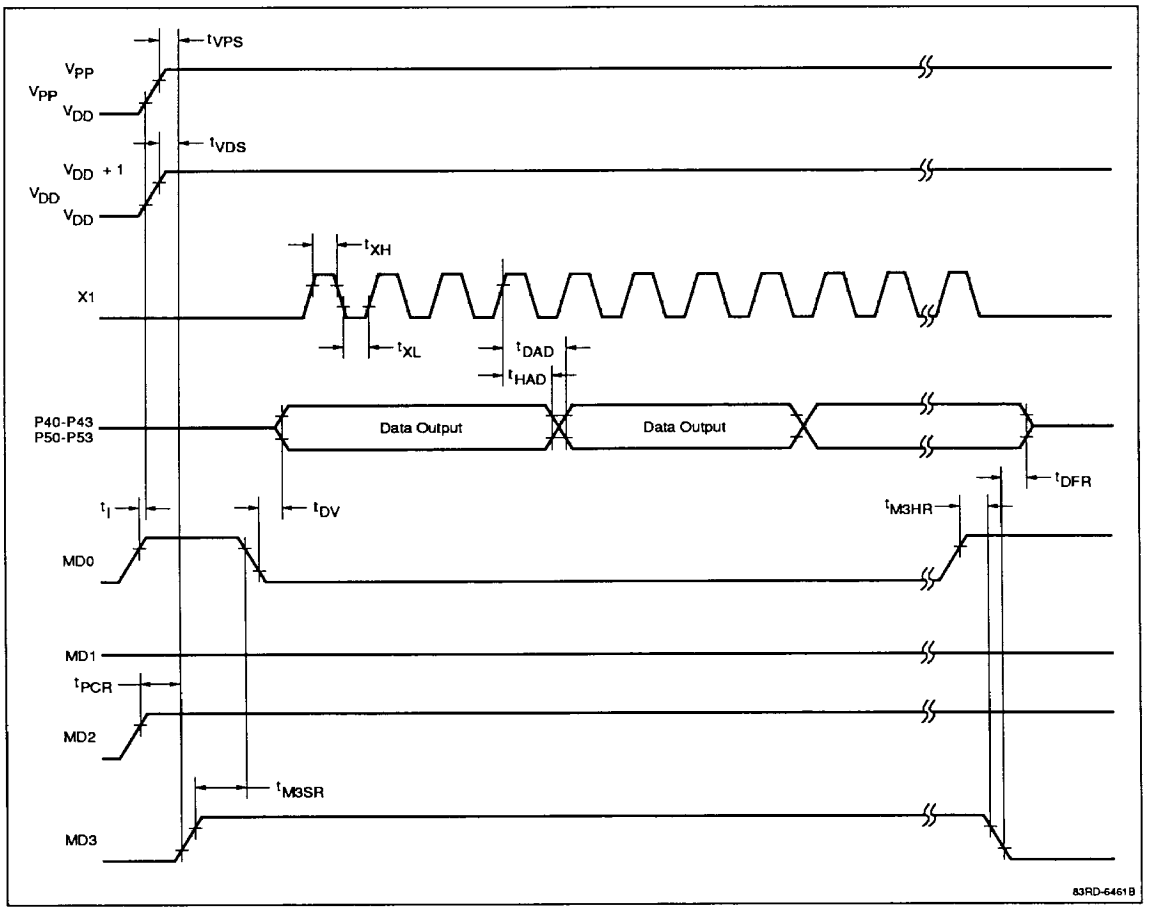


Figure 12. OTP Memory Read Timing (Programmable)



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