



52B13/52B13H

16K Electrically Erasable PROM

T-46-13-27

August 1991

Features

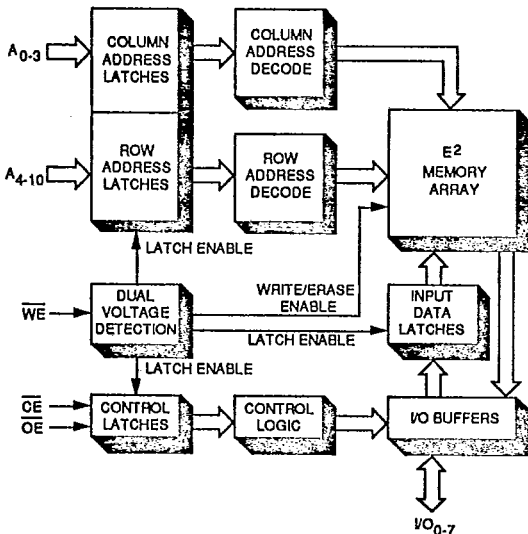
- **Military, Extended and Commercial Temperature Range**
 - -55° C to +110° C WRITE Operation (Military)
 - -55° C to +125° C READ Operation (Military)
 - -40° C to +85° C Operation (Extended)
 - 0° C to +70° C Operation (Commercial)
- **Input Latches**
- **5V ± 10% 2K x 8 EEPROM**
- **1 ms (52B13H) or 9 ms TTL Byte Erase/Write**
- **10,000 Erase/Write Cycles per Byte Minimum**
- **Chip Erase and Byte Erase**
- **DITrace®**
- **Fast Read Access Time – 200 ns**
- **Infinite Number of Read Cycles**
- **JEDEC Approved Byte Wide Memory Pinout**
- **Intel 2816/2816A E² Compatible**
- **MIL-STD-883 Class B Compliant**

Description

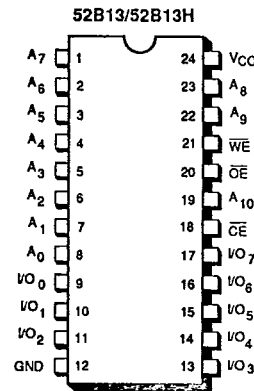
SEEQ's 52B13 and 52B13H are 2048 x 8 bit, 5 volt electrically erasable programmable read only memories (EEPROMs) which are specified over the military and extended temperature range respectively. They have input latches on all addresses, data, and control (chip and output) enable lines. Data is latched and electrically written by a TTL (or a 21V pulse) on the Write Enable pin. Once written, which requires under 10 ms, there is no limit to the number of times data may be read. Both byte and chip erase modes are available. The erasure time in either mode is under 10 ms, and each byte may be erased and written a minimum of 10,000 times.

The 52B13 is compatible to the Intel 2816/2816A and SEEQ's 5213. For system upgrades of these older generation EEPROMs, the 52B13 is specified over the industry standard temperature ranges and has an access time of 200 ns. The 52B13 is available in a 24 pin cerdip package.

Block Diagram



Pin Configuration



Pin Names

A ₀ -A ₁₀	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O ₀₋₇	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

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Technology, Incorporated

MD400104/-

www.DataSheet4U.com

These EEPROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic reconfiguration (the alteration of operating software in real-time) is made possible by this device. Applications will be found in military avionics systems, programmable character generators, self-calibrating instruments/machines, programmable industrial controllers, and an assortment of other systems. Designing the EEPROMs into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

Device Operation

SEEQ's 52B13 and 52B13H have six modes of operation (see Table 1) and except for the chip erase mode they require only TTL inputs to operate these modes.

To write into a particular location of the 52B13 or 52B13H, that byte must first be erased. A memory location is erased by presenting the 52B13 or 52B13H with Chip Enable at a TTL low while Output Enable is a TTL high, and TTL highs (logical '1's) are being presented to all the I/O lines. These levels are latched and the data written when write enable is brought to a TTL low level. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B13H performs the same as the 52B13 except that the device byte erase/byte write time has been enhanced to 1 ms.

The 52B13 is compatible to prior generation EEPROMs which required a high voltage signal for writing and erasing. In the 52B13 there is an internal dual level detection

circuit which allows either a TTL low or 21V signal to be applied to \overline{WE} to execute an erase or write operation. The 52B13 specifies no restriction on the rising edge of \overline{WE} .

For certain applications, the user may wish to erase the entire memory. A chip erase is performed in the same manner as a byte erase except that Output Enable is between 14V and 22V. All 2K bytes are erased in under 10ms.

A characteristic of all EEPROMs is that the total number of write and erase cycle is not unlimited. The 52B13 and 52B13H have been designed for applications requiring up to 10,000 write and erase cycles per byte. The write and erase cycling characteristic is completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to \overline{WE} , enabling the chip, and enabling the outputs. Data is available t_{CE} time after Chip Enable is applied or t_{AA} time from the addresses. System power may be reduced by placing the 52B13 or 52B13H into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

DiTrace

SEEQ's family of EEPROMs incorporate a DiTrace field. The DiTrace feature is a method for storing production flow information to wafer level in an extra column of EEPROM cells. As each major manufacturing operation is performed the DiTrace field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Table 1. Mode Selection ($V_{CC} = 5V \pm 10\%$)

Mode	PIN	\overline{OE} (18)	\overline{OE} (20)	\overline{WE} (21)	I/O (9-11, 13-17)
Read ^[1]		V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby ^[1]		V_{IH}	Don't Care	V_{IH}	High Z
Byte Erase ^[2]		V_{IL}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write ^[2]		V_{IL}	V_{IH}	V_{IL}	D_{IN}
Chip Erase ^[2]		V_{IL}	V_{OE}	V_{IL}	$D_{IN} = V_{IH}$
Write/Erase Inhibit		V_{IH}	Don't Care	Don't Care	High Z

NOTES:

- \overline{WE} may be from V_{IH} to 6V in the read and standby mode.
- \overline{WE} may be at V_{IL} (TTL WE Mode) or from 15 to 21V (High Voltage \overline{WE} mode) in the byte erase, byte write, or chip erase mode of the 52B13/52B13H.

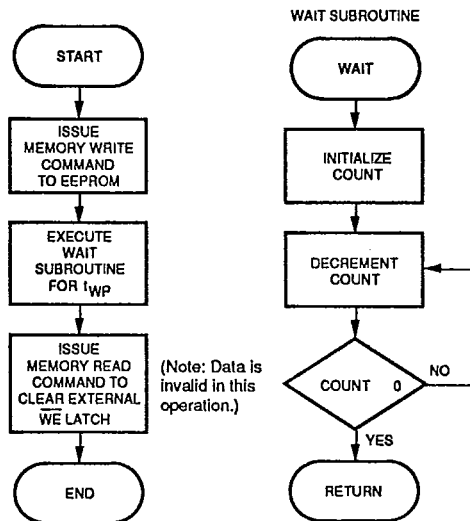
Power Up/Down Considerations

SEEQ's "52B" E² family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

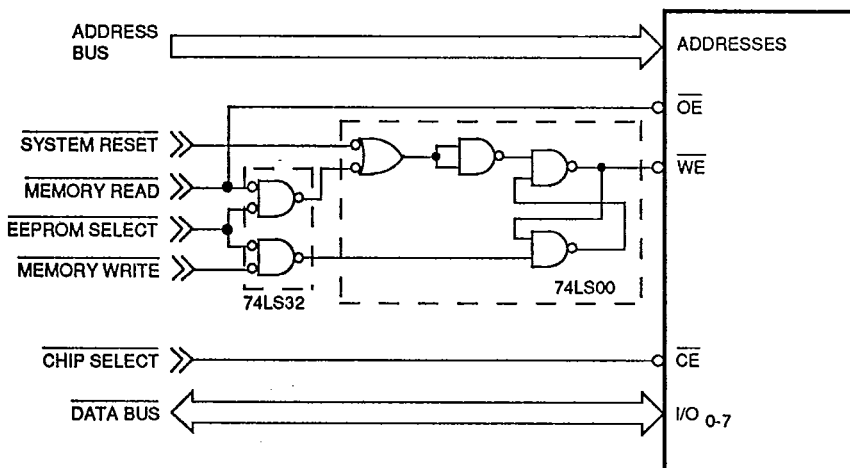
1. V_{CC} is less than 3 V.¹⁾
2. A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.

Writing will also be prevented if \overline{CE} or \overline{OE} are in a logical state other than that specified for a byte write in the mode selection table.

Typical EEPROM Write/Erase Routine



Microprocessor Interface Circuit Example for Byte Write/Erase



NOTE:

1. Characterized. Not tested.

Absolute Maximum Stress Ratings***Temperature**

Storage -65°C to +150°C

Under Bias

Military/Extended -65°C to +135°C

Commercial -10°C to +80°C

D.C. Voltage applied to all Inputs or Outputs

with respect to ground +6.0 V to -0.5 V

Undershoot/Overshoot pulse of less than 10 ns

(measured at 50% point) applied to all inputs or

outputs with respect to ground (undershoot) -1.0 V

(overshoot) + 7.0 V

 \overline{WE} During Writing/Erasing

with Respect to Ground +22.5V to -0.3V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		52B33-200 52B33H-200	52B33-250 52B33H-250	52B33-300 52B33H-300	52B33-350 52B33H-350
Temperature Range	Commercial	0°C to +70°C	0°C to +70°C	0°C to +70°C	0°C to +70°C
	Extended	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C
	Military				
	Read	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
	Write	-55°C to +110°C	-55°C to +110°C	-55°C to +110°C	-55°C to +110°C
Vcc Supply Voltage		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T _{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

D.C. Operating Characteristics During Read or Erase/Write(Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage					
	Read Mode			10	μA	$\overline{WE} = V_{IH}$
	TTL W/E Mode			10	μA	$\overline{WE} = V_{IL}$
	High Voltage W/E Mode			1.5	mA	$\overline{WE} = 22V, \overline{CE} = V_{IL}$
	High Voltage W/E Inhibit Mode			1.5	mA	$\overline{WE} = 22V, \overline{CE} = V_{IH}$
	Chip Erase — TTL Mode			10	μA	$\overline{WE} = V_{IL}$
	Chip Erase — High Voltage Mode			1.5	mA	$\overline{WE} = 22V$
I_{CC1}	V_{CC} Standby Current					
	Military/Extended		15	35	mA	$\overline{CE} = V_{IH}$
	Commercial		15	30	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current					
	Military/Extended		50	90	mA	$\overline{CE} = \overline{OE} = V_{IL}$
	Commercial		50	80	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2		$V_{CC} + 1$	V	
V_{WE}	\overline{WE} Read Voltage	2		$V_{CC} + 1$	V	
	\overline{WE} Write/Erase Voltage					
	TTL Mode	-0.1		0.8	V	
	High Voltage Mode	14		22	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA
V_{OE}	\overline{OE} Chip Erase Voltage	14		22	V	$I_{OE} = 10$ μA

Equivalent A.C.**Test Conditions^[2]**Output Load: 1 TTL gate and $C_L = 100$ pFInput Rise and Fall Times: ≤ 20 ns

Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level:

Inputs 1V and 2V

Outputs 0.8V and 2V

Capacitance^[1] $T_A = 25^\circ C, f = 1$ MHz

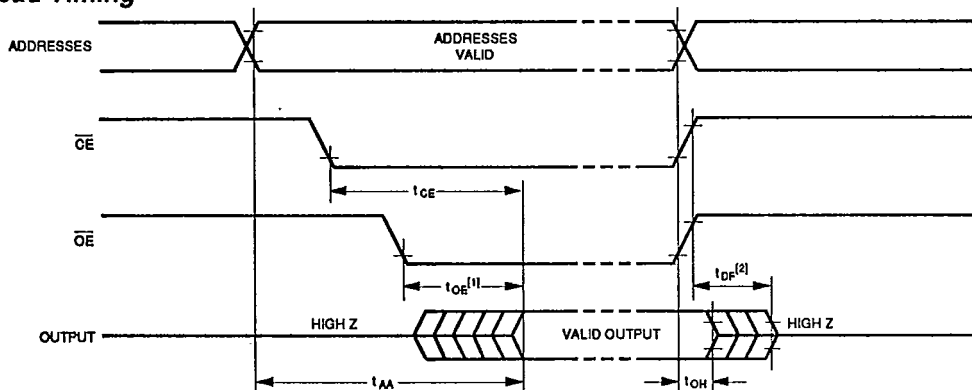
Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	10	pF	$V_{OUT} = 0V$
CV_{CC}	V_{CC} Capacitance	500	pF	$\overline{OE} = \overline{CE} = V_{IH}$
CV_{WE}	V_{WE} Capacitance	10	pF	$\overline{OE} = \overline{CE} = V_{IH}$

NOTES:

1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. These are equivalent test conditions and actual test conditions are dependent on the tester.

A.C. Operating Characteristics During Read (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Device Number Extension	52B13		52B13H		Units	Test Conditions
			Min.	Max.	Min.	Max.		
t_{AA}	Address Access Time	-200 -250 -300 -350		200 250 300 350		200 250 300 350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable to Data Valid	-200 -250 -300 -350		200 250 300 350		200 250 300 350	ns	$\overline{OE} = V_{IL}$
$t_{OE}^{(1)}$	Output Enable to Data Valid	-200 -250 -300 -350		80 90 90 110		80 90 90 110	ns	$\overline{CE} = V_{IL}$
$t_{DF}^{(2)}$	Output Enable to High Impedance	-200 -250 -300 -350	0 0 0 0	60 70 70 80	0 0 0 0	60 70 70 80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold	All	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read Timing**NOTES:**

- \overline{OE} may be delayed to $t_{AA} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{AA} .
- t_{DF} is specified from \overline{OE} or \overline{CE} , whichever occurs first.

A.C. Operating Characteristics During Write/Erase

(Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Max.	Units
t_s	\overline{CE} , \overline{OE} or Address Setup to \overline{WE}	50		ns
t_{DS}	Data Setup to \overline{WE}	15		ns
$t_H^{(1)}$	\overline{WE} to \overline{CE} , \overline{OE} , Address or Data Change	50		ns
t_{WP}	Write Enable (\overline{WE}) Pulse Width Byte Modes — 52B13	9		ms
	Byte Modes — 52B13H	1		
$t_{WR}^{(2)}$	\overline{WE} to Mode Change	50		ns
	\overline{WE} to Start of Next Byte Write Cycle			
	\overline{WE} to Start of Read Cycle		2	μ s

NOTES:

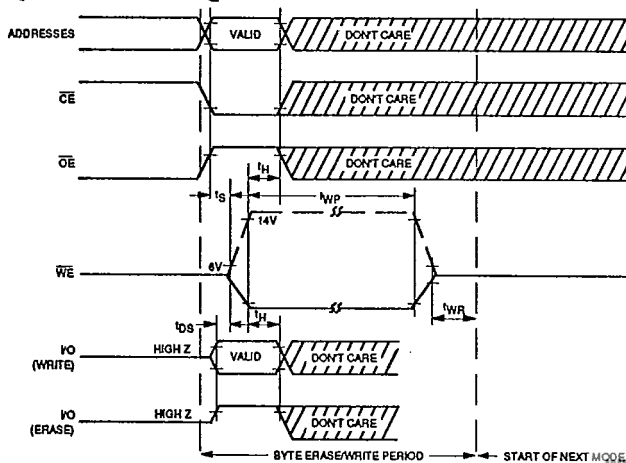
- After t_H , hold time, from \overline{WE} , the inputs \overline{CE} , \overline{OE} , Address and Data are latched and are "Don't Care" until t_{WR} , Write Recovery Time, after the trailing edge of \overline{WE} .
- The Write Recovery Time, t_{WR} , is the time after the trailing edge of \overline{WE} that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.

52B13/52B13H High Voltage Write Specifications

Except for the functional differences noted here, the 52B13 and 52B13H operate to the same specifications, including the TTL W/E mode.

Symbol	Function/Parameter	52B13		52B13H		Units	
		Min.	Max.	Min.	Max.		
t_{WP}	Write Enable Pulse Width Byte Write/Erase	Military/Extended	9	20	1	20	ms
		Commercial	9	20	1	10	ms
	Chip Erase	Military/Extended	9	20	9	20	ms
		Commercial	9	20	9	20	ms
V_{WE}	\overline{WE} Write/Erase Voltage High Voltage Mode	14	22	14	22	V	

Byte Erase or Byte Write Timing

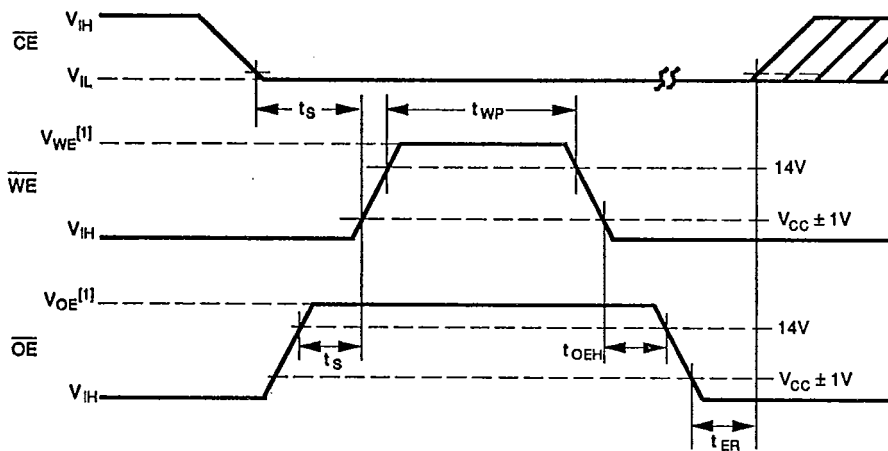


Notes: See AC notes

Chip Erase Specifications

Symbol	Parameter	Min.	Max.	Units
t_s	\overline{OE} , \overline{OE} Setup to \overline{WE}	1		μs
t_{OEH}	\overline{OE} Hold Time	1		μs
t_{WP}	\overline{WE} Pulse Width	10		ms
t_{ER}	Erase Recovery Time		10	μs

Chip Erase Timing



NOTES:

1. V_{WE} and V_{OE} can be from 15V to 21V in the high voltage mode for chip erase on 52B13.

Ordering Information

