SIEMENS

# ICs for Communications

4 Channel ADPCM Controller
Quad ADPCM

PEB 7274 Version 1.2

PEF 7274 Version 1.2

Data Sheet 08.97

DS 1

| PEB 7274<br>Revision History: Current Version: 08.97 | | |
|---|---|---|
| Previous Version: Preliminary Data Sheet 01.97 | | |
| Page (in previous Version) | Page (in new Version) | Subjects (major changes since last revision) |
| - | 5 | List of figures (new) |
| 52 | 52 | Note added (The last 15 bits ...) |
| 72 | 72 | Input leakage current (Values added for neg. temperature range, XTAL1) |
| 72 | 72 | Input/Output voltage (addapted to TTL levels, test conditions added) |
| 74 | 74 | Frame strobe delay $t_{FSD}$ (new) |
| 77 | 77 | Bit clock delay $t_{BCd}$ = 25 ns (changed)<br>DSYNC delay $t_{DSYNC}$ (new) |

**Edition 08.97**

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# 1 Overview

The four channel ADPCM Controller PEB 7274 (Quad ADPCM) features four independent full duplex Adaptive Differential Pulse Code Modulation voice coders with individually selectable compression down to 16, 24, 32 or 40 kbit/s as specified by CCITT Recommendation G.726. A-law, µ-law or 16-bit linear operation is provided.

An optional echosupression algorithm is included as well as Artificial Echo loss insertion and a programmable tone generation.

The device is optimized for operation in PCM-4 and PCM-8 systems together with the PEB 2466 SICOFI-4-µC and the PEB 2091 IEC-Q V5.x. An internal FAX/Modem recognition allows simple allocation of the data rate needed for modem transmission or connection of modems/data rate convertors as the PSB 7110 ISAR.

The Quad ADPCM provides two PCM interfaces allowing free selection of input and output time slots via register bit setting. A bypass mode facilitates data over voice applications.

Flexible applications are supported by connecting a low cost microcontroller via a serial processor interface. Indirect access to DSP RAM is provided via the controller interface.

Additional frame synchronization signals for each channel with selectable timing conditions allow the direct connection to standard codec filters.

The Quad ADPCM is a low power consuming CMOS device. It comes in a P-MQFP-44 package.

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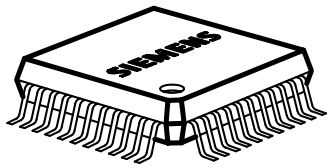
# 4 Channel ADPCM Controller PEB 7274
# Quad ADPCM

**PEF 7274**

**Version 1.2** **CMOS**

## 1.1 Features




**P-MQFP-44**

- 4 full duplex ADPCM Voice Coders
- 16/24/32/40 kbit/s compression rate
- CCITT G.726, G.721 compliant
- Compression rate individually programmable during operation
- Cascadable for PCM-8 Systems
- Parameterizable Echosupression
- Programmable tone generation
- A-Law, µ-Law or 16 bit linear operation
- Pprogrammable FAX/Modem-tone detection, compliant to G.164
- Optional Artificial Echo Loss compliant to ETSI ETS 300 175
- Stand-alone operation in PCM-4 Systems without microcontroller
- A-law or µ-law default set per pin strapping
- 2 PCM-Interfaces 1.536, 2.048 or 4.096 MHz providing 12 to 64 time slots
- Frame Strobe Signals for standard codec filters, long frame and short frame timing
- Serial Microcontroller Interface
- DECT synchronization clock
- JTAG Boundary Scan compliant to IEEE 1149.1
- Sub-micron CMOS Technology
- P-MQFP-44 Package

| Type | Ordering Code | Package |
|---|---|---|
| PEB 7274 | Q67101-H6678 | P-MQFP-44 |
| PEF 7274 | Q67101-H6893 | P-MQFP-44 |

## 1.2 Logic Symbol

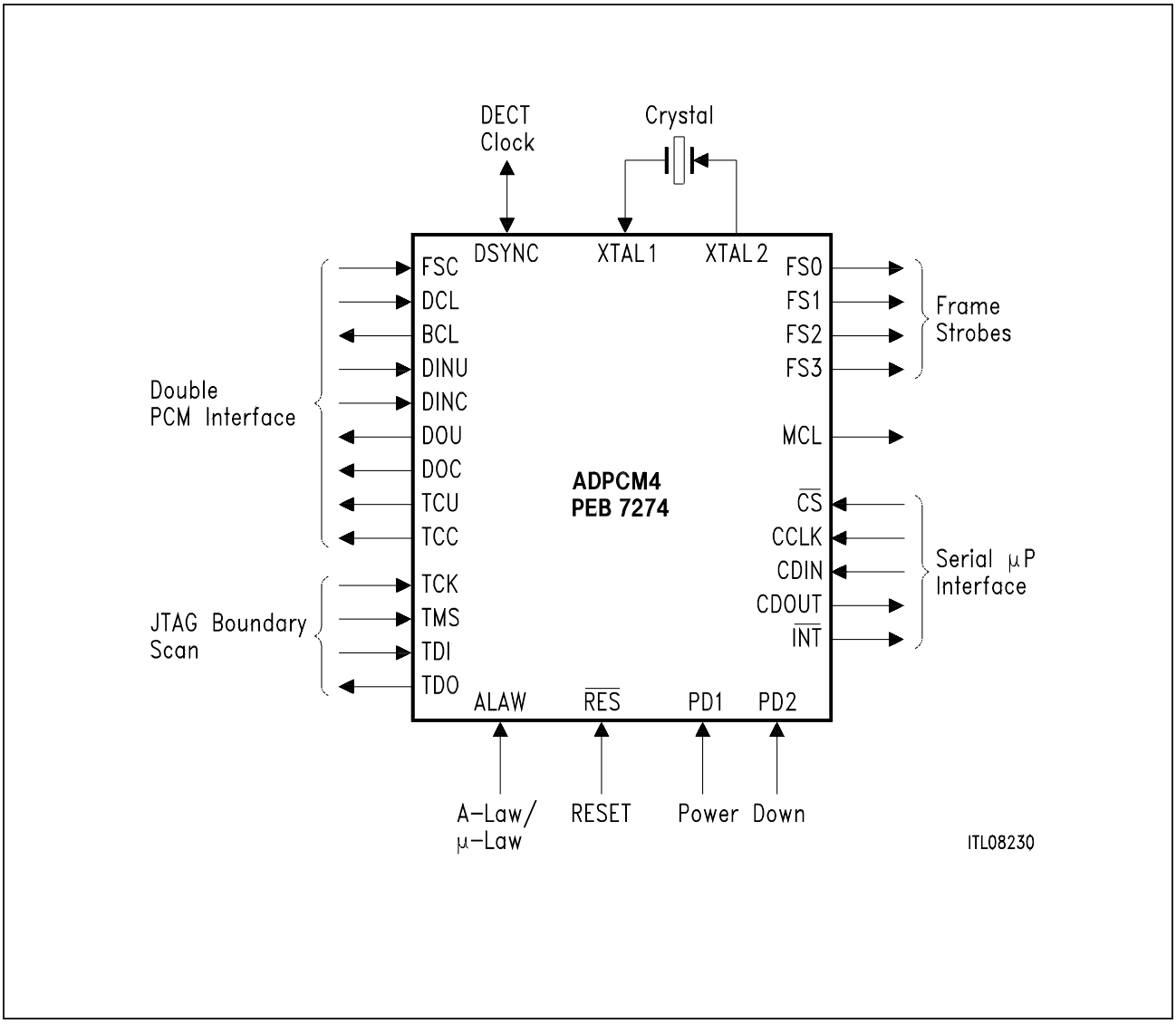



**Figure 1 Logic Symbol**

## 1.3 Pin Configuration

(top view)

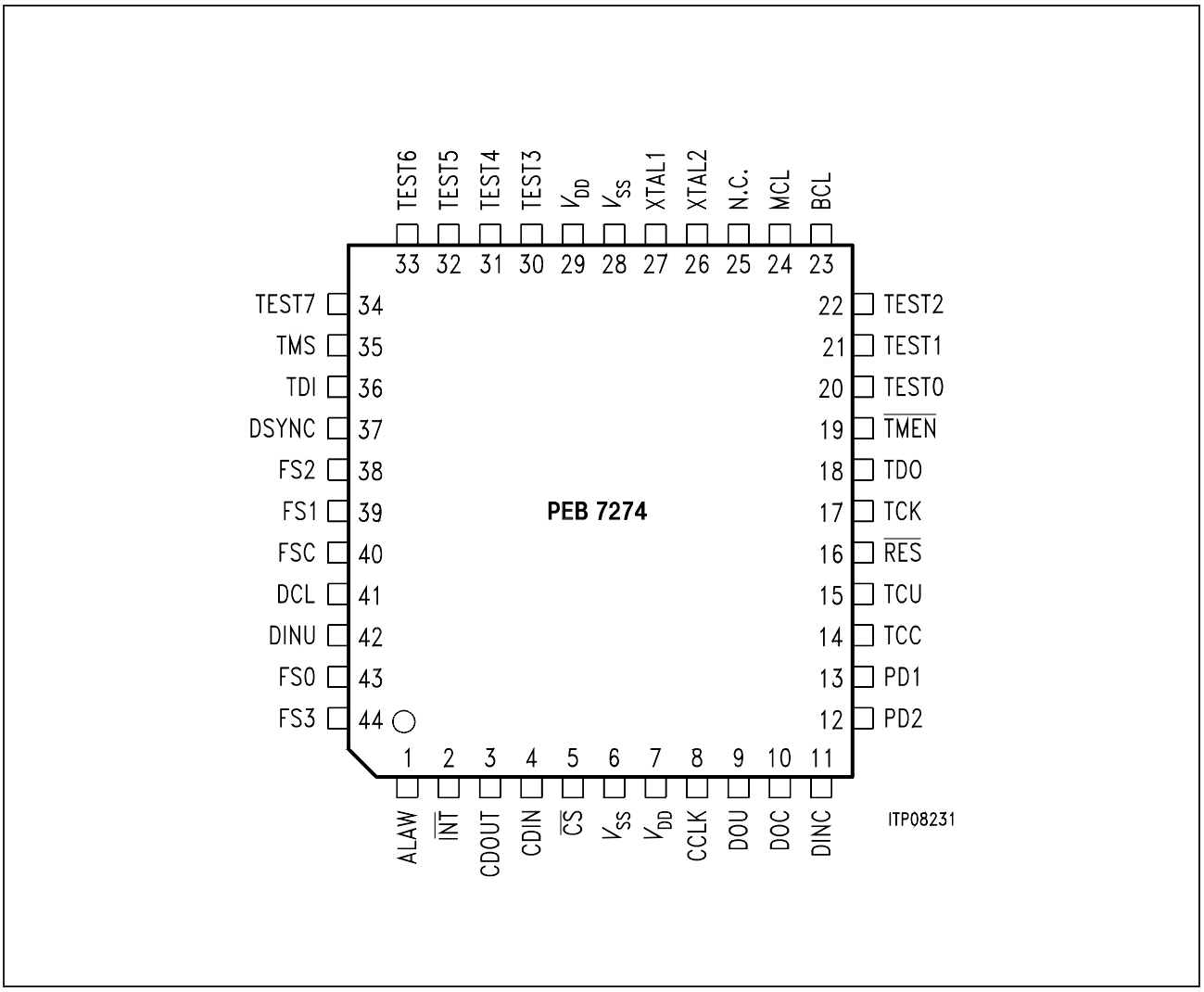



**Figure 2 Pin Configuration (top view)**

## 1.4 Pin Definitions and Functions

| Pin No. | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| **Power Supply Pins** | | | |
| 7, 29 | $V_{DD}$ | I | Supply Voltage (5 V +/-5 %) |
| 6, 28 | $V_{SS}$ | I | Ground (0 V) |
| **JTAG Boundary Scan** | | | |
| 17 | TCK | I | Test Clock |
| 35 | TMS | I | Test Mode Select, internal pullup |
| 36 | TDI | I | Test Data Input, internal pullup |
| 18 | TDO | O | Test Data Output |
| **PCM Interface** | | | |
| 11 | DINC | I | Data in Compressed. Input of ADPCM data synchronous to DCL clock |
| 10 | DOC | O (OD) | Data out Compressed. Output of ADPCM data synchronous to DCL clock. Open drain. |
| 42 | DINU | I | Data in Uncompressed. Input of PCM data synchronous to DCL clock |
| 9 | DOU | O (OD) | Data out Uncompressed. Output of PCM data synchronous to DCL clock. Open drain. |
| 40 | FSC | I | Frame synchronization clock. The start of time slot 0 is marked. |
| 41 | DCL | I | Data clock. Clock range 1.536 to 4.096 MHz. |
| 23 | BCL | O | Bit clock. Half the DCL clock is output on this pin.<br>*Note: This pin is not included in the boundary scan path.* |
| 14 | $\overline{TCC}$ | O | Transmit Control Compressed, low active. TCC is low during the slots data is transmitted on DOC. |
| 15 | $\overline{TCU}$ | O | Transmit Control Uncompressed, low active. TCU is low during the slots data is transmitted on DOU. |

| Pin No. | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| Microcontroller Interface | | | |
| 5 | $\overline{CS}$ | I | Chip Select enable to read or write data, active low. Connect to $V_{DD}$ if not used. |
| 8 | CCLK | I | Controller data clock. Shifts data from or to the device. Connect to $V_{DD}$ if not used. |
| 4 | CDIN | I | Controller Data In. CCLK determines the data rate. Connect to $V_{DD}$ if not used. |
| 3 | CDOUT | O | Controller Data Out. CCLK determines the data rate. CDOUT is "high Z" if no data is transmitted. |
| 2 | $\overline{INT}$ | O (OD) | Interrupt. Low active, open drain. |
| Miscellaneous Function Pins | | | |
| 24 | MCL | O | Master Clock. The crystal clock is output to act as a DSP master clock for another Quad ADPCM. The signal is enabled by setting the bit ADF2:MCE.<br>*Note: This pin is not included in the boundary scan path.* |
| 43 | FS0 | O | Frame Sync 0. High during the time the uncompressed data of channel 0 is active on the PCM bus. |
| 39 | FS1 | O | Frame Sync 1. High during the time the uncompressed data of channel 1 is active on the PCM bus. |
| 38 | FS2 | O | Frame Sync 2. High during the time the uncompressed data of channel 2 is active on the PCM bus. |
| 44 | FS3 | O | Frame Sync 3. High during the time the uncompressed data of channel 3 is active on the PCM bus. |
| 1 | ALAW | I | Select A-law (ALAW = high) or µ-law (ALAW = low) as default setting after reset. |

Miscellaneous Function Pins (cont'd)

| | | | |
|---|---|---|---|
| 16 | $\overline{\text{RES}}$ | I | Master Reset, low active. |
| 27 | XTAL1 | I | Crystal In. 20.48 MHz crystal or 20.48 MHz clock signal is connected. |
| 26 | XTAL2 | O | Crystal Out. 20.48 MHz crystal is connected. Leave open, if no crystal is connected. |
| 37 | DSYNC | I/O | DECT Sync. Output or Input of 800 ms or 2.4 s DECT master clock. |
| 13 | PD1 | I | Power Down 1. A '1' disables DSP 1. DSP 1 holds operation of channels 0 and 1. Also disables data input and output on the compressed side as well as the DECT-sync generation. |
| 12 | PD2 | I | Power down 2: A '1' disables DSP 2. DSP 2 holds operation of channels 2 and 3. Disables Congestion tone generator. |
| 20, 21, 22, 30, 31, 32, 33, 34 | TEST0.. TEST7 | O | Test pins. Used for production testing only. Do not connect. |
| 19 | $\overline{\text{TMEN}}$ | I | Test pin. Used for production testing only. Active low. Internal pullup. Do not connect. |

## 1.5 Functional Block Diagram

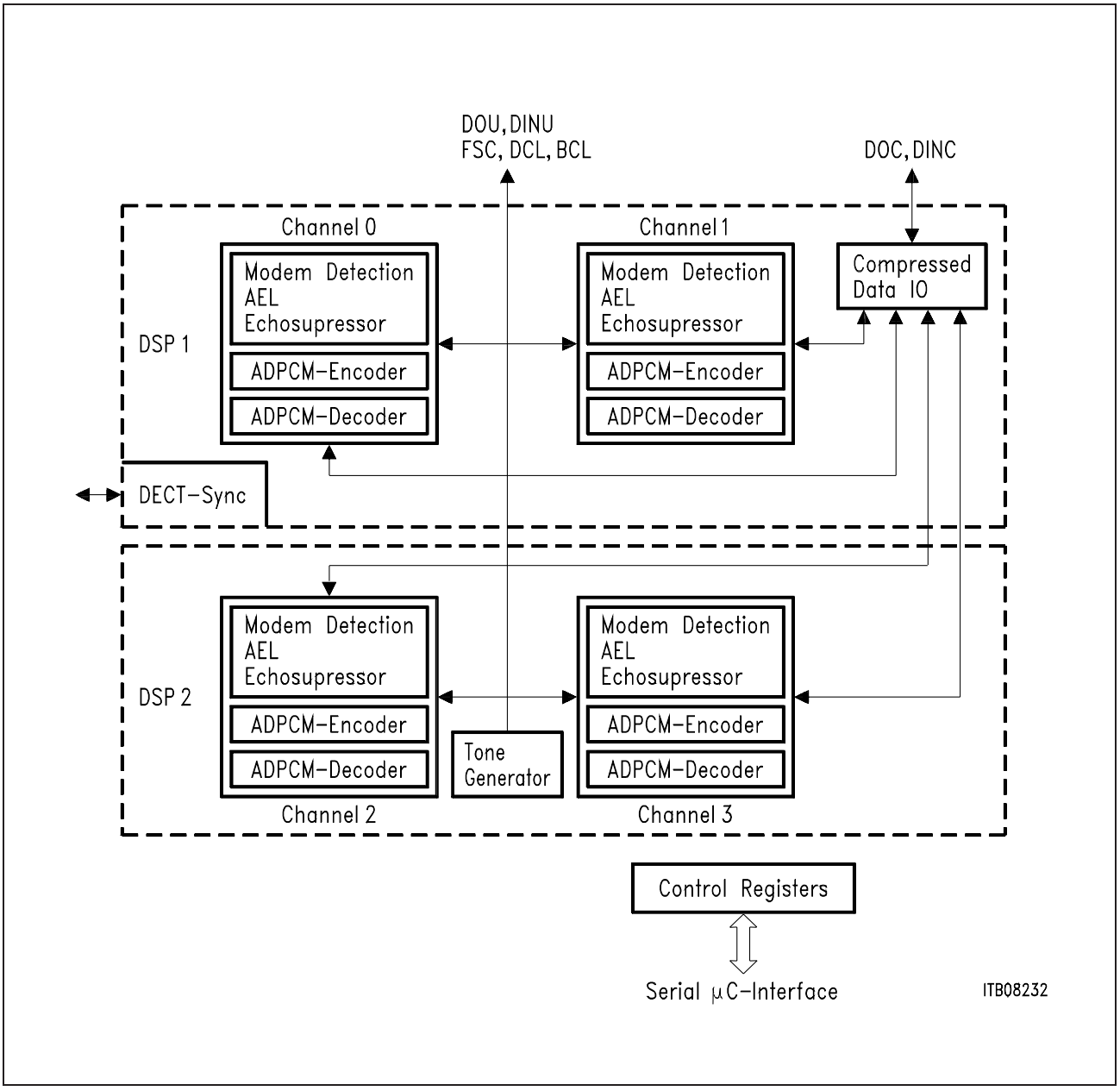



**Figure 3 Block Diagram**

Two DSP cores contain two ADPCM coders each. The I/O of the compressed data is handled by DSP 1. The tone generator resides in DSP 2. Hence, if DSP 1 is disabled (pin PD1 high), no input/output of compressed data of all four channels is possible. If DSP 2 is disabled, no tone generator is provided.

## 1.6 System Integration

### 1.6.1 PCM-4 System

**Figure 4** gives a general overview of integration in a PCM-4 system. The register set of the Quad ADPCM is in a default configuration. No connection to the microcontroller is necessary. The PCM interface is working with a double data clock of 1.536 MHz coming from the IEC-Q V5.x. This corresponds to a number of 12 PCM time slots or 3 IOM-channels respectively. The DINU and DINC pins are tied together as well as the DOU and DOC pins. This way, the two PCM busses are using the same physical lines. The IEC-Q is in the NT-TE-1536 mode at the NT side and the COT-1536 mode at the LT side. It uses the PCM slots 0 and 1. There, the Quad ADPCM reads and writes the compressed data. It takes the uncompressed data from the time slots 4, 5, 8 and 9 (see figure below, the most left timeslot being slot 0). The SICOFI-4-µC is programmed to read/write these time slots.

Note that the IEC-Q uses an IOM-2 interface where control information such as C/I-commands and Monitor messages are exchanged on time slots 2 and 3. These time slots should consequently not be used to exchange compressed or uncompressed data.

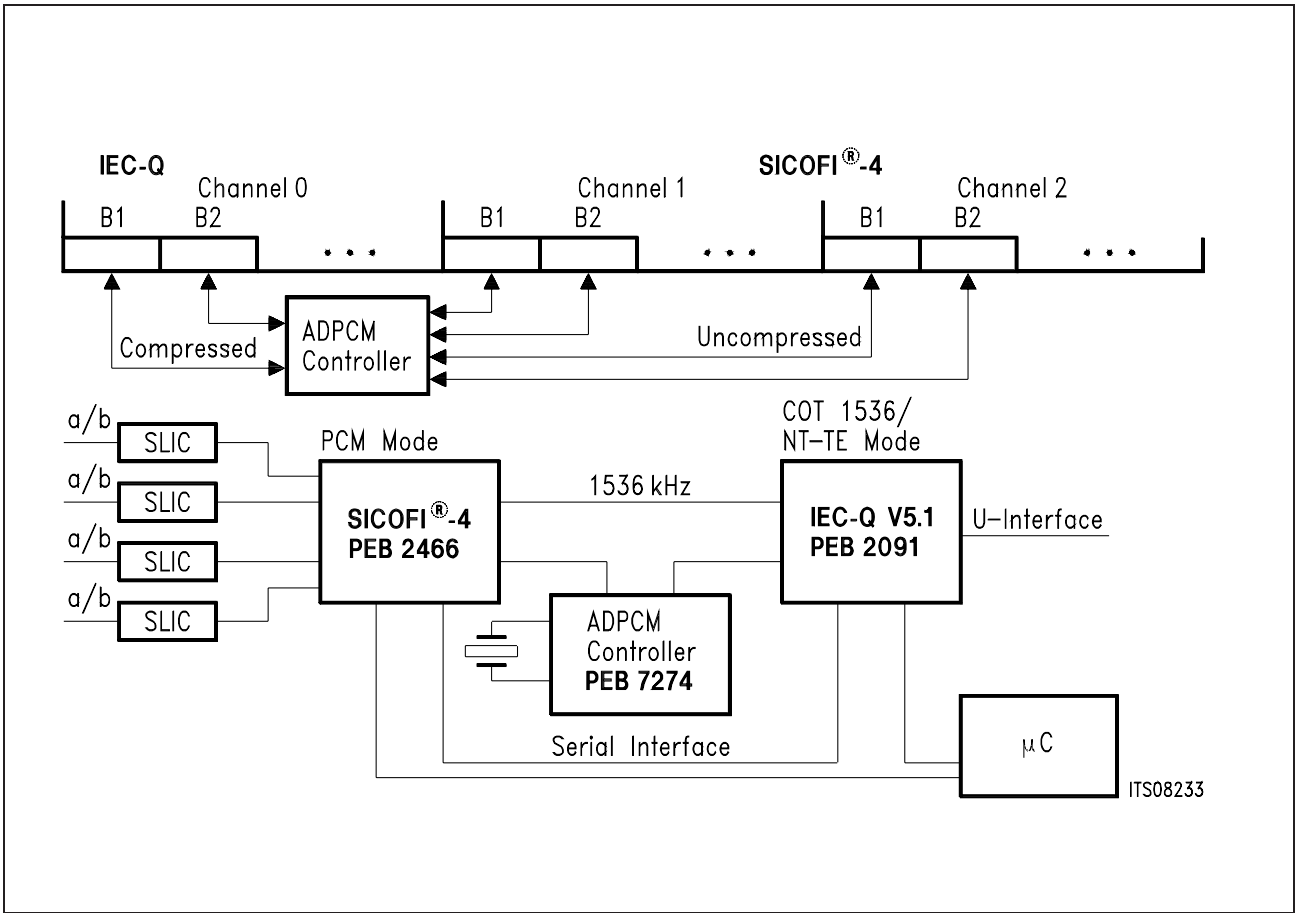



**Figure 4 Integration in PCM-4 System**

The SICOFI-4-µC uses the 1.536 MHz PCM clock to internally generate its masterclock. The IEC-Q also issues a 7.68 MHz clock. This clock can be used as microcontroller clock. The IEC-Q V5.x allows to program this clock rate between 0.92 and 7.68 MHz.

The automatic modem detection enables the PEB 7274 Quad ADPCM to monitor the compressed and uncompressed side of the PCM highway in all four channels in parallel. This allows to dynamically allocate the data rate needed for the transmission of high speed modem signals or to hand over the control to the PSB 7110 ISAR. The Quad ADPCM detects a fax/modem tone. The microcontroller then sets the compressed output of the according channel to a highly impedant state. The PSB 7110 ISAR takes over the uncompressed receive data, performs modem operation and data rate adaptation and passes the output data onto the timeslot left open by the Quad ADPCM.

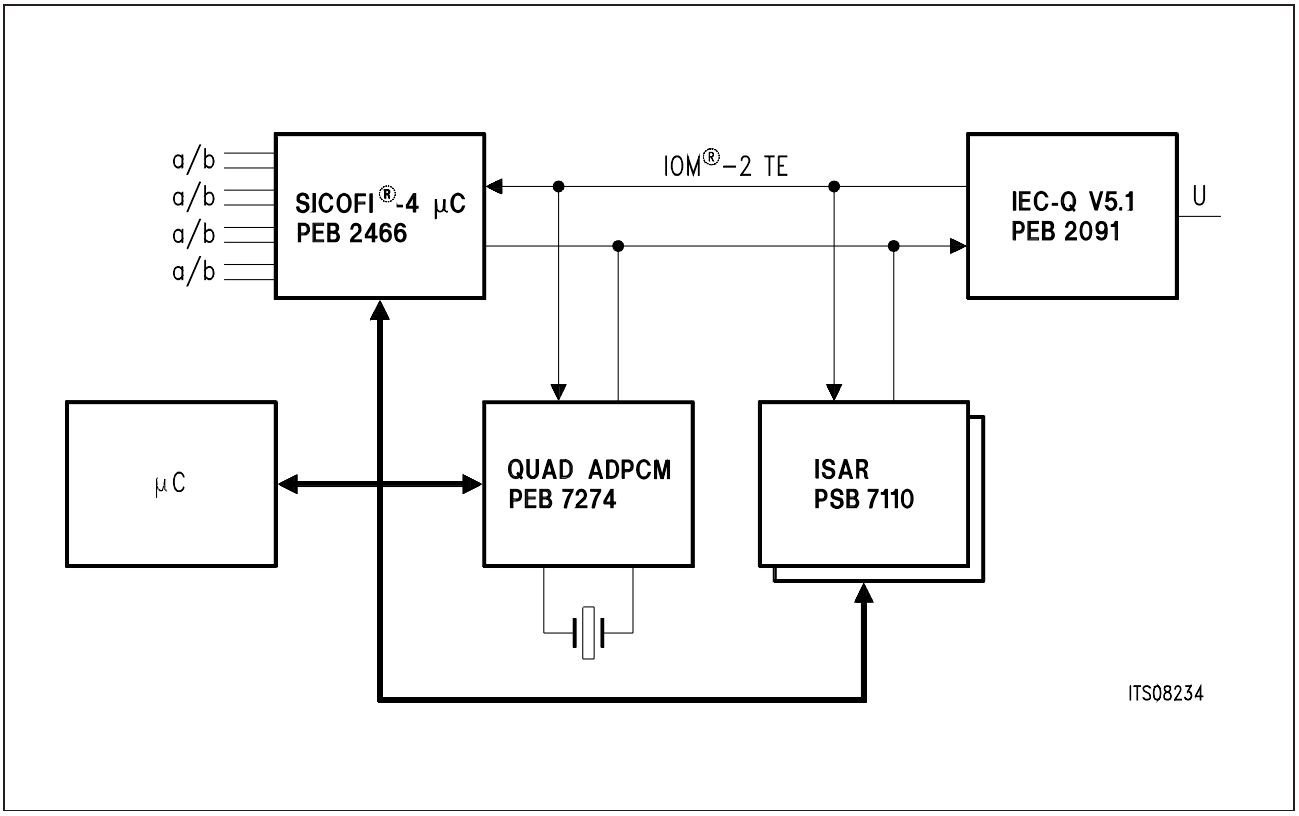



**Figure 5 Integration in PCM-4 System with Automatic Modem Handling**

Two PSB 7110 ISAR provide 14.4 kbit/s modem transmission on all four channels. The ISAR occupies 3 bit leaving 5 bit for direct 14.4 kbit/s modem transmission. One ISAR can be used if fax operation is not expected on all four channels simultaneously.

### 1.6.2 PCM-4 System using Standard Codec Filters

The Quad ADPCM provides additional frame sync signals for each channel. In case the data clock is not at a rate of 1.536 MHz, it has to be generated with an additional PLL. The microcontroller selects the appropriate timing conditions for the frame sync pulses. Short frame and long frame mode are provided.

An additional bit clock (BCL) allows to easily connect single clock mode devices (e.g. CODECs) and double clock mode devices (e.g. IEC-Q V5.x) as well.

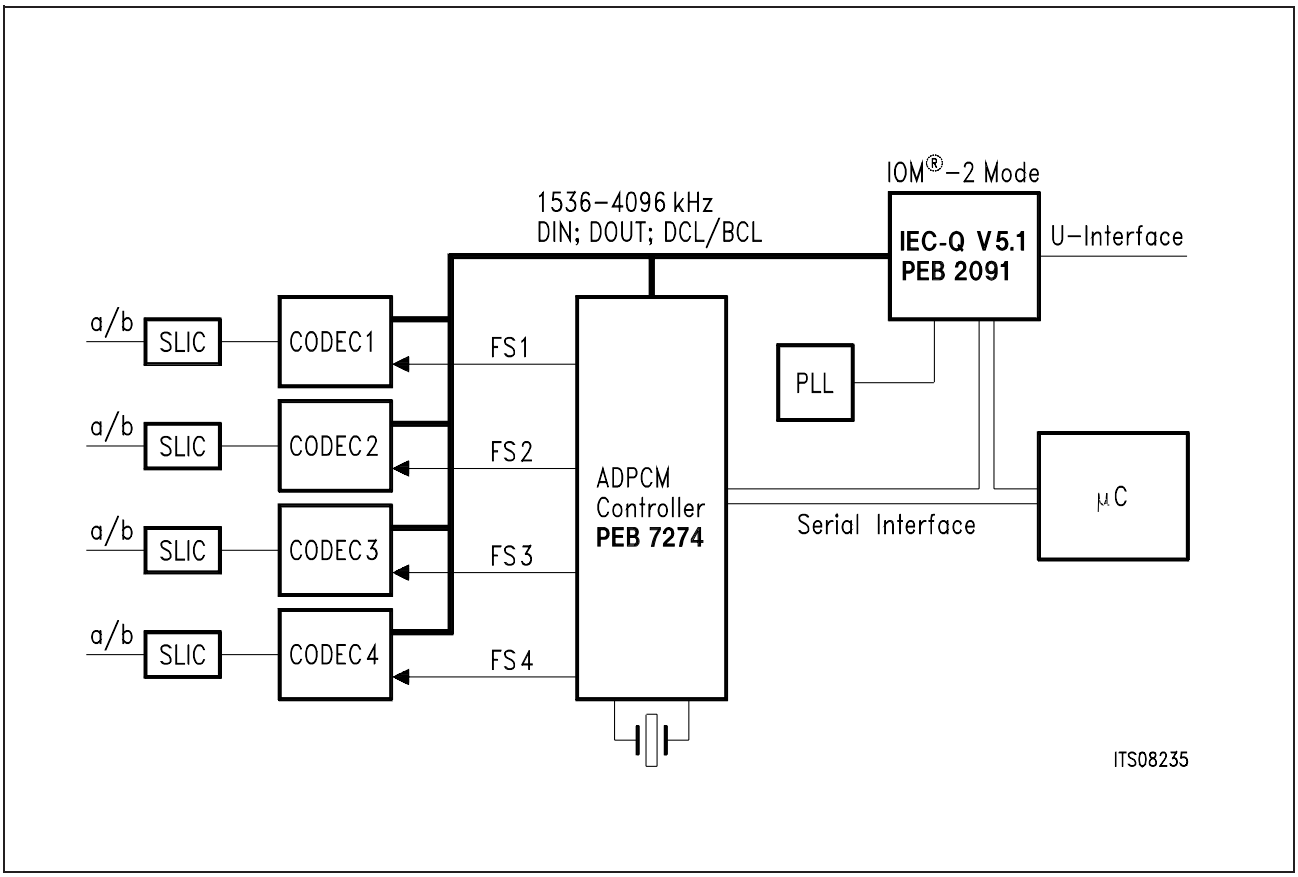



**Figure 6 Integration in PCM-4 Systems using Standard Codec Filters**

### 1.6.3 PCM-8 System

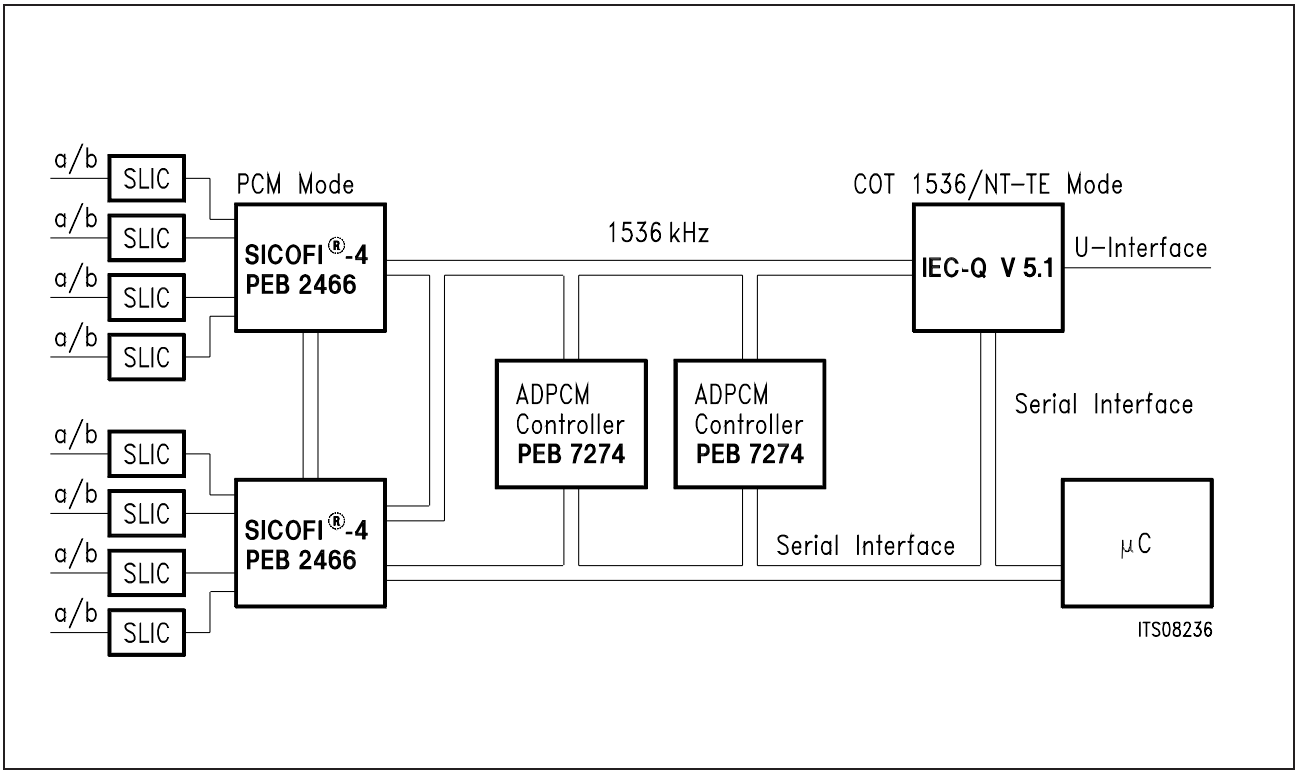



**Figure 7 Integration in PCM-8 Systems**

**Figure 7** depicts an integration in a PCM-8 system. The PCM interface is working with a double data clock of 1.536 MHz coming from the IEC-Q V5.x. This corresponds to a number of 12 PCM time slots or 3 IOM-channels respectively. The IEC-Q is in the NT-TE-1536 mode at the NT side and the COT-1536 mode at the LT side. It uses the PCM slots 0 and 1. There, the two Quad ADPCM read and write the compressed data. They take the uncompressed data from the time slots 4 to 11 (time slots count 0 to 11). The two SICOFI-4-µC are programmed to read/write these time slots. The DINU and DINC pins of both Quad ADPCM are tied together as well as the DOU and DOC pins. This way, the two PCM busses of the Quad ADPCM are using the same physical lines. This is possible by proper time slot assignment.

Note that the IEC-Q uses an IOM-2 interface where control information such as C/I-commands and Monitor messages are exchanged on time slots 2 and 3. These two slots should not be used for compressed or uncompressed data transfer.

No additional clock generator for the PCM data clock is necessary because the 1.536 MHz PCM clock is issued by the IEC-Q.

The IEC-Q also issues a 7.68 MHz clock which can be used as microcontroller clock.

### 1.6.4 DECT Linecard

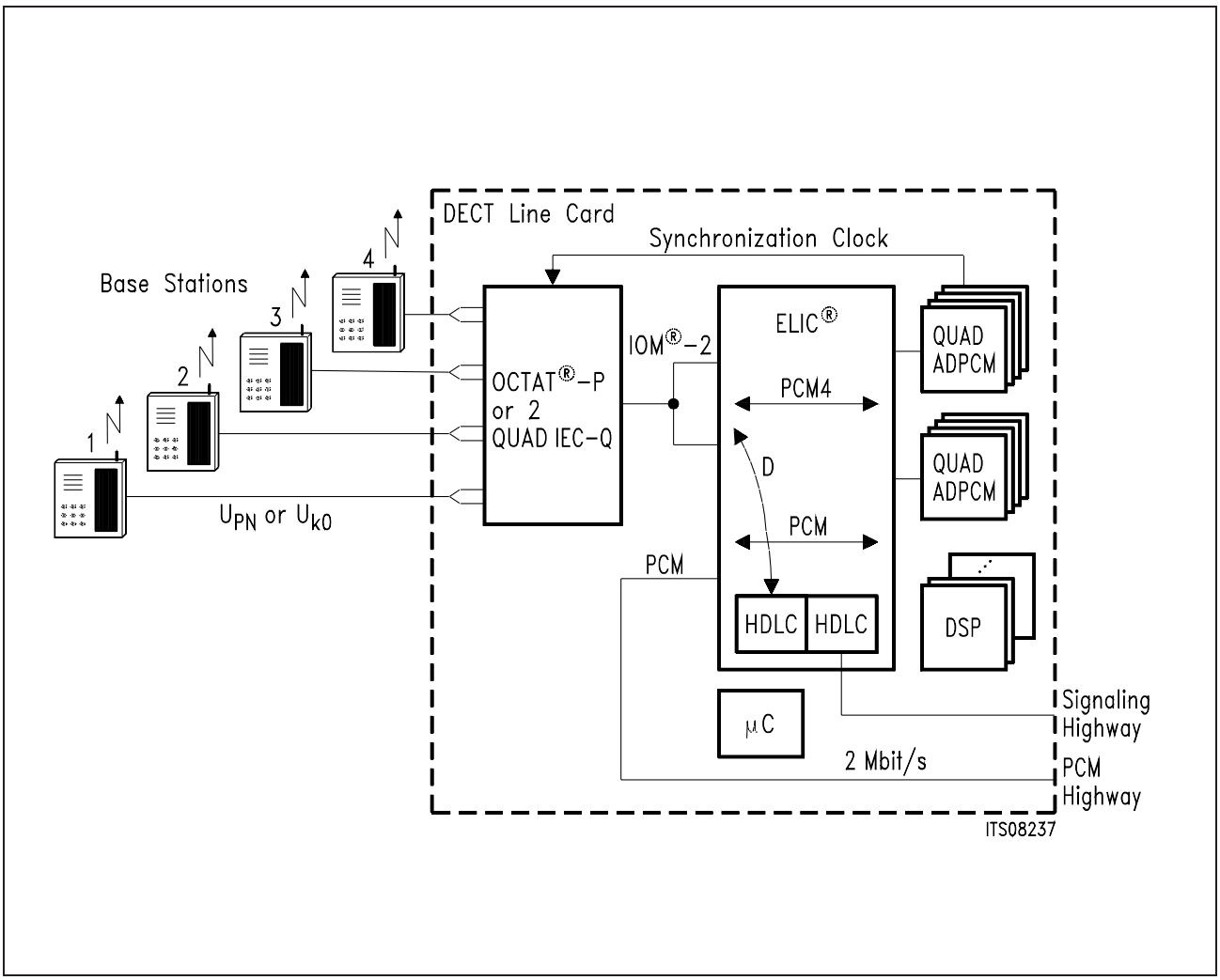



**Figure 8 Integration in a DECT Linecard**

Figure **8** presents the integration in a linecard for a PBX featuring DECT basestations. The Quad ADPCM features flexible access to arbitrary time slots of the PCM highway by it's two PCM interfaces. One of the Quad ADPCM provides a DECT synchronization clock of either 800 ms or 2.4 s period. The other Quad ADPCM receive this clock for synchronized reprogramming of e.g. the data rates or other registers.

Together with the PEB 2096 OCTAT-P or the PEB 24902/PEB 24911 Quad IEC-Q as layer-1 transceivers, seamless handover is possible in the linecard.

# 2 Functional Description

## 2.1 ADPCM Coder

The Quad ADPCM contains two DSP cores each implementing the algorithms for two channels. It supports full duplex ADPCM coding and encoding as specified by CCITT recommendation G.726. A-law, µ-law and 16 bit linear operation are selectable separately for each channel by setting the UTi-register corresponding to channel i.

The synchronous coding adjustment (SCA) unit of the decoder (see fig. **10**) prevents cumulative distortion occurring on tandem operation, e.g. ADPCM - PCM - ADPCM. It can optionally be disabled to improve the signal/noise ratio when going from PCM to analog coding.

Figure **9** shows the structure of the encoder as given in CCITT rec. G.726.

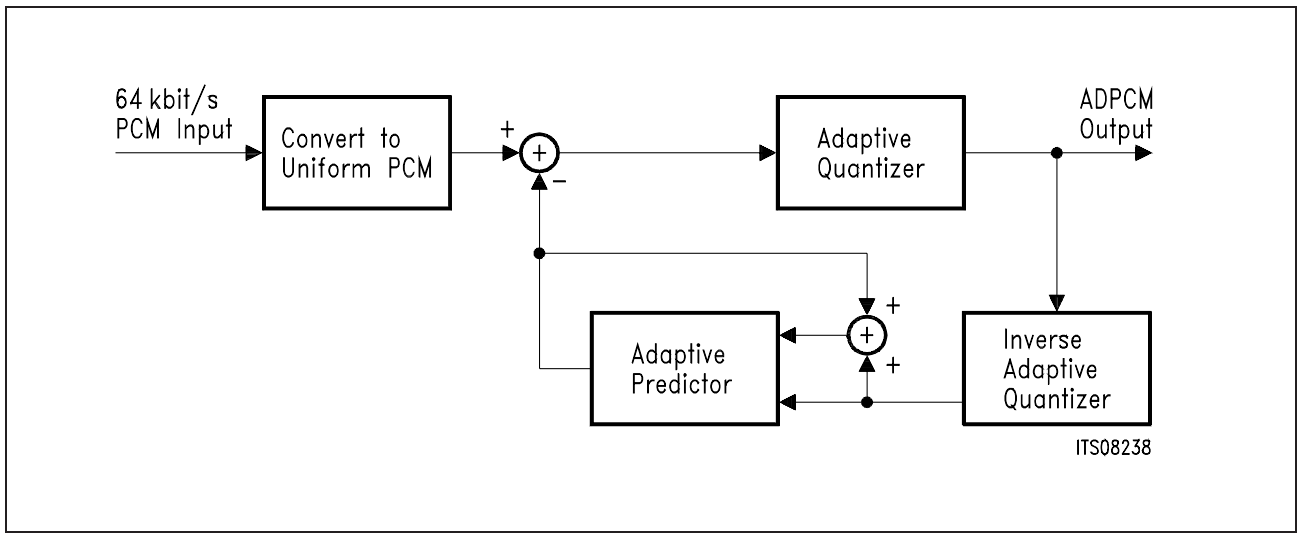



**Figure 9 Encoder Block Diagram**

Figure **10** illustrates the structure of the decoder.

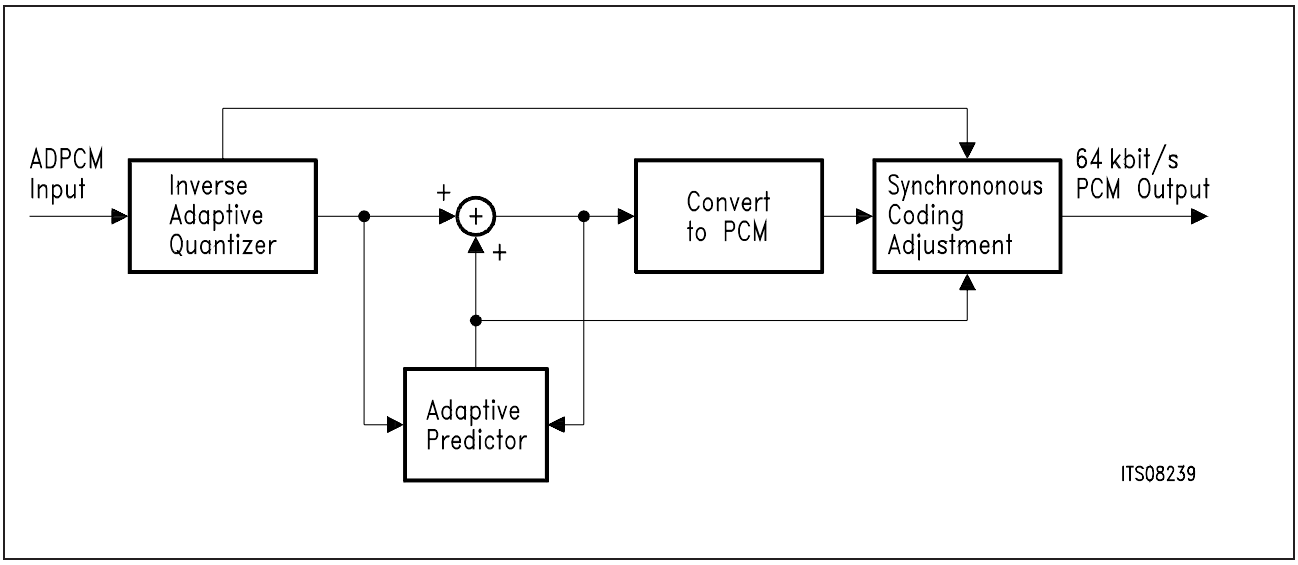



**Figure 10 Decoder Block Diagram**

## 2.2 PCM Interface

The Quad ADPCM allows most flexible use of the PCM interface. It can select the time slots of the four uncompressed data streams as well as the beginning of the compressed data stream via register programming. There is a data-in line for the uncompressed data (pin DINU) and a data-in line for the compressed data (pin DINC) as well as two data-out lines for uncompressed data and compressed data respectively (pins DOU and DOC). If the time slots of both data streams do not overlap, both outputs and both inputs can be electrically connected.

Four time slots can be assigned to the four uncompressed data streams. They select the input as well as the output of the uncompressed data. The uncompressed channel assignments are controlled by the UTi registers (i being the channel number 0..3). In case of single clock mode the bit MSB:UTMi is used to extend the programming range to a maximum of 64 time slots.

The compressed data can start at any bit. The four compressed data streams are tied together. The compressed data of channel 0 comes first, then the compressed data of channel 1 etc. In the DPP register, the number *n* of the first compressed data bit is selected. Depending on the compression rate, two, three, four or five compressed bits will be placed at the bit positions *n*, *n+1*, *n+2* etc. The first compressed bit of the second channel directly follows the last bit of the first channel. The first bit of the third channel directly follows the last bit of the second channel etc. If the compression rate is changed the bit positions of the higher channels change as well. In case of bitwise bypassing or a combination of compression and bypassing the same principle applies.

Figure **11** illustrates the relation of the frame sync signal at the FSC pin, the numbering of the bits in the frame and the beginning of the slots. Double data clock mode is

assumed. The user has to take care not to 'overlap' data by multiple allocation of channels to same timeslots.

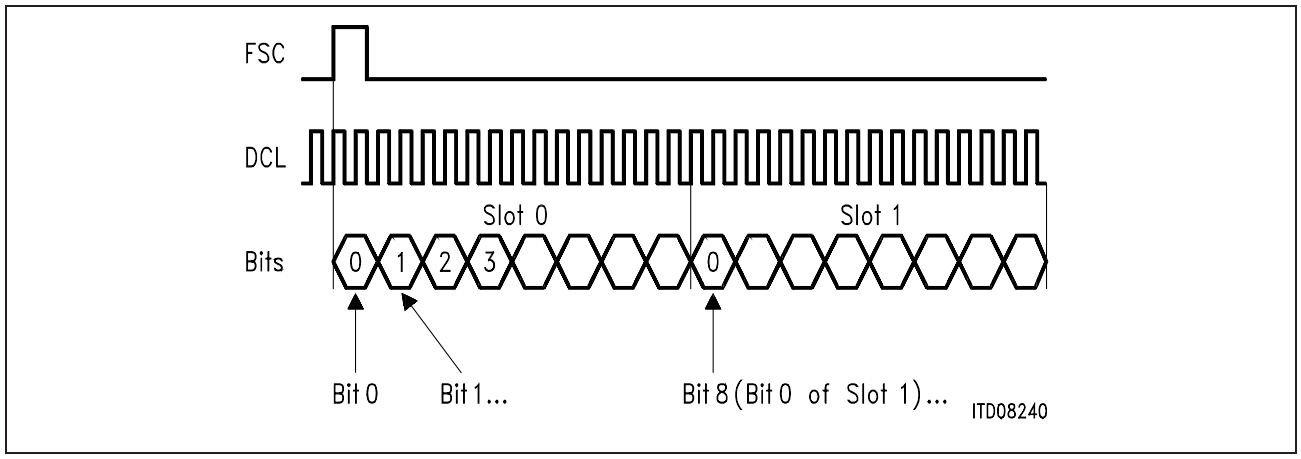



**Figure 11 Allocation of Data to Slots and within the Slots**

The rising edge of the FSC marks the start of the 125 µs frame. Each slot consists of 8 bits. The beginning of the compressed data can be set to every bit of the frame as given in figure **11**. The compressed channel assignment is programmed via the register DPP. In case of single clock mode at 4.096 MHz only the first 256 bits may be selected as start position. Care has to be taken by proper programming of the DPP and UTi registers not to overlap data if the two PCM interfaces shall work on one PCM highway.

Input data and output data is always allocated to the same time slots.

Start and execution time of the DSP programs are such that coding and decoding are performed in one single frame if the slot assignment is properly chosen. That is, for the default time slot assignment as given in figure **4** as well as for the PCM-8 system shown in figure **7**, the propagation delay through two ADPCM channels in a system (coding on one side, decoding on the other side) is one single frame.

## 2.3 Propagation Delay

The begin of the decoder and the encoder program is tied to the frame clock at FSC. It is optimized to provide a one frame group delay for the complete encoding/decoding operation on all four channels if the time slots of uncompressed data and compressed data are assigned properly.

Figure **12** gives the location of the decoder start time and the encoder start time in the frame. If the uncompressed input data is read in the time slots before the encoder starts, it is available to the compressed output immediately after the encoder stops. If the compressed input data is read before the decoder starts, the uncompressed data is available to the uncompressed output immediately after the decoder stops. In the example of figure **12**, the uncompressed data is read at the time slots 4, 5, 8 and 9 before the encoder starts. It is compressed during time slot 11 and put to the DOC pin in time slots 0 and 1 of the next frame.

The compressed data is read at time slots 0 and 1 before the decoder starts. It is decoded during time slots 2 and 3 and put to the DOU pin during time slots 4, 5, 8 and 9 in the same frame it has been read. Note that the decoding takes longer than the encoding.

Hence, with the default time slot assignment as described in section **1.6.1**, the delay to compress data is one frame and the uncompressed data is available in the same frame.

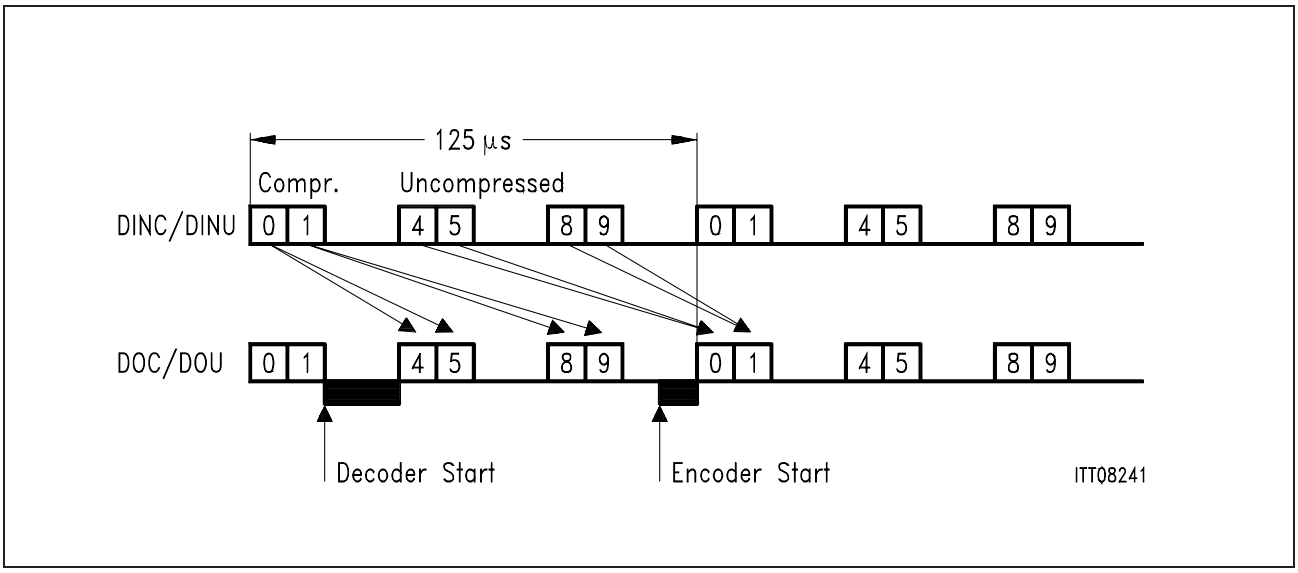



**Figure 12 Decoder / Encoder Timing in a PCM-4 System**

If two Quad ADPCM devices are put together in a PCM-8 system and the DCL clock is 1.536 MHz, there are not enough time slots for the uncompressed data left before the start of the encoder. Therefore, the encoder start position can be shifted to the begin of the frame by setting the ADF2:ENS bit to '1'. If this is done in one of the two Quad ADPCM, the timing as given in figure **13** results.

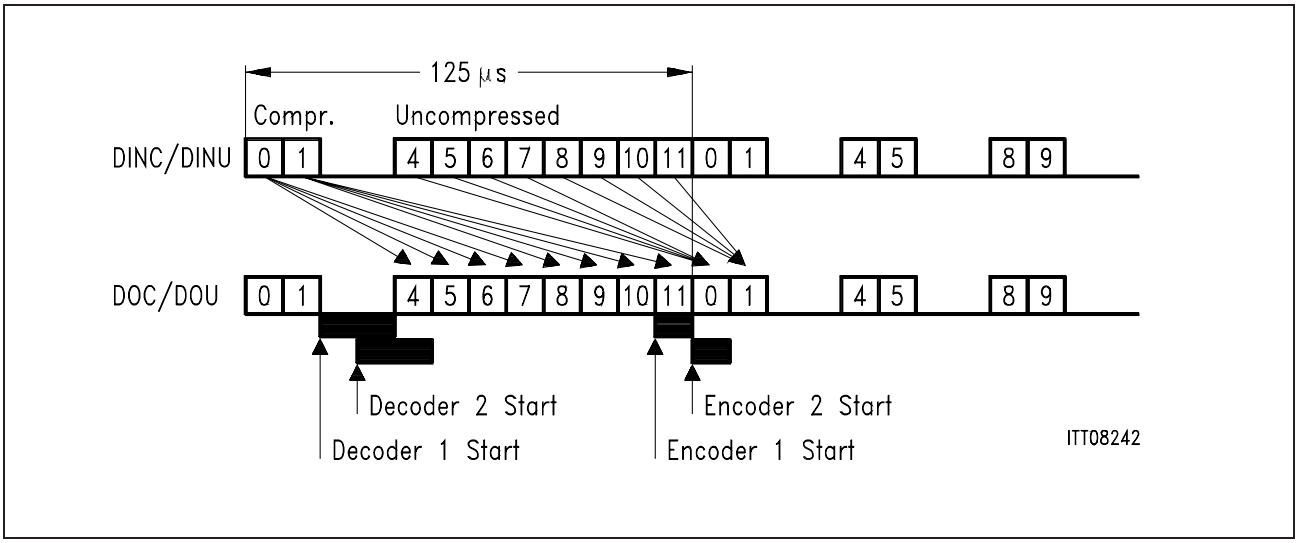



**Figure 13 Decoder / Encoder Timing in a PCM-8 System**

The uncompressed data of slots 4 to 7 is processed during time slot 11 in the encoder of device 1 and passed to DOC at slot 0 of the next frame. The uncompressed data of slots 8 to 11 is processed during slot 0 of the next frame and put to DOC at slot 1. Again, all channels have a one frame delay for the complete encoding/decoding operation.

If the time slots are not assigned as proposed above, the delay of one or more channels may be two frames.

If the DCL clock rate is higher than 1.536 MHz more than 12 time slots are available. In this case, there are several ways to assign the time slots appropriately for minimum delay. Note however that the encoding time then is longer than one time slot and the decoding takes more than two time slots.

The exact start and end of the decoder and the encoder at the different DCL clock rates is given in the tables below:

**Decoder start after slot number**

| | ADF2:DCLK = 0 | ADF2:DCLK = 1 |
|---|---|---|
| **ADF2:ENS= 0** | 1 | 3 |
| **ADF2:ENS= 1** | 2 | 5 |

**Decoder end after slot number**

| DCL = 1536 kHz | ADF2:DCLK = 0 | ADF2:DCLK = 1 |
|---|---|---|
| **ADF2:ENS= 0** | 3 | 7 |
| **ADF2:ENS= 1** | 4 | 9 |

| DCL = 2048 kHz | ADF2:DCLK = 0 | ADF2:DCLK = 1 |
|---|---|---|
| **ADF2:ENS= 0** | 4 | 9 |
| **ADF2:ENS= 1** | 5 | 11 |

| DCL = 4096 kHz | ADF2:DCLK = 0 | ADF2:DCLK = 1 |
|---|---|---|
| **ADF2:ENS= 0** | 7 | 14 |
| **ADF2:ENS= 1** | 8 | 16 |

**Encoder start after slot number**

| DCL = 1536 kHz | ADF2:DCLK = 0 | ADF2:DCLK = 1 |
|---|---|---|
| **ADF2:ENS= 0** | 10 | 21 |
| **ADF2:ENS= 1** | start of next frame | start of next frame |

| DCL = 2048 kHz | ADF2:DCLK = 0 | ADF2:DCLK = 1 |
|---|---|---|
| ADF2:ENS= 0 | 13 | 27 |
| ADF2:ENS= 1 | 14 | 29 |

| DCL = 4096 kHz | ADF2:DCLK = 0 | ADF2:DCLK = 1 |
|---|---|---|
| ADF2:ENS= 0 | 25 | 51 |
| ADF2:ENS= 1 | 26 | 53 |

**Encoder end after slot number**

| DCL = 1536 kHz | ADF2:DCLK = 0 | ADF2:DCLK = 1 |
|---|---|---|
| ADF2:ENS= 0 | start of next frame | start of next frame |
| ADF2:ENS= 1 | 0 of next frame | 1 of next frame |

| DCL = 2048 kHz | ADF2:DCLK = 0 | ADF2:DCLK = 1 |
|---|---|---|
| ADF2:ENS= 0 | start of next frame | 30 |
| ADF2:ENS= 1 | 0 of next frame | 0 of next frame |

| DCL = 4096 kHz | ADF2:DCLK = 0 | ADF2:DCLK = 1 |
|---|---|---|
| ADF2:ENS= 0 | 28 | 57 |
| ADF2:ENS= 1 | 29 | 59 |

*Note: IF ADF2:ENS is set to ’0’, 16 bit are issued at DOC. If ADF2:ENS is set to ’1’, only 8 bit are issued at DOC.*

## 2.4 Echosuppression and Speech Detection

The PEB 7274 Quad ADPCM has a very flexible echosuppressor integrated. In addition to the direction of the echosuppressor (attenuation on the compressed or uncompressed side) all parameters required to optimize the speech detection and signal suppression are also fully programmable. All parameters are part of the DSP RAM and need to be reprogrammed after every reset. No reset settings exist for DSP RAM parameters. Refer to the section **3.16.1** for the procedure of programming DSP RAM cells.

### 2.4.1 Echosuppression

To account for echos from the far end side with up to 70 ms delay an echosuppressor is implemented in the DSP algorithms of the PEB 7274. Echos mainly result when converting digital speech/data information (e.g. from U interface, $S_0$ interface or DECT interface) into analog tip/ring signals. Depending on the origin of the echo the delay of the echo varies. Figure **14** shows typical sources of echos in a DECT PBX system connected to the public exchange with analog and digital trunk lines.

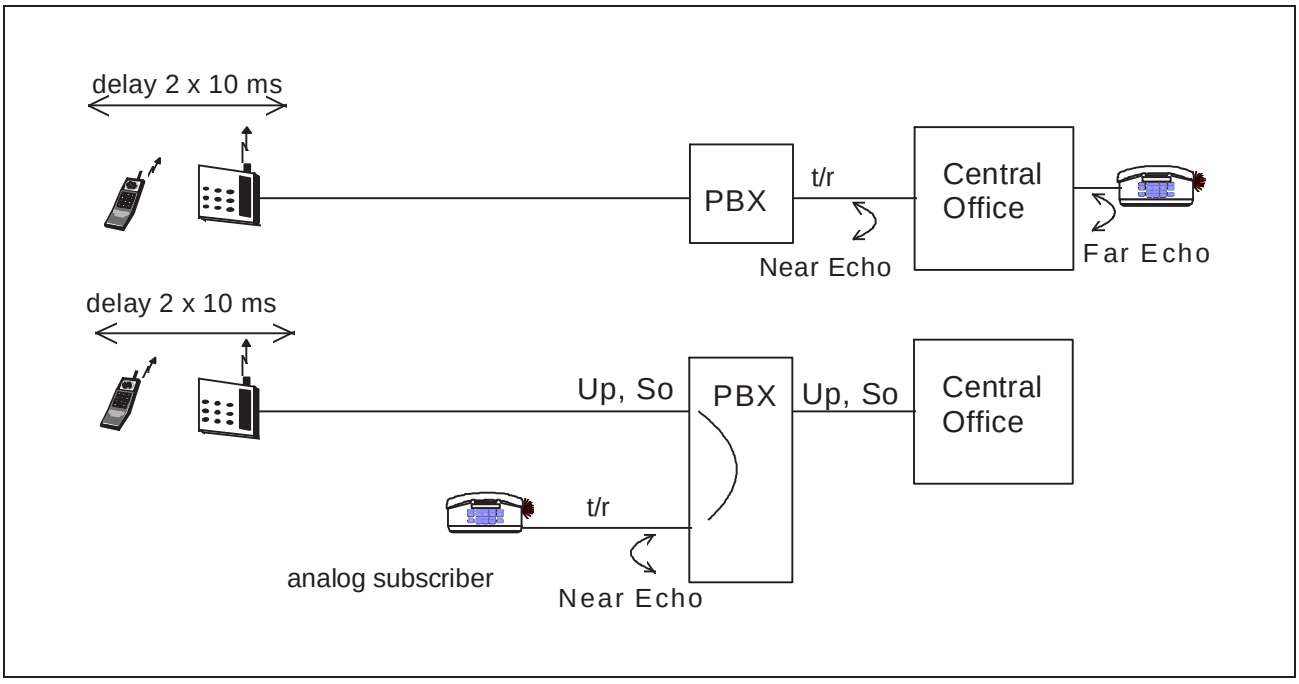



**Figure 14 Echo Sources in a DECT PBX System**

Far end echos are unpredictable with respect to duration and delaytime because these parameters change with each communication connection established. Unlike near end echos where these parameters can only vary within a limited bandwidth far end echos can not be cancelled. The suppression implemented instead consists of a gain stage which adds an additional attenuation to the receive path (typically 9 dB) while speech is recognized in the transmit path and the receive power level does not exceed a specified limit. The receive power level limit guarantees that despite of echosuppression the participant on the other side of the line can switch echosuppression off by speaking loud.

The signal flow path with all programmable echosuppression parameters is illustrated in figure **15**. The programming parameters of the echosuppression are described in section **3.16.6**.

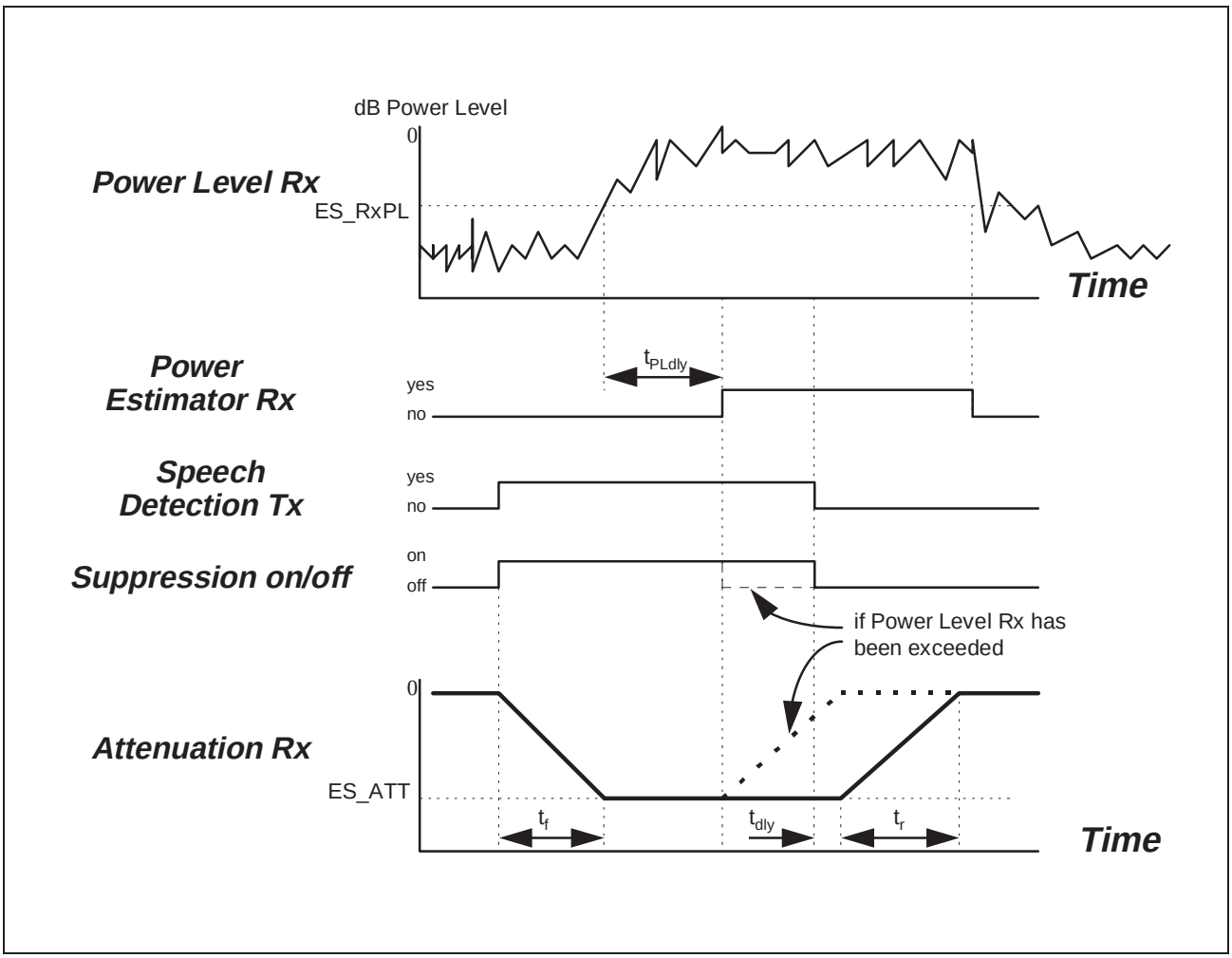



**Figure 15 Echosuppressor Functionality**

The echosuppressor is switched off with time constant $t_r$ without any delay when the estimated receive power level is above the value programmed in ES_RxPL during the time constant $t_{PLdly}$.

As figures **16** and **17** show the PEB 7274 allows also to select the direction of suppression. In DECT systems typically the suppression would be performed on the compressed side (figure **16**). This ensures that local echos which would be noticed by the speaker on side A (handy) due to the 2 x 10 ms delay are attenuated.

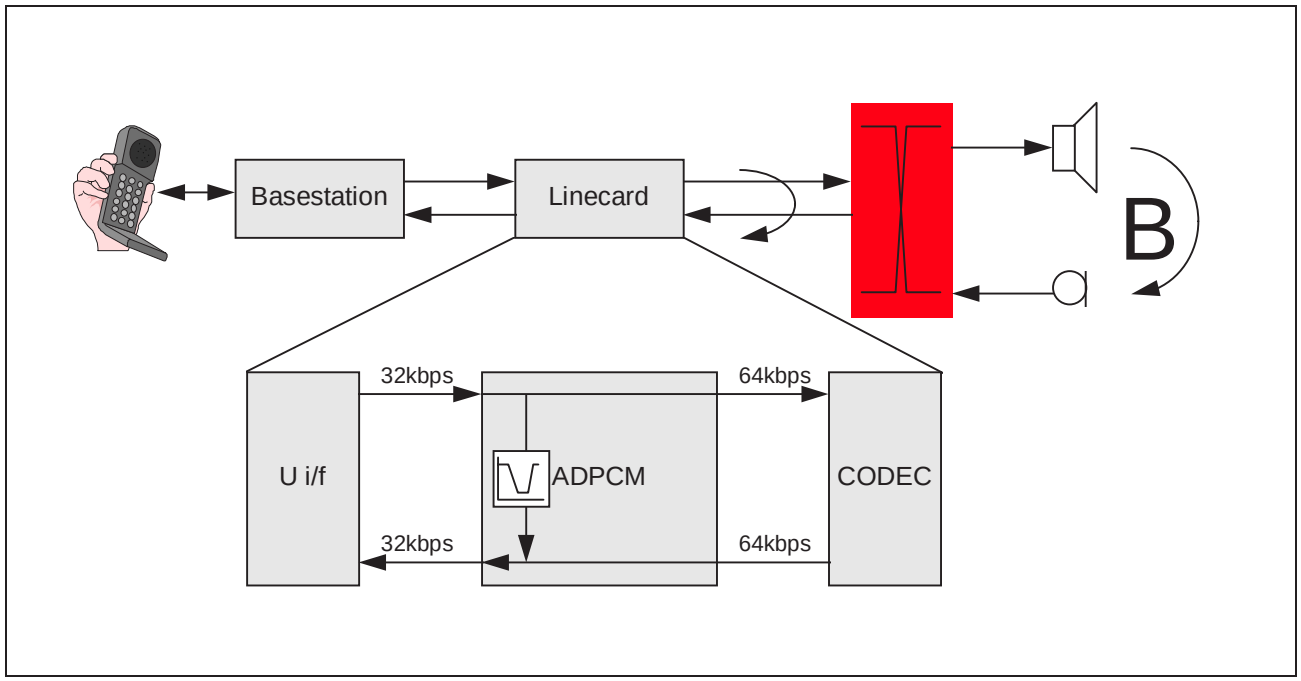



**Figure 16 Echosuppression on the Compressed Side (DECT System)**

In non-DECT systems like PCM-4 applications (i.e. without delay in the order of milliseconds) the far end echo from side B must be attenuated. For this reason the uncompressed PEB 7274 output of side A ( = receive signal containing far end echo) will be suppressed as soon as speech is detected in the transmit path (= uncompressed input of PEB 7274). This guarantees improved speech quality for side A. Refer to figure **17** for details.

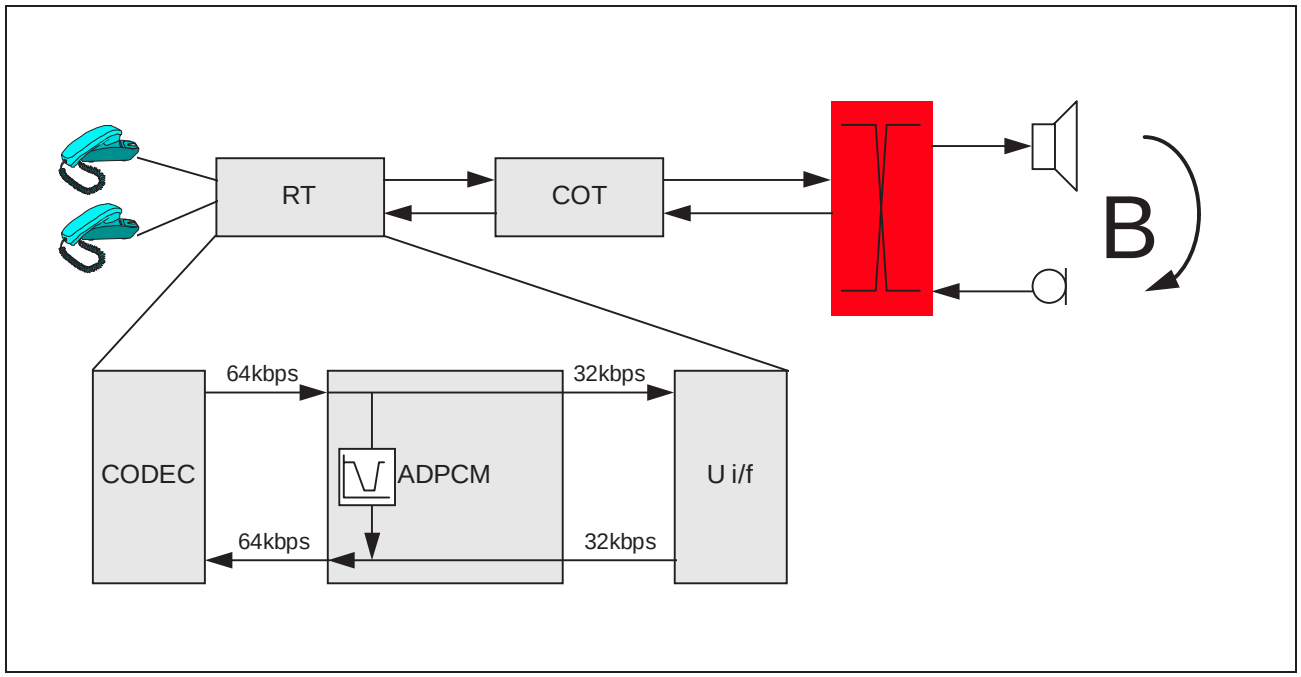



**Figure 17 Echosuppresion on the Uncompressed Side (PCM-4/8 System)**

### Echosuppressor Related Parameters

All parameters used in conjunction with the echsuppressor are located in the DSP RAM. A summery is given in the table below. For a detailed description please refer to section **3.16.6**.

| Parameter | Description |
|---|---|
| ES_ATT | Echosuppressor Attenuation<br>Determines the level of attenuation in the receive path if speech is detected in the transmit path and the estimation of receive power is below the specified limit. |
| ES_DLY | Echosuppressor Delay<br>Specifies the delay time $t_{dly}$ between the disappearance of speech (speechdetector: no speech) and the start of the rise time of the echosuppressor. |
| ES_RISE | Echosuppressor Rise Time<br>Specifies the time $t_r$ in which the attenuation is increased from the programmed value to 0 dB. |
| ES_FALL | Echosuppressor Fall Time<br>Specifies the time $t_f$ in which the attenuation is decreased from 0 dB to the programmed value if speech is detected in the transmit path. |
| ES_PLdly | Echosuppressor Receive Power Level Delay<br>This coefficient is the time constant $t_{PLdly}$ for the power estimator of the receive signal. |
| ES_RxPL | Echosuppressor Receive Power Level<br>This parameter specifies the power level threshold for receive direction. If the signal in the receive path exceeds the programmed value the attenuation added by the echsuppressor will be switched off after $t_{PLdly}$ has elapsed. This guarantees that despite of echosuppression the subscriber on the other end of the line can switch echosuppression off by speaking loud. |

### 2.4.2 Speech Detector

Basically the speech detector makes use of the burst characteristic of speech. That means, every fast change in signal amplitude compared to the average signal level is recognized as speech. This is done by averaging the input signal with a lowpass filter (noise monitor lowpass) and comparing the output of this lowpass with the input signal itself.

As shown in figure **18** the speech detector mechanism is composed of three seperate blocks:

- Power estimator in the receive path
- Speech detection preprocessing in the transmit path
- Noise monitor in the transmit path

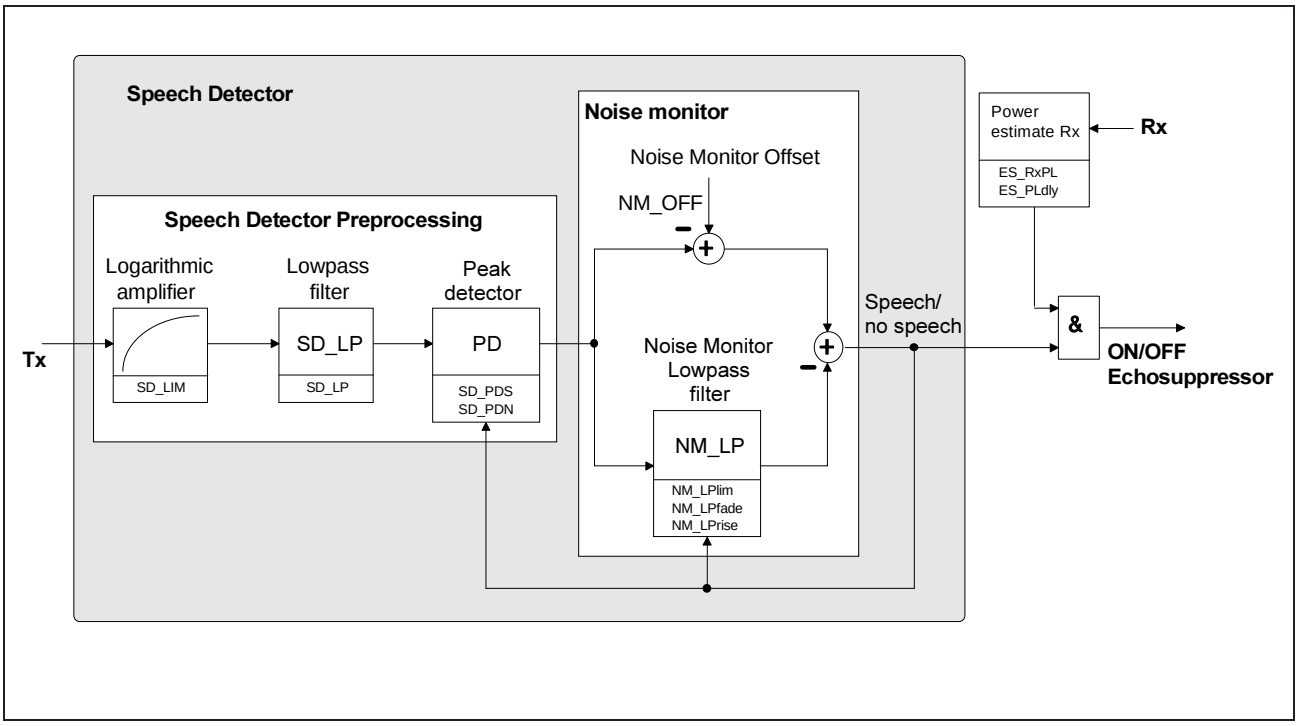



**Figure 18 Speech Detector Mechanism**

The speech detection is performed by components which offer programmable parameters. These components are the logarithmic amplifier, the speech detection lowpass filter, the peak detector and the noise monitor.

They have the following functions:

- Logarithmic Amplifier
  Compression of the signal area of the incoming transmit signal.
- Speech Detection Lowpass Filter
  Spike reduction of the incoming signal.

- Peak Detector
  Improvement of speech detection by offering different time constants for detected and non-detected speech.
- Noise Monitor
  Discriminates between speech and noise. The noise monitor comprises a lowpass filter and an programmable offset. For a detailed description refer to section **2.4.2.1**.

Figure **19** gives an illustration of the speech detector parameters.

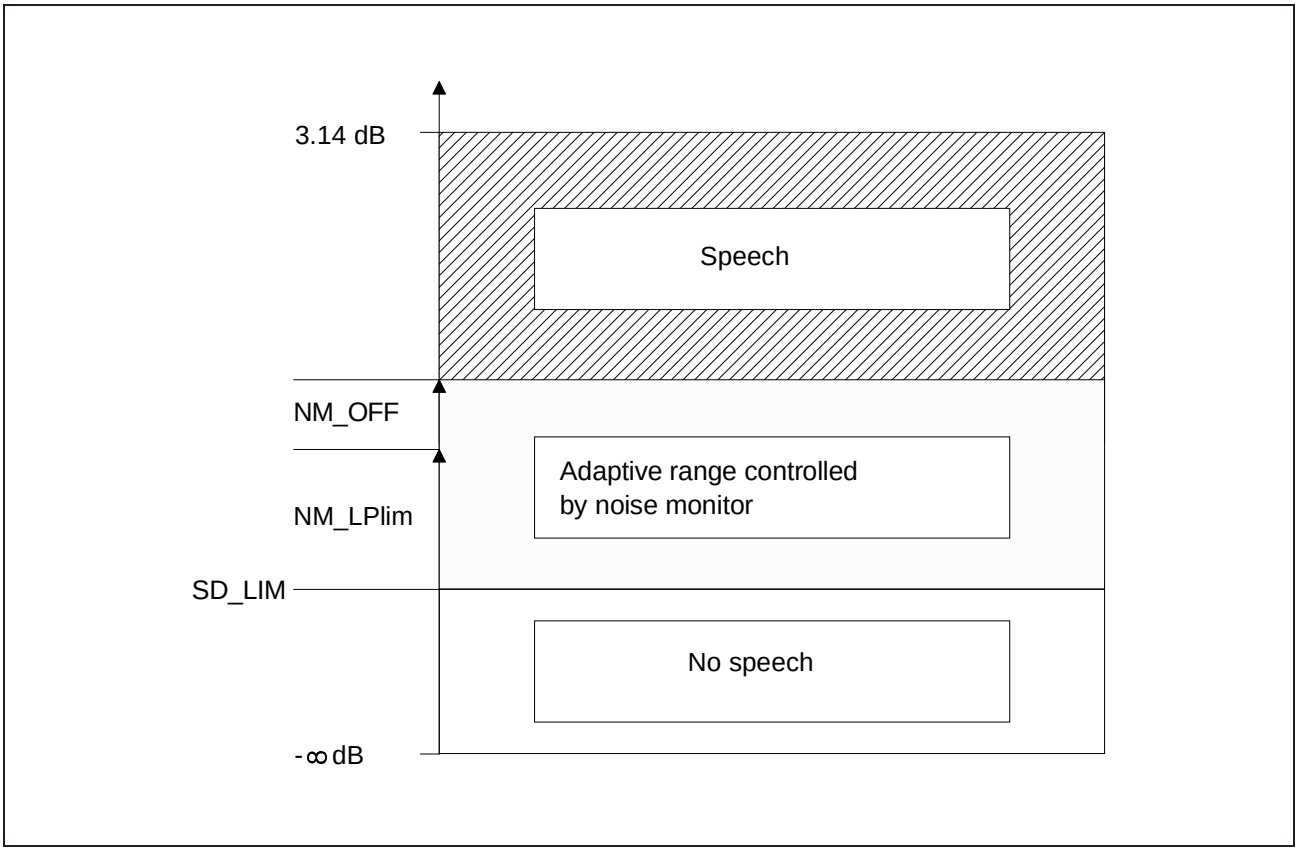



**Figure 19 Speech Detector Parameters**

### 2.4.2.1 Noise Monitor

The tasks of the noise monitor are to differentiate voice signals from background noise, even if it exceeds the voice level, and to recognize voice signals without any delay. Therefore the Noise Monitor consists of the Noise Monitor Lowpass Filter (NM_LP) and the Noise Monitor Offset (NM_OFF) in two separate branches. Basically it works on the burst-characteristic of the speech: voice signals consist of short peaks with high power (bursts). In contrast, background noise can be regarded approximately stationary from its average power.

The noise monitor is able to discriminate between speech and noise. It consists of the noise monitor lowpass filter NM_LP and the offset NM_OFF. Basically it works on the burst-characteristic of the speech: Voice signals consist of short peaks with high power (bursts). Background noise can be regarded approximately stationary from its averaged power. The task of the noise monitor is to recognize voice signals without any delay and to recognize background noise. Since only a difference between the average signal level and the instant signal leads to speech recognition, the influence of noise on the decision is cancelled, even if the noise level exceeds the voice level. See figure **19** for illustration of the programmable parameters of the Noise Monitor.

### Noise Monitor Lowpass Filter

The noise monitor lowpass filter NM_LP provides different time constants for noise (nondetected speech) and speech. It determines the average of the noise reference level. In case of background noise the level at the output of the lowpass filter is approximately the level of the input. Due to the offset NM_OFF the comparator remains in the initial state. In case of speech the difference of the signal level between the offset branch and the lowpass branch at the comparator increases and the comparator output changes its state. At speech bursts the digital signals arriving at the comparator via the offset branch change faster than those via the lowpass branch so that the comparator output changes polarity.

Hence two logical levels are generated

- one for speech and
- one for noise.

A small fade constant NM_LPfade enables a fast discharging of the lowpass after the end of the speech recognition. It is recommended to choose a large rising constant NM_LPrise so that speech itself charges the lowpass very slowly.

Generally it is not recommended to program an infinite rise time NM_LPrise because in that case noise approximation is disabled. The maximum value for the lowpass is limited to the programmable value NM_LPlim to detect continuous tones as speech and activate the echosuppressor.

### Offset

The offset stage NM_OFF represents a level threshold between signal and averaged noise. By this parameter a reference level is programmed to a percentage of full speech signal.

### Noise Monitor Related Parameters

All parameters used in conjunction with the noise monitor are located in the DSP RAM. A summery is given in the table below. For a detailed description please refer to section **3.16.5**.

| Parameter | Description |
|---|---|
| NM_LPlim | Noise Monitor Lowpass Limit<br>This value limits the charging off the lowpass filter. A continous input signal, that has to be detected as speech, has to be above this limit. |
| NM_LPfade | Noise Monitor Lowpass Fade Constant<br>Enables the fast discharge of the noise monitor lowpass after the end of speech recognition. |
| NM_LPrise | Noise Monitor Lowpass Rise Time<br>Determines the time the noise monitor lowpass is charged after speech is recognized. |
| NM_OFF | Noise Monitor Offset<br>Specifies a level threshold between signal and noise. Speech bursts mus be NM_OFF dB above the average signal to be recognized. |

#### 2.4.2.2 Speech Detection Preprocessing

As described in the preceding chapter, the Noise Monitor is able to discriminate between speech and noise. In very short speech pauses e.g. between two words, however, it changes immediately to non-speech, which is equal to noise. Therefore a peak detection is required in front of the Noise Monitor.

### Peak detector

The peak detector bridges the very short speech pauses during a monologue so that the respective time constant has to be long. Furthermore, the speech bursts are stored so that a sure speech detection is guaranteed. But if no speech is recognized the noise monitor lowpass must be charged very fast to the averaged noise level. Additionally the noise edges are to be smoothed. Therefore two time constants are necessary and have to be programmed separately: SD_PDS for speech and SD_PDN for noise (background) signals. Hence ’speech mode’ may be detected faster and kept longer than ’no speech mode’ so that smaller breaks may not cause switching. Also noise is smoothened.

### Speech Detection Lowpass Filter

The peak detector is very sensitive to spikes. The lowpass SD_LP filters the receive signal containing noise in a way that main spikes are eliminated. Due to the programmable time constant SD_LP it is possible to defuse high-energy sibilants and noise edges.

### Logarithmic Amplifier

To compress the speech signals in their amplitudes and to ease the detection of speech, the signals have to be companded logarithmically. Hereby, the speech detector should not be influenced by the system noise which is always present but should discriminate between speech and background noise. The limitation of the logarithmic amplifier can be programmed via the parameter SD_LIM. SD_LIM is related to the maximum PCM level. A signal exceeding the limitation defined by SD_LIM is getting amplified logarithmically, while very smooth system noise below is neglected. It should be the level of the minimum system noise which is always existing.

### Principle of Speech Detection

The diagrams in figure **20** graphically describe the inputs and outputs of the speech detector blocks. The result is not completely identical to the implementation in the Quad ADPCM echosupressor but helps to understand the function of the speech detector.

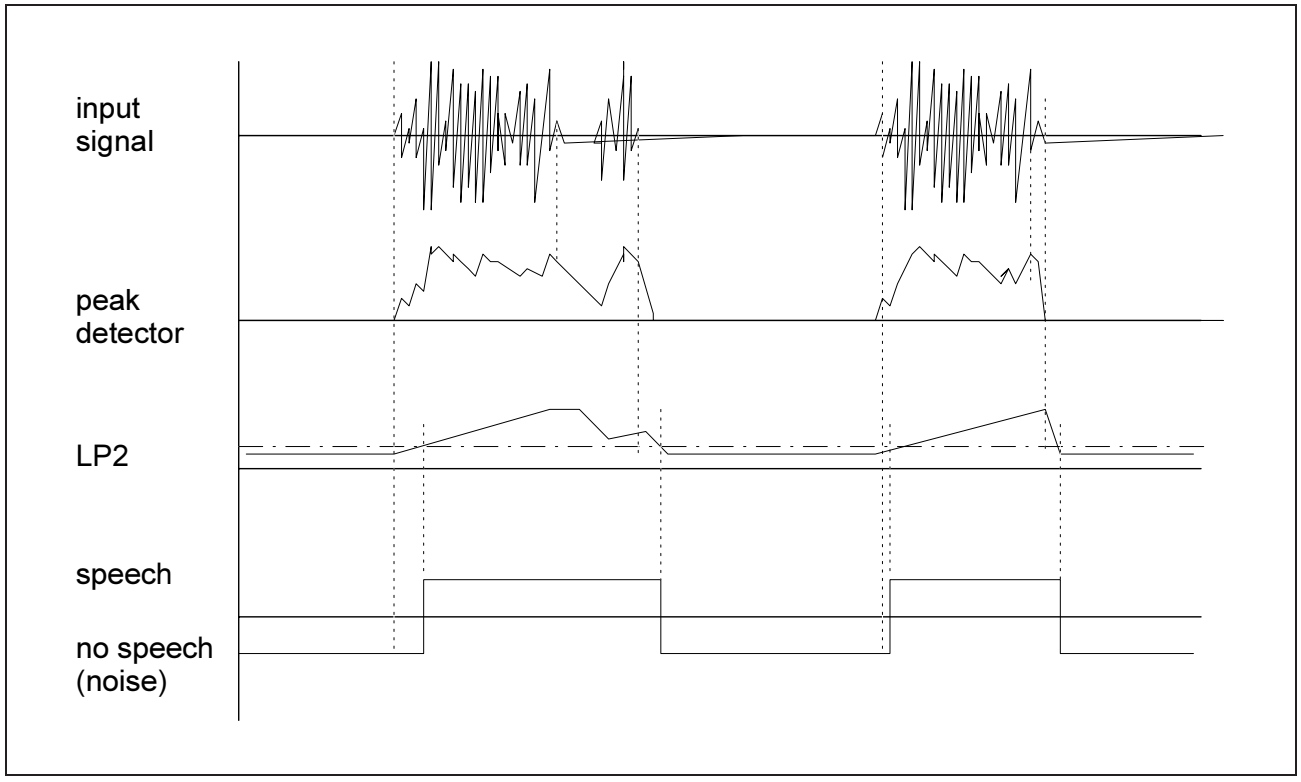



**Figure 20 Speech Detection Principle**

The first diagram shows the analog representation of the input signal, since this signal form is more convenient for the readers understanding of the signal processing. In the ADPCM circuits the signal is delivered to the speech detector digitally. The peak detector output is the envelope of the input signal, where short pauses are bridged. The next diagram explains the function of the noise monitor with the two branches (noise monitor offset input and noise monitor lowpass filter). In the lower diagram the result of the signal processing in the speech detector is shown.

### Speech Detector Related Parameters

All parameters used in conjunction with the speech detection are located in the DSP RAM. A summery is given in the table below. For a detailed description please refer to section **3.16.5**.

| Parameter | Description |
|---|---|
| SD_LIM | Speech Detection Limit<br>Input signals below the level determined by SD_LIM are not processed by the speech detector. Usually SD_LIM is programmed for a threshold that is a few dB above the noise floor of the system. |
| SD_LP | Speech Detection Lowpass<br>This time constant determines how the main spikes are being eliminated. Note that if SD_LP is large the response time of the speechdetector is long. |
| SD_PDS | Speech Detection Peak Detector ’Speech’<br>This coefficient specifies the time constant for speech signals. A large value should be programmed to avoid quick charging during speech. |
| SP_PDN | Speech Detection Peak Detector ’Noise’<br>This coefficient specifies the time constant for noise signals. Small time constants allow quick adaptation to changes of the noise level. |

## 2.5 Fax/Modem Detection

A fax/modem tone detection is implemented in each channel of the Quad ADPCM. Typically a 2.1 kHz tone is used to indicate the remote side that a fax or modem is requesting a connection. To guarantee a reliable detection of this tone fully programmable parameters are provided. These parameters allow an adjustment to individual requirements. As soon as a tone which fullfills all programmed conditions is detected, an interrupt will be generated (provided the interrupt generation was enabled with the FDE register). In the register FDS the source of the interrupt can be read. The Quad ADPCM indicates the successfull detection seperately for compressed and uncompressed side with a ’1’.

Reading the FDS register will automatically reset the interrupt line ($\overline{INT}$ = high). Every transition of bits in the FDS register generates an interrupt. A ’1’ to ’0’ transition will however occure only after the device detected that no information is sent any more (power monitoring). The stopping of the 2.1 kHz tone will not cause a ’1’ to ’0’ transition. Optionally each channel bit in the FDS register may individually be reset to ’0’. This reset is performed by programming the corresponding FDE:EMi bit to ’0’ (resets the two FDS detection bits of channel i for of uncompressed and compressed side to ’0’). After reprogramming the FDE:EMi bit to ’1’ the next interrupt will be generated as soon as the fax/modem tone criterias are fullfilled again.

*Note: No default DSP RAM values are available after a reset. All parameters need to be programmed after reset.*

The operation of the fax/modem detection is illustrated in figure **21**. For reliable tone detection a combination of frequency criteria and time criteria must be met.

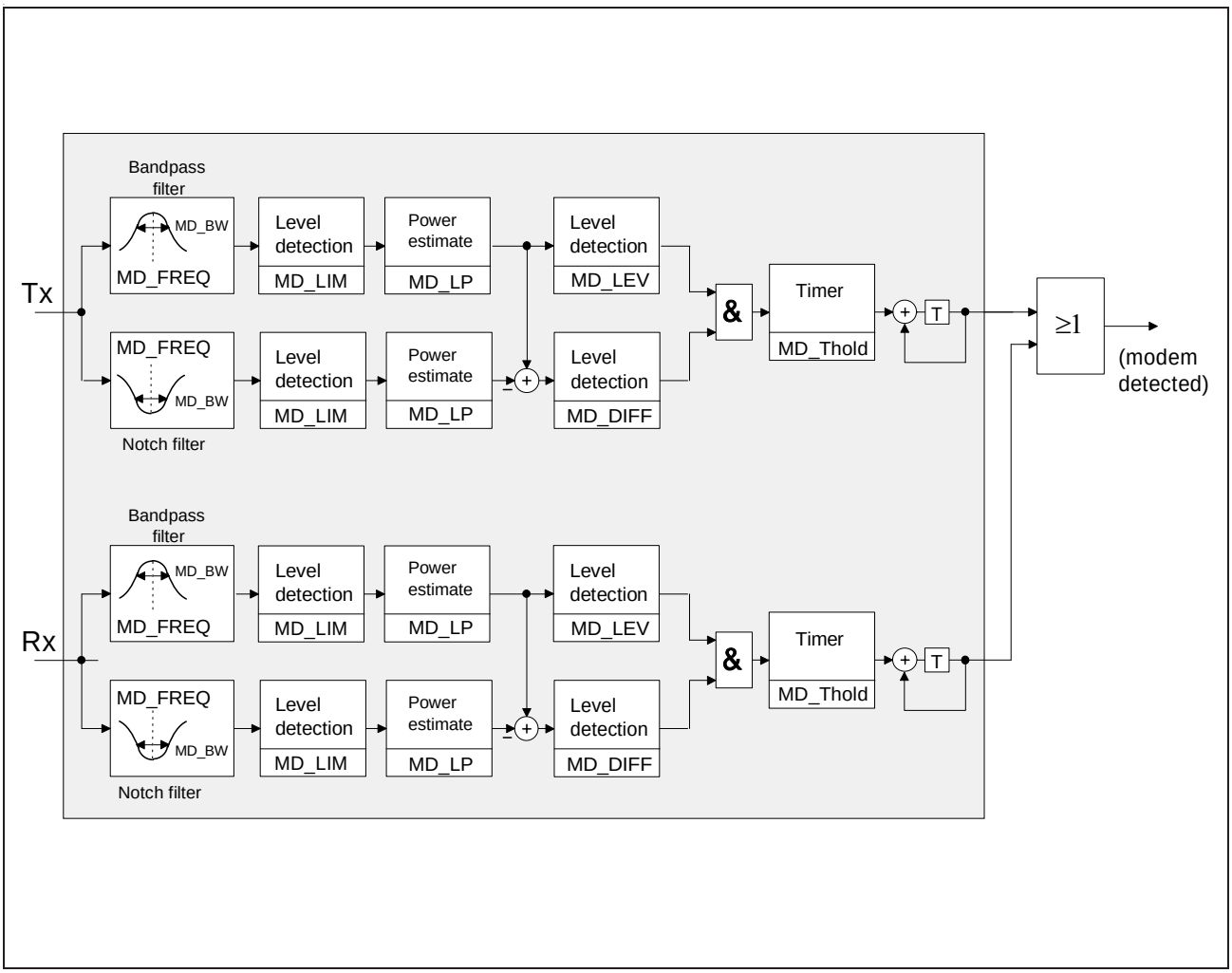



**Figure 21 Fax/Modem Tone Detection**

The upper branches of the Rx- and Tx-path contain the bandpass filter and can detect modem tones. The lower branches contain the notch filter to filter out the modem signal so that the output signals of these branches represent the power in the remaining band.

For speech signals the output signal of the lower branch will be large compared to the output of the upper path and vice versa for modem signals.

The center frequency and bandwidth of the modem filters can be programmed using parameters MD_FREQ and MD_BW (bandpass and notch filter). The filter outputs are averaged using a lowpass filter with parameter MD_LP so that the power estimate of the signals are obtained.

A minimum modem level of -40 dB which has to be detected is specified by CCITT standard G.164. A respective limit value can be programmed using parameter MD_LIM.

The difference value MD_DIFF is implemented for modem signal detection in the transmit path. If the difference of the signal energy in the modem frequency band and out of the modem frequency band is larger than MD_DIFF a modem signal can be detected.

For large values of MD_DIFF erraneous fax/modem detection for speech input signals is avoided. On the other hand modem signals with small frequency deviations or additional noise are not detected anymore. Smaller values of MD_DIFF allow fax/modem detection in a noisy environment. Protection against erraneous fax/modem detection for speech input signals is however reduced.

The timer (MD_Thold)has been implemented to eliminate the influence of transients. Adjustment should be such that modem tones of minimum duration 500 ms duration can be detected as required by CCITT specification G.164.

### Fax/Modem Detection Related Parameters

All parameters used in conjunction with the fax/modem detection are located in the DSP RAM. A summery is given in the table below. For a detailed description please refer to section **3.16.7**.

| Parameter | Description |
|---|---|
| MD_FREQ | Fax/Modem Detection Center Frequency<br>Should be adjusted to the frequency of the modem signal to be detected (2.1 kHz tones). |
| MD_BW | Fax/Modem Detection Bandwidth<br>Determines the bandwidth of the modem filter. |
| MD_LP | Fax/Modem Detection Lowpass<br>Specifies the time constant for the power estimator. |
| MD_Tbreak | Fax/Modem Detection Break Time<br>Tone breaks of less than the specified time are ignored. |
| MD_Thold | Fax/Modem Detection Hold Time<br>Specifies the time the detection conditions have to be valid for fax/modem detection. |
| MD_DIFF | Fax/Modem Detection Difference<br>This parameter specifies the difference the outputs of the bandpass and the notch filter have to exceed. If the difference of the signal energy in the modem frequency band and out of the modem frequency band is larger than MD_DIFF a modem signal can be detected. |
| MD_LEV | Fax/Modem Detection Level<br>Determines the threshold below which noise or signals are ignored. |
| MD_LIM | Fax/Modem Detection Limit<br>The level programmed in MD_LIM is compared with the output of the modem filter. If the level of the modem signal is above MD_LIM modem detection can be activated. |

| | |
|---|---|
| MD_LEVE | The parameter specifies the level for the end of the fax/modem detection. |
| MD_TIME | The parameter specifies the timing conditions for the end of the fax/modem detection. |

## 2.6 Artificial Echo Loss

An Artificial Echo Loss (AEL) can be added to the receive path. The AEL gain can be programmed from -45 dB to 0 dB. The direction of the AEL is opposite to the direction of the echo suppression as set in the ESE register. The AEL can be enabled for each channel independently by setting the ADF register bits EA3 ... EA0 to ’1’.

### Artificial Echo Loss Related Parameters

The parameter used in conjunction with the AEL is located in the DSP RAM. A summery is given in the table below. For a detailed description please refer to section **3.16.4**

| Parameter | Description |
|---|---|
| AEL_GAIN | Artificial Echo Loss Gain<br>Determines the level of the AEL added to the receive path. |

## 2.7 Congestion Tone Generator

A programmable tone with an amplitude between -45 dBm and 0 dBm and a frequency between 0 Hz and 1 kHz can be put to the uncompressed data output instead of the PCM data. The ADPCM data is not evaluated if the congestion tone generator is enabled.

The tone can be used to create a 'line occupied' signal already in the terminal side of a wireless local loop system in the case the air interface is occupied. The tone can be enabled for each channel independently by setting the ADF register bits EC3 ... EC0 to '1'. It's modulation is done by enabling and disabling it at the appropriate rate. DSP 2 has to be enabled for the tone generation.

### Congestion Tone Generator Related Parameters

All parameters used in conjunction with the congestion tone generator are located in the DSP RAM. A summery is given in the table below. For a detailed description please refer to section **3.16.2**.

| Parameter | Description |
|---|---|
| CT_FREQ | Congestion Tone Frequency |
| CT_LEV | Determines the level of the Congestion Tone |
| CT_GAIN | Specifies the frequency gain |

## 2.8 Frame Strobe Outputs

The application in pair gain systems together with standard codec filters is supported with one Frame Strobe output per channel at the pins FSi (i = 0 to 3 being the channel number).

There are two different timings available, referred to as short frame and long frame, respectively. The selection is done with the FST bit in the configuration register CR. CR:FST set to '1' selects short frame timing. CR:FST set to '0' selects long frame timing.

If CR:FSEN is set to '0', all four FSi outputs are tied to $V_{SS}$. Figures **22** and **23** give the timings for short framing. Figure **24** and **25** illustrate the long frame timings.

In short frame timings the first bit starts with the falling edge of FSi. The frame strobe signal is high during one DCL period in single clock mode (ADF2:DCLK = ’1’) as well as in double clock mode (ADF2:DCLK = ’0’).

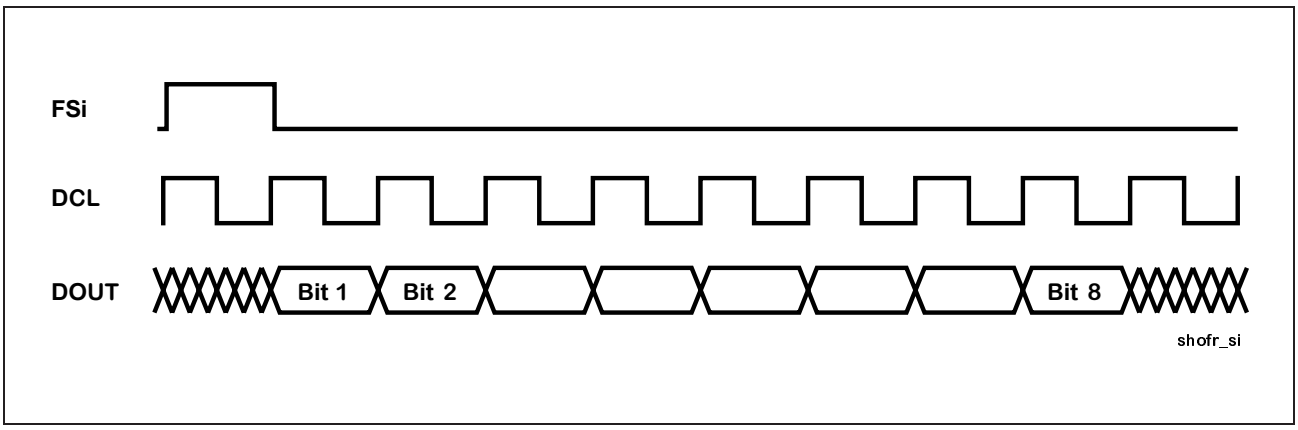



**Figure 22 Frame Strobe Output: Short Frame Timing, Single Clock Mode**

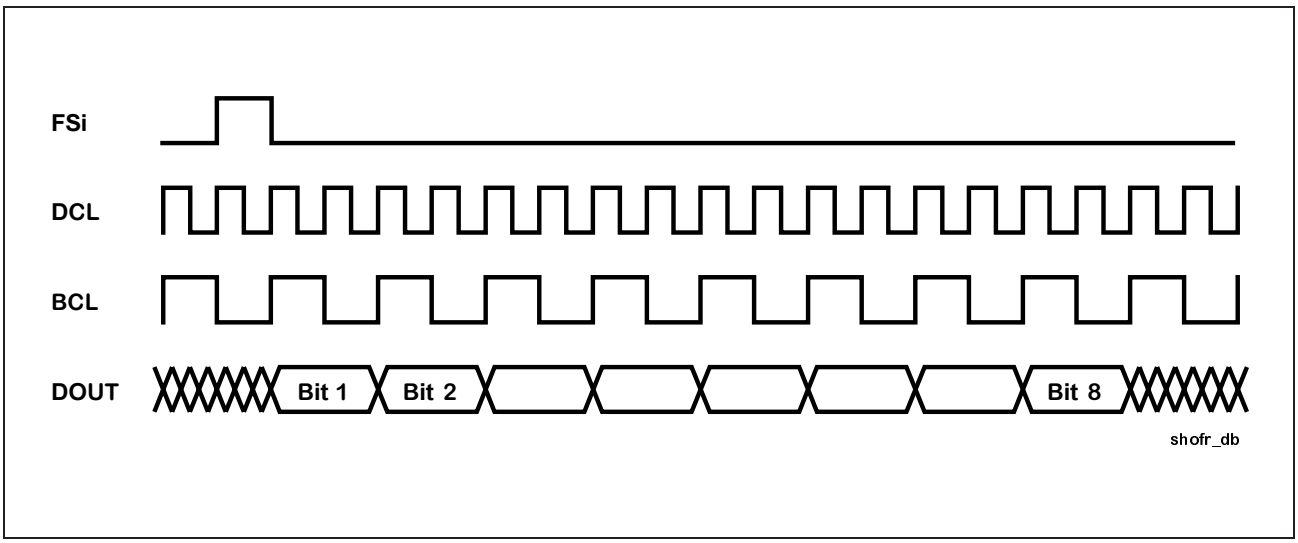



**Figure 23 Frame Strobe Output: Short Frame Timing, Double Clock Mode**

In double clock mode, the BCL signal can be used by the recieving device to determine when the PCM data is shifted in.

At long frame timing the time slots are nominally coincident with the rising edge of FSi. The frame strobe signal is high during all 8 (single clock mode), 16 (double clock mode) respectively, DCL periods marking one complete time slot.

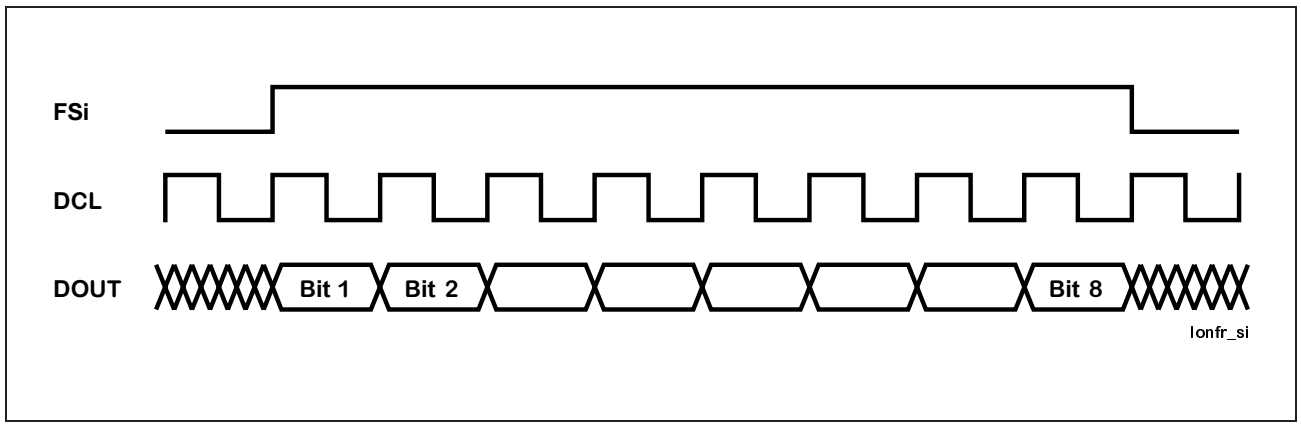



**Figure 24 Frame Strobe Output: Long Frame Timing, Single Clock Mode**

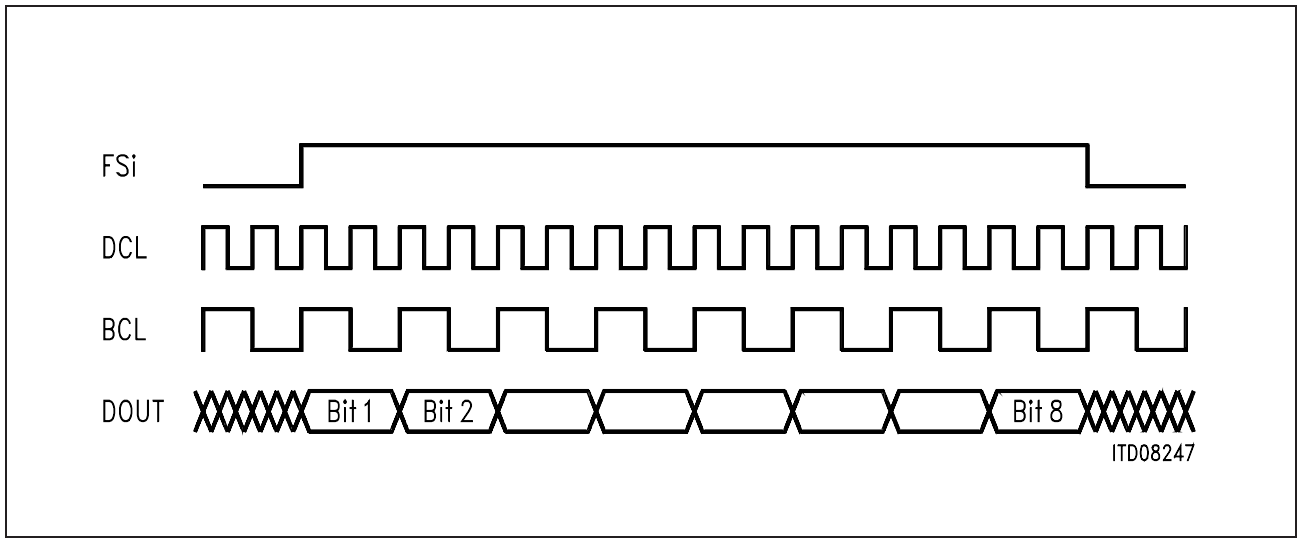



**Figure 25 Frame Strobe Output: Long Frame Timing, Double Clock Mode**

In double clock mode, the BCL signal can be used by the recieving device to determine when the PCM data is shifted in.

## 2.9 Serial Microcontroller Interface

The serial microcontroller interface consists of four lines: $\overline{CS}$, CCLK, CDIN and CDOUT. $\overline{CS}$ is used to start a serial access to the registers. Following a falling edge of $\overline{CS}$, the first eight bits received on CDIN specify the command. The following data byte is stored in the selected register with the rising edge on $\overline{CS}$. The first received bit specifies a read (bit = ’0’) command or a write command (bit = ’1’). The following five bits give the register address (MSB first).

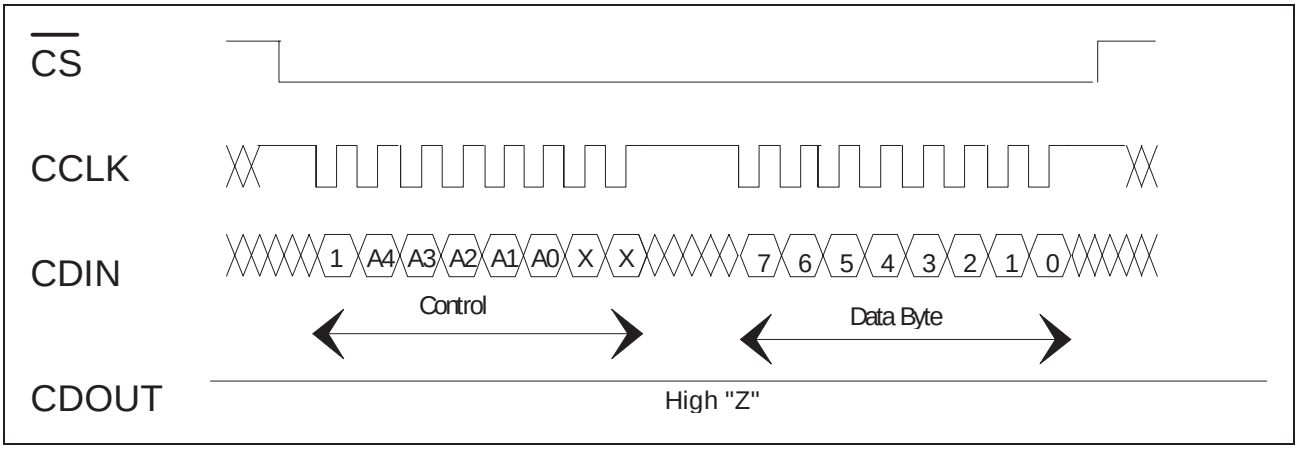



**Figure 26 Microcontroller Interface Timing: Write Access**

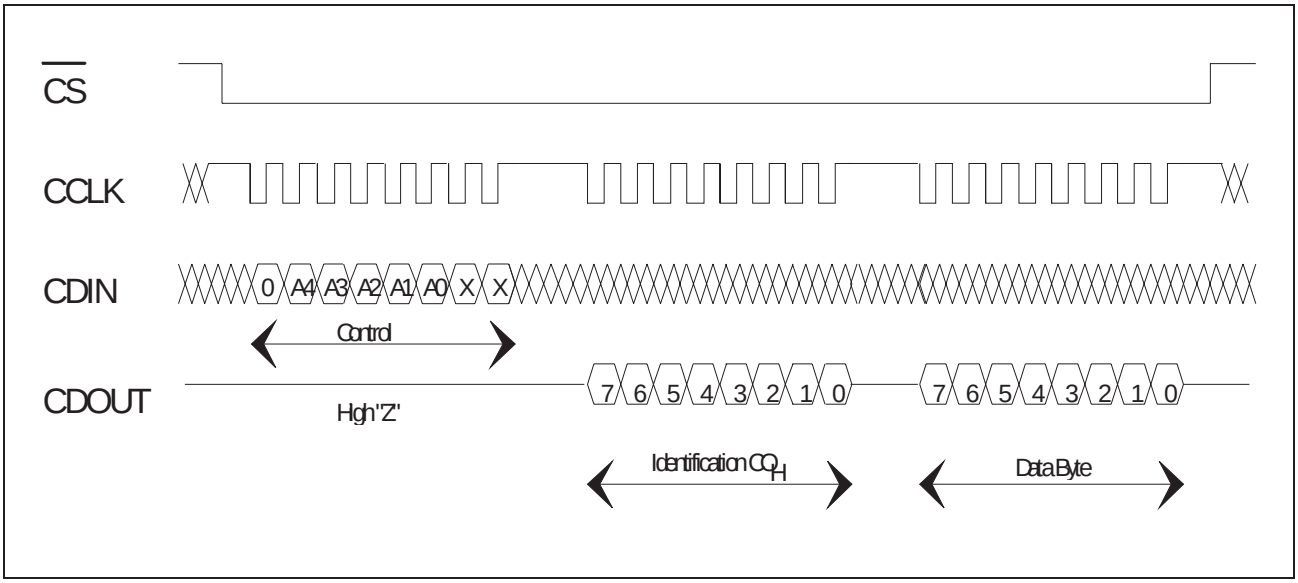



**Figure 27 Microcontroller Interface Timing: Read Access**

In a read access an ID-Byte ($CO_H$) is issued before the data byte as shown in figure **27**.

The maximum data clock frequency to be applied at pin CCLK is 7.68 MHz. CCLK may pause between control and read/write byte(s). These breaks may be arbitrarly long or missing at all.

Data bits at CDIN are latched by the device with the rising edge of CCLK. The bits at CDOUT are put to the line with the falling edge of CCLK, they may therfore be latched by the µC with the rising edge.

Indirect Access to the DSP RAM is provided via the COM register, the DST register, the DATA registers and the ADR register. The DATA registers are used to either read data from or write data to the DSP RAM. The read access of the other registers is only used to control the register contents.

Data put into the registers at an arbitrary time is valid with the next rising edge of the frame clock at FSC. If the DSYNC pin is input, data is valid at the next rising edge of the frame at FSC after the next falling edge of the clock at DSYNC.

## 2.10 Boundary Scan Test Controller

The Quad ADPCM provides a boundary scan support for a cost effective board testing. It consists of:

- –Complete boundary scan for 22 signals (pins) according to IEEE Std. 1149.1 specification
- –Test access port controller (TAP)
- –Four dedicated pins (TCK, TMS, TDI, TDO)
- –One 32-bit IDCODE register

All pins except the power supply pins, the ’not connected’ pin and pins BCL, MCL, TDI, TDO, TCK, TMS, XTAL1 and XTAL2 are included in the boundary scan.

When the TAP controller is in the appropriate mode data is shifted into or out of the boundary scan via the pins TDI/TDO using clock at pin TCK. The clock rate at pin TCK may be up to 10 MHz.

Depending on the pin functionality one, two or three boundary scan cells are provided.

*Note: There are several pins, which for chip test are used as I/O pins. Please refer to section 1.4 whether these pins are inputs or outputs. However, they are included to the boundary scan as I/O pins with three scan cells.*

| Pin Type | Number of Boundary Scan Cells | Usage |
|---|---|---|
| Input | 1 | input |
| Output | 2 | output, enable |
| I/O | 3 | input, output, enable |

The pins are included in the following sequence in the boundary scan:

| Boundary Scan Number TDI ––> | Pin Number | Pin Name | Type | Number of Scan Cells |
|---|---|---|---|---|
| 1 | 37 | DSYNC | I/O | 3 |
| 2 | 38 | FS2 | O | 2 |
| 3 | 39 | FS1 | O | 2 |
| 4 | 40 | FSC | I | 1 |
| 5 | 41 | DCL | I | 1 |
| 6 | 42 | DINU | I | 1 |
| 7 | 43 | FS0 | O | 2 |
| 8 | 44 | FS3 | O | 2 |
| 9 | 1 | ALAW | I | 1 |
| 10 | 2 | $\overline{\text{INT}}$ | O | 2 |
| 11 | 3 | CDOUT | O | 2 |
| 12 | 4 | CDIN | I | 1 |
| 13 | 5 | $\overline{\text{CS}}$ | I | 1 |
| 14 | 8 | CCLK | I | 1 |
| 15 | 9 | DOU | O | 2 |
| 16 | 10 | DOC | O | 2 |
| 17 | 11 | DINC | I | 1 |
| 18 | 12 | PD2 | I | 1 |
| 19 | 13 | PD1 | I | 1 |
| 20 | 14 | $\overline{\text{TCC}}$ | O | 2 |
| 21 | 15 | $\overline{\text{TCU}}$ | O | 2 |
| 22 | 16 | $\overline{\text{RES}}$ | I | 1 |

### 2.10.1 TAP Controller

The *Test Access Port* (TAP) controller implements the state machine defined in the JTAG standard IEEE Std. 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change.

Following the standard definition 7 instructions are executable.

**TAP controller instructions:**

| Code | Instruction | Function |
|---|---|---|
| 000 | EXTEST | External testing |
| 001 | INTEST | Internal testing |
| 010 | SAMPLE/PRELOAD | Snap-shot testing |
| 011 | IDCODE | Reading ID code |
| 100 | CLAMP | Reading outputs |
| 101 | HIGHZQ | Z-State of all boundary scan output pins |
| 11X | BYPASS | Bypass operation |

**EXTEST** is used to examine the board interconnections.

When the TAP controller is in the state "update DR", all output pins are updated with the falling edge of TCK. When it has entered state "capture DR" the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

**INTEST** supports internal chip testing.

When the TAP controller is in the state "update DR", all inputs are updated internally with the falling edge of TCK. When it has entered state "capture DR" the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

Note: 001 (INTEST) is the default value of the instruction register.

**SAMPLE/PRELOAD** provides a snap-shot of the pin level during normal operation or is used to preload (TDI) / shift out (TDO) the boundary scan with a test vector. Both activities are transparent to the system functionality.

**BYPASS**, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

**HIGHZQ** sets all pins included to the boundary scan path into a high impedance state. In this state, an in-circuit test system may drive signals onto these pins.

**CLAMP** allows the state of the signals included in the boundary scan driven from the Quad ADPCM to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. These signals will not change while CLAMP is selected.

**IDCODE** serially reads out the 32-bit identification register via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

| Version | Device Code | Manufacturer Code | | Output |
|---|---|---|---|---|
| 0001 | 0000 0000 0011 0011 | 0000 1000 001 | 1 | --> TDO |

*Note: In the state 'test logic reset' the code '011' is loaded into the instruction code register.*

## 3 Register and DSP RAM Location Description

Operational modes are set per register programming. The default state of all registers after reset is such that operation in a PCM-4 system is possible without access of the microcontroller to the Quad ADPCM. A-law or µ-law operation can then be set by pin strapping.

All registers except the FDS and the DST register are of read / write type. These can be used to control the register contents and to read DSP RAM data of the DATAL and DATAH registers. The address map and a register summary are given in the following table. Registers with addresses $12_H$ to $1F_H$ are not accessible to the user. They are used for test purposes only.

*Note: Defaults of registers with two default values given depend on the setting of the ALAW pin.*
*ALAW pin low: left reset value is valid.*
*ALAW pin high: right rest value is valid.*

## Table 1 Register Summary

| Address (hex) | Register Name | Reset value (hex) | Description | Refer to page |
|---|---|---|---|---|
| 00 | UT0 | 26 or 27 | Uncompressed Timeslot of channel 0[1)] | 50 |
| 01 | UT1 | 2E or 2F | Uncompressed Timeslot of channel 1[1)] | 50 |
| 02 | UT2 | 46 or 47 | Uncompressed Timeslot of channel 2[1)] | 50 |
| 03 | UT3 | 4E or 4F | Uncompressed Timeslot of channel 3[1)] | 50 |
| 04 | MSB | 00 | MSB of PCM time slots[1)] | 53 |
| 05 | CRR | 00 | Compression Rate Register[1)] | 49 |
| 06 | DPP | 00 | Decoding PCM Position[1)] | 52 |
| 07 | ADF | 00 | Additional Features Register | 54 |
| 08 | ADF2 | 00 | Additional Features Register 2[2)] | 54 |
| 09 | CR | 00 | Configuration Register[2)] | 48 |
| 0A | ESE | 00 | Echosuppressor enable | 53 |
| 0B | FDE | FF | FAX Detection Enable Register | 55 |
| 0C | FDS | 00 | FAX Detection Status Register[3)] | 56 |
| 0D | DST | 00 | DSP Status Register[3)] | 56 |
| 0E | COM | 00 | Command Register | 57 |
| 0F | ADR | 00 | Address of DSP RAM block | 58 |
| 10 | DATAH | 00 | DSP RAM Data Register, high byte | 58 |
| 11 | DATAL | 00 | DSP RAM Data Register, low byte | 58 |

1) A change in this register becomes effective only after 2 frames
2) A change in this register becomes effective in the next frame
3) No write access by the user

## 3.1 Configuration Register (CR)

The Configuration Register CR selects the general setting valid for all four channels.

| FSEN | FST | MCLK1 | MCLK0 | OSB | DS1 | DS0 | RES |
|---|---|---|---|---|---|---|---|

**FSEN** Frame Strobe Enable
1 ... enable frame strobes at pins FS3..FS0
0 ... set pins FS3 to FS0 to $V_{SS}$

**FST** Frame Synchronization Type
0 ... selects long frame
1 ... selects short frame

**MCLK1, MCLK0** Master Clock selection
The frequency at DCL must be disclosed to the device for proper operation as given in the table below:

| MCLK1 | MCLK0 | Clock at DCL pin |
|---|---|---|
| 0 | 0 | 1536 kHz |
| 0 | 1 | 2048 kHz |
| 1 | 0 | 4096 kHz |
| 1 | 1 | reserved |

**OSB** Oscillator Bypass
1 ... bypasses the internal oscillator if no crystal is connected to XTAL1 and XTAL2
0 ... when a crystal is connected to XTAL1 and XTAL2

**DS1, DS0** DECT Sync Mode
The Quad ADPCM provides a DECT Synchronization clock of either 800 ms period or 2.4 s period at the DSYNC pin. The clock can also be fed into the Quad ADPCM if the DSYNC pin is programmed as input. The settings are programmed as given in the table below:

| DS1 | DS0 | Clock period at DSYNC pin |
|---|---|---|
| 0 | 0 | DSYNC pin tied to $V_{SS}$ |
| 0 | 1 | input |
| 1 | 0 | 800 ms |
| 1 | 1 | 2.4 s |

If DSYNC is output, it generates a signal with a low time of 62.5 µs. The falling edge of this signal is at the rising edge of FSC.

If DSYNC is input, the contents of the registers with the addresses 0 to $6_H$, $8_H$ and $9_H$ are stored with the first rising edge at the FSC pin after the falling edge at the DSYNC pin. This allows synchronous adaption of the compression rate and disabling/ enabling of outputs on all devices in a system. If DSYNC is input, ADF2:SBE is 'don't care'. The signal starts at the frame n+3 if enabled during frame n.

**RES** Reset

1 ... resets the device to it's default state.
The effect is the same as applying a 'low' to the $\overline{RES}$ pin for 2 DSP clock cycles. The Reset bit is set to low after 2 DSP cycles.

## 3.2 Compression Rate Register (CRR)

The Compression Rate Register CRR selects the compression rate for each channel separately.

| CR31 | CR30 | CR21 | CR20 | CR11 | CR10 | CR01 | CR00 |
|---|---|---|---|---|---|---|---|

**CR31, CR30** Compression Rate for channel 3

**CR21, CR20** Compression Rate for channel 2

**CR11, CR10** Compression Rate for channel 1

**CR01, CR00** Compression Rate for channel 0

The compression rates for each channel are set according to the table below:

| CRi1 | CRi0 | compression rate of channel i |
|---|---|---|
| 0 | 0 | 32 kb/s |
| 0 | 1 | 40 kb/s |
| 1 | 0 | 16 kb/s |
| 1 | 1 | 24 kb/s |

If the UTi:M1 bit is set to one (bypass-mode, see section **3.3**), the number of bypassed most significant bits is set by the CRR register as given in the table below. The MSBs of the un-compressed data are passed to the compressed location.

| CRi1 | CRi0 | number of bypassed bits, channel i, UTi:M0 = 0 | number of bypassed bits, channel i, UTi:M0 = 1 |
|---|---|---|---|
| 0 | 0 | 1 | 4 |
| 0 | 1 | 2 | 5 |
| 1 | 0 | 3 | 6 |
| 1 | 1 | 8 µ-Law | 8 a-law |

CRi1 and CRi0 set to 1 internally encodes and decodes the data. Hence, all features like echosuppression, AEL etc. are available.

*Note:Due to the conversion law given by the µ-Law, only at a-law operation an exact bypass operation is possible.*

### 3.3 Uncompressed Time slot Registers (UT0 ... UT3)

The Uncompressed Time slot registers UTi select the operation mode of channel i (i = 0, 1, 2, 3) together with the PCM time slot where the uncompressed data is taken from pin DINU and put to pin DOU, respectively.

| TS4 | TS3 | TS2 | TS1 | TS0 | M2 | M1 | M0 |
|---|---|---|---|---|---|---|---|

**TS4 ... TS0** Time slot select

The time slot on the PCM interface is selected where the **uncompressed data** is taken from and written to, respectively. As the maximum data rate is 4.096 MHz, there are in single clock mode a maximum of 64 time slots. The slots are set as given in the table below. The setting of the UTi registers must take into account the available number of time slots. The MSB is a part of the MSB register: MSB:UTMi for channel i.

| MSB: UTMi | TS4 | TS3 | TS2 | TS1 | TS0 | slot number |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | | | ... |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

**M2 ... M0** Compression Mode Selection

A-law, µ-law, 16 bit linear operation or complete disable of the corresponding channel is selected as given below. In the 16 bit linear case the uncompressed data occupies two time slots. Data is taken from and written to the slot as defined by TS4 to TS0 and the next one. The synchronous coding adjustment (SCA, see figure **10**) can be disabled.

| M2 | M1 | M0 | description | mode |
|---|---|---|---|---|
| 0 | 0 | 0 | channel disabled [1)] | Powerdown |
| 0 | 0 | 1 | Encoder 16-bit lin. to ADPCM<br>Decoder ADPCM to 16-bit lin.<br>SCA disabled | Linear |
| 0 | 1 | 0 | bypass 1, 2, 3 or 8 bit as set by CRR register [1)] | Bypass, Data-over-voice |
| 0 | 1 | 1 | bypass 4, 5, 6 or 8 bit as set by CRR register [1) 2)] | Bypass, Data-over-voice |
| 1 | 0 | 0 | Encoder µ-law to ADPCM<br>Decoder ADPCM to µ-law<br>SCA disabled | PCM without SCA |
| 1 | 0 | 1 | Encoder A-law to ADPCM<br>Decoder ADPCM to A-law;<br>SCA disabled | PCM without SCA |
| 1 | 1 | 0 | Encoder µ-law to ADPCM<br>Decoder ADPCM to µ-law<br>SCA enabled | PCM |
| 1 | 1 | 1 | Encoder A-law to ADPCM<br>Decoder ADPCM to A-law;<br>SCA enabled | PCM |

1) These modes set the ADPCM algorithm in Powerdown and Reset as specified by CCITT Rec. G.726

2) Bypass of 8 bits causes encoding and decoding providing all features as AEL, echosuppression etc. Real bypass only with less than 8 bit.

The default after reset is as given in the table below. The default time slots are fixed while the default compression law depends on the state at the ALAW pin.

| register | ALAW-pin | default after reset |
|---|---|---|
| UT0 | 0 | 26 |
| UT0 | 1 | 27 |
| UT1 | 0 | 2E |
| UT1 | 1 | 2F |
| UT2 | 0 | 46 |
| UT2 | 1 | 47 |
| UT3 | 0 | 4E |
| UT3 | 1 | 4F |

### 3.4 Decoder PCM Position Register (DPP)

The Decoder PCM-position register DPP selects the bit in the frame where the **compressed data** is taken from pin DINC and put to pin DOC, respectively. In double clock mode, each frame consists of not more than 256 bits, depending on the DCL clock rate. The binary content of the DPP register gives the bit number in the frame, where the compressed data begins. In bit clock mode there are up to 512 bits in each frame. In that case, the assignment of the compressed data is restricted to the first 256 bits in the frame.

The compressed data is tied together. The DPP register give the location of the MSB of the compressed data of channel 0. The MSB of the compressed data of channel 1 directly follows the LSB of channel 0. The MSB of channel 2 follows the LSB of channel 1 etc.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MSB | | | | | | | LSB |

*Note: If a lower frequency than 4.096 MHz is applied at the DCL pin, the setting of the DPP register must take into account the available number of bits.*

*Note: The last 15 bits of a frame must not be used as start position for the compressed data.*

### 3.5 MSB of PCM Time Slots Register (MSB)

The MSB register contains the most significant bits of the time slots assignment for **uncompressed data**. This register is only necessary when the single bit clock mode is enabled (ADF2:DCLK = ’1’). In this case, there are 64 time slots available. If ADF2:DCLK is set to ’0’, there are only 32 time slots available and the MSB:UTMi bits are not taken into account.

It also contains the disable bits DOi of the compressed and uncompressed output. As long as the DOi bit is ’1’, the corresponding output time slot on pins DOU and DOC is in ’Z’-state allowing the PSB 7110 ISAR to pass data onto this time slot.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| UTM3 | UTM2 | UTM1 | UTM0 | DO3 | DO2 | DO1 | DO0 |

**UTM3 ... 0** Uncompressed Time slot most significant bit (MSB) of corresponding channel 3, 2, 1 or 0

**DO3 ... 0**
0 ... Enable Output of corresponding channel 3, 2, 1 or 0
1 ... Disable Output of corresponding channel 3, 2, 1 or 0 resets ADPCM algorithm

### 3.6 Echo Suppressor Enable Register (ESE)

The ESE register contains the enable bits of the four echo suppressor algorithms and the direction of the suppressed echo. The other echo suppressor parameters reside in the DSP RAM. They are indirectly programmed via the COM, ADR and DATA registers.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| E3 | E2 | E1 | E0 | D3 | D2 | D1 | D0 |

**E3 ... 0**
0 ... Disable Echosuppressor of corresponding channel 3, 2, 1 or 0
1 ... Enable Echosuppressor of corresponding channel 3, 2, 1 or 0

**D3 ... 0** Direction of suppressed echo of corresponding channel 3, 2, 1 or0
0 ... the echo from transmit path to receive path of the **un**compressed side is suppressed
1 ... the echo from transmit path to receive path of the compressed side is suppressed.

*Note:The direction of the AEL is the opposite direction of the echosuppression.*

### 3.7 Additional Feature Register (ADF)

The Additional Features register contains the enable bits of the AEL and the congestion tone generator.

| EA3 | EA2 | EA1 | EA0 | EC3 | EC2 | EC1 | EC0 |
|---|---|---|---|---|---|---|---|

**EA3 ... 0** 0 ... Disables Artificial echo loss AEL of corresponding channel 3, 2, 1 or 0
1 ... Enable Artificial echo loss AEL of corresponding channel 3, 2, 1 or 0

**EC3 ... 0** 0 ... Disable Congestion tone of corresponding channel 3, 2, 1 or 0
1 ... Enable Congestion tone of corresponding channel 3, 2, 1 or 0

### 3.8 Additional Feature Register 2 (ADF2)

The Additional Features register 2 contains the bit to select double or single clock mode for the DCL clock and the bit to select the start time of the encoder algorithm.

*Note: The ENS bit should not be changed during operation to avoid cracking.*

| DCLK | ENS | SBE | MCE | | | | |
|---|---|---|---|---|---|---|---|

**DCLK** Data Clock Mode
The clock rate at DCL is either equal to the data rate (single clock) or twice the data rate (double clock).
0 ... selects double clock at DCL
1 ... selects single clock at DCL

**ENS** ENcoder Start
The time when the encoder algorithm starts is set according to the tables in section **2.3**.

*Note:If ADF2:ENS is set to '0', 16 bit are issued at DOC.*
*If ADF2:ENS is set to '1', only 8 bit are issued at DOC.*

**SBE** Synchronous Buffer enable

1 ... If DSYNC is output (CR:DS1 = 1), the contents of the registers with the addresses 0 to $6_H$, $8_H$ and $9_H$ are stored with the first rising edge at the FSC pin after the falling edge at the DSYNC pin.

0 ... If DSYNC is output (CR:DS1 =1), the contents of the registers with the addresses 0 to $6_H$, $8_H$ and $9_H$ are stored with the next rising edge at the FSC pin.

If DSYNC is input, SBE is don't care. The contents of the registers with the addresses 0 to $6_H$, $8_H$ and $9_H$ are stored with the first rising edge at the FSC pin after the falling edge at the DSYNC pin.

**MCE** Master Clock Enable

1 ... Enables the output of the 20.48 MHz crystal clock on the pin MCL. This clock can be used for clocking other Quad ADPCMs.

0 ... Disable master clock output on pin MCL.

### 3.9 Fax/Modem Detection Enable Register (FDE)

The Fax/Modem Detection Enable Register contains the enable bits of the fax/modem detection. If the enable bit is set to low, the corresponding bits (compressed and uncompressed input) in the Fax/Modem Detection Status FDS register will be reset.

| EM3 | EM2 | EM1 | EM0 | EAD3 | EAD2 | EAD1 | EAD0 |
|---|---|---|---|---|---|---|---|

**EM3 ... 0**

1 ... Enable Modem detection of corresponding channel 3, 2, 1 or 0

0 ... Disable Modem detection of corresponding channel 3, 2, 1 or 0

**EAD3 ... 0**

1 ... Enable Automatic Disable of echosuppressor of corresponding channel 3, 2, 1 or 0 as given by G.164. Disables ES if fax/modem is detected.

0 ... Disable the automatic deactivation if the echosuppressor if a fax/modem is detected.

### 3.10 Fax / Modem Detection Status Register (FDS)

The FAX/Modem Detection Status register contains the status of the FAX/Modem tone detection. If a tone is detected, the corresponding bit is set to '1'. The transition of any bit in the FDS register causes an interrupt at the $\overline{\text{INT}}$ pin. This interrupt is reset after a read of the FDS register. To reset a bit of the FDS register, the corresponding bit of the FDE register has to be reset. If then the bit of the FDE register is set to '1' again, the detection mechanism is ready for the next fax/modem detection.

The end of the fax/modem transmission also resets the corresponding bit and creates a new interrupt.

| DU3 | DU2 | DU1 | DU0 | DC3 | DC2 | DC1 | DC0 |
|---|---|---|---|---|---|---|---|

**DU3 ... 0** Detection at Uncompressed input of corresponding channel 3, 2, 1 or 0

**DC3 ... 0** Detection at Compressed input of corresponding channel 3, 2, 1 or 0

### 3.11 DSP Status Register (DST)

The DSP Status Register controls access to the DATAH and DATAL registers by the microcontroller.

| | | | | | | RDY2 | RDY1 |
|---|---|---|---|---|---|---|---|

**RDY2** 1 ... DSP 2 has completed processing the current command from the microcontroller.
0 ... indicates that the command from the microcontroller to DSP 2 is not yet completely processed by DSP 2.

**RDY1** 1 ... DSP 1 has completed processing the current command from the microcontroller.
0 ... indicates that the command from the microcontroller to DSP 1 is not yet completely processed by DSP 1.

### 3.12 Command Register (COM)

The COM register provides access to the DSP RAM. The access to both DSPs is simultaneously possible with the two status bits and the two command bits. The R/$\overline{W}$ bit selects read or write access. The status bits allows access to the RAM. The command bit releases the content of the DATA register to the DSP.

| R/$\overline{W}$ | | | | PD2 | PD1 | CMD2 | CMD1 |
|---|---|---|---|---|---|---|---|

**R/$\overline{W}$** Read/Write
1 ... read access to the DSP RAM
0 ... write access to the DSP RAM

**PD2** 1 ... DSP 2 is deactivated
0 ... DSP 2 is activated two frames later

**PD1** 1 ... DSP 1 is deactivated
0 ... DSP 1 is activated two frames later

**CMD2** A ’1’ indicates a read or write access of the microcontroller to DSP 2.
This bit is automatically reset when DSP 2 has read the COM register.

**CMD1** A ’1' indicates a read or write access of the microcontroller to DSP 1.
This bit is automatically reset when DSP 1 has read the COM register.

*Note: The PDi bit is only taken into account if the corresponding PDi pin is low. Setting the PDi pin to high forces the DSP to powerdown state.*

*Note: Read access to both DSP RAMs simultaneously is not permitted. The data would be lost as there is only one data register for high byte and low byte respectively.*

### 3.13 Address of DSP RAM Register (ADR)

The ADR register contains the DSP RAM address. The range is 0 to $FF_H$.

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|

### 3.14 DSP RAM Data High Byte Register (DATAH)

The DATAH register contains the high byte of the data for/from the DSP RAM.

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|

### 3.15 DSP RAM Data Low Byte Register (DATAL)

The DATAL register contains the low byte of the data for/from the DSP RAM.

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|

## 3.16 DSP RAM Loactions

Access to the DSP RAM is provided via the COM register, the DST register, the ADR register together with the DATAH and the DATAL registers. See sections **3.12** to **3.15** for register description. This section lists DSP parameters and addresses.

Each adress points to a 16 bit word. The 8 MSB are related to the DATAH register, the 8 LSB are related to the DATAL register. The table below summarizes the location of all parameters and gives a reference to the following sections with a detailed parameter description.

**Table 2 Summary of DSP Parameter Locations**

| RAM Adress (hex) | High Byte Nib. 3 | High Byte Nib. 2 | Low Byte Nib. 1 | Low Byte Nib. 0 | Function | refer to page |
|---|---|---|---|---|---|---|
| 00 | CT_FREQ [1] | | | | congestion tone | 61 |
| 01 | CT_LEV [1] | | CT_GAIN [1] | | generator | 61, 61 |
| 02 | TF_BW [1] | | TF_RES [1] | | tone filter | 62, 62 |
| 03 | TF_ATT [1] | | TF_SAT [1] | | | 63, 63 |
| 04 | - | | AEL_GAIN | | artificial echo loss | 63 |
| 05 | NM_LPlim | | SD_LIM | | speech detector | 65, 64 |
| 06 | SD_LP | | NM_OFF | | and | 64, 65 |
| 07 | NM_LPfade | | SP_PDN | | noise monitor | 65, 64 |
| 08 | NM_LPrise | | SD_PDS | | | 65, 64 |
| 09 | ES_ATT | | ES_DLY | | echo suppressor | 66, 66 |
| 0A | ES_RISE | | ES_FALL | | | 66, 67 |
| 0B | ES_PLdly | --- | ES_RxPL | | | 67, 67 |
| 0C | MD_FREQ | | | | modem detection | 68 |
| 0D | MD_BW | | | | | 68 |
| 0E | MD_LP | | MD_LIM | | | 68, 69 |
| 0F | MD_Tbreak | | MD_Thold | | | 69, 69 |
| 10 | MD_DIFF | | MD_LEV | | | 69, 69 |
| 11 | MD_LEVE | | MD_TIME | | | 69, 70 |

1) Applies only to DSP 2.

### 3.16.1 Programming DSP RAM Cells for Extended Features

To make use of the PEB 7274 features of echosuppression, fax/modem tone detection, tone generation and artificial echo loss special parameters located in the DSP RAM must be programmed. A typical programming sequence to write parameters to a DSP RAM cell and read the programmed values back for confirmation is described below.

*Note: DSP RAM cells are not loaded with default values after reset.*

**Example: Load RAM value for bandwidth of fax/modem detection with 100Hz**

Write DSP RAM with following parameters:

| | |
|---|---|
| DSP RAM Adress: | $0D_H$ |
| High Byte for 100Hz: | $22_H$ |
| Low Byte for 100Hz: | $B3_H$ |

| | | | |
|---|---|---|---|
| Write Data High Register (DATAH) | = $C0_H$ | $22_H$ | |
| Write Data Low Register (DATAL) | = $C4_H$ | $B3_H$ | |
| Write RAM address for parameter bandwidth (ADR) | = $BC_H$ | $0D_H$ | |
| Write simultaneously to DSP 1 and DSP 2 (COM) | = $B8_H$ | $03_H$ | |
| Read if RAM write operation is completed (DST) | = $34_H$ | => DST | = $03_H$ = OK |

Read back bandwidth RAM cell for DSP 1 and DSP 2 (ADR still $0D_H$):

| | | | |
|---|---|---|---|
| Read DSP1 bandwidth RAM cells (COM) | = $38_H$ | $81_H$ | |
| Read if RAM read operation is completed(DST) | = $34_H$ | => DST | = $01_H$ = OK |
| Read Data High Register (DATAH) | = $40_H$ | => DATAH | = $22_H$ = OK |
| Read Data Low Register (DATAL) | = $44_H$ | => DATAL | = $B3_H$ = OK |
| Read DSP2 bandwidth RAM cells (COM) | = $38_H$ | $82_H$ | |
| Read if RAM read operation is completed(DST) | = $34_H$ | => DST | = $02_H$ = OK |
| Read Data High Register (DATAH) | = $40_H$ | => DATAH | = $22_H$ = OK |
| Read Data Low Register (DATAL) | = $44_H$ | => DATAL | = $B3_H$ = OK |

*Note: DSP parameters given in tables show not the complete coding possibilities due to space limitation.*
*If values are required that are not listed below, complete tables are available on disk.*

### 3.16.2 Congestion Tone Generator

**Congestion Tone Frequency (CT_FREQ)**

This parameter specifies the frequency of the congestion tone that may be output on the uncompressed side instead of the PCM data.

Range: 0 Hz to 1 kHz

DSP range: $0000_H$ to $2000_H$

Coding: freq [kHz] = (CT_FREQ / 65536) x 8

**Congestion Tone Level (CT_LEV)**

The level of the congestion tone can be programmed using this parameter.

Range: 0 dB to -45 dB, -∞ dB

Coding: refer to table **3**

**Table 3 Values for the Congestion Tone Level**

| Hex Value | Level in dB | Hex Value | Level in dB | Hex Value | Level in dB | Hex Value | Level in dB |
|---|---|---|---|---|---|---|---|
| 10 | 0.00 | 22 | - 10.10 | 4C | - 24.64 | 72 | - 40.21 |
| 0B | - 1.16 | 31 | - 14.54 | 52 | - 28.16 | 7A | - 44.64 |
| 11 | - 2.50 | 40 | - 18.06 | 5B | - 31.26 | 08 | -10E9 |
| 13 | - 5.00 | 42 | - 22.14 | 67 | - 36.06 | | |

**Congestion Tone Frequency Gain (CT_GAIN)**

CT_GAIN determines the frequency gain.

Range: 0 dB to -48 dB, -∞ dB

Coding: refer to table **4**

**Table 4 Values for the Congestion Tone Frequency Gain**

| Hex Value | Gain in dB | Hex Value | Gain in dB | Hex Value | Gain in dB | Hex Value | Gain in dB |
|---|---|---|---|---|---|---|---|
| 10 | 0.00 | B2 | - 7.50 | 91 | - 18.06 | 8E | - 42.14 |
| 21 | - 3.25 | A1 | - 10.10 | 8B | - 24.08 | 8F | - 48.16 |
| 40 | - 5.00 | A0 | - 12.04 | 8C | - 30.10 | 90 | - 10E9 |
| 08 | - 6.02 | 92 | - 14.54 | 8D | - 36.12 | | |

### 3.16.3 Tone Filter

**Tone Filter Bandwidth (TF_BW)**

Determines the bandwidth of the tone filter.

Range: 0 to -1

Coding: refer to table **5**

**Table 5 Values for the Tone Filter Bandwidth**

| Hex Value | | Hex Value | | Hex Value | |
|---|---|---|---|---|---|
| 81 | 0.0000000 | 91 | - 0.5000000 | B2 | - 0.9062500 |
| 82 | - 0.2500000 | 92 | - 0.6250000 | FA | - 0.9980469 |
| 83 | - 0.3750000 | 94 | - 0.7187500 | | |
| 84 | - 0.4375000 | A2 | - 0.8125000 | | |

**Tone Filter Resonance Frequency (TF_RES)**

Range: 80 Hz to 2 kHz

Coding: refer to table **6**

**Table 6 Values for the Tone Filter Resonance Frequency**

| Hex Value | Freq. in Hz | Hex Value | Freq. in Hz | Hex Value | Freq. in Hz | Hex Value | Freq. in Hz |
|---|---|---|---|---|---|---|---|
| 81 | 2000.00 | 93 | 1034.83 | B4 | 480.31 | DC | 210.78 |
| 82 | 1678.28 | 9C | 858.33 | BC | 423.03 | F3 | 125.87 |
| 83 | 1510.57 | A3 | 721.37 | C3 | 357.05 | FA | 79.59 |
| 8F | 1321.82 | AC | 601.07 | CC | 298.43 | | |

**Tone Filter Attenuation Factor (TF_ATT)**

Determines the out-of-frequency attenuation.

Range: 0 dB to 48 dB

Coding: refer to table **7**

**Table 7 Tone Filter Attenuation**

| Hex Value | Atten. in dB | Hex Value | Atten. in dB | Hex Value | Atten. in dB | Hex Value | Atten. in dB |
|---|---|---|---|---|---|---|---|
| F1 | 48.16 | D0 | 30.10 | B0 | 18.06 | 90 | 6.02 |
| F0 | 42.14 | C0 | 24.08 | A0 | 12.04 | 80 | 0.00 |
| E0 | 36.12 | | | | | | |

**Tone Filter Saturation Amplification (TF_SAT)**

Range: -12 dB to 12 dB

Coding: refer to table **8**

**Table 8 Values for Tone Filter Saturation Amplification**

| Hex Value | Ampl. in dB | Hex Value | Ampl. in dB | Hex Value | Ampl. in dB | Hex Value | Ampl. in dB |
|---|---|---|---|---|---|---|---|
| 00 | 12.041 | 41 | 4.048 | 7C | -0.493 | B9 | -7.180 |
| 10 | 9.542 | 32 | 2.961 | 6B | -1.025 | A9 | -8.519 |
| 20 | 7.959 | 72 | 2.006 | 4A | -1.972 | 99 | -12.041 |
| 30 | 7.044 | 1A | 1.023 | CA | -3.059 | 08 | -10E9 |
| 70 | 6.088 | 3C | 0.462 | 49 | -5.494 | | |
| 21 | 5.460 | 09 | 0.000 | F9 | -6.089 | | |

### 3.16.4 Artificial Echo Loss Gain (AEL_GAIN)

Determines the level of the AEL added to the receive path.

Range: 0 dB to -45 dB, -∞ dB

Coding: refer to table **3** (CT_LEV)

### 3.16.5 Speech Detector and Noise Monitor

**Speech Detection Limit (SD_LIM)**

This parameter determines the maximum limit of a signal for speech detection.

Range: -96 dB to 0 dB

DSP range: $00_H$ to $7F_H$

Coding: limit [dB] = -96.32 + SD_LIM x 0.7525

**Speech Detection Lowpass (SD_LP)**

This parameter specifies how the main spikes of the signal are being eliminated.

Range: 1 ms to 170 ms

Coding: refer to table **9**

**Table 9 Values for the Time Constant**

| Hex Value | time in ms | Hex Value | time in ms | Hex Value | time in ms | Hex Value | time in ms |
|---|---|---|---|---|---|---|---|
| 00 | 0.94 | 34 | 15.00 | 54 | 60.17 | 64 | 120.41 |
| 0D | 2.00 | 41 | 21.27 | 5B | 73.08 | 6D | 132.07 |
| 1E | 4.00 | 44 | 30.06 | 61 | 85.27 | 6B | 146.22 |
| 23 | 7.05 | 51 | 42.60 | 62 | 102.34 | 71 | 170.60 |

**Peak Detector Noise (SD_PDN)**

This time constant specifies the .

Range: 1 ms to 170 ms

Coding: refer to table **9** (SD_LP)

**Peak Detector Speech (SD_PDS)**

This time constant specifies the .

Range: 1 ms to 170 ms

Coding: refer to table **9** (SD_LP)

### Noise Monitor Lowpass Limit (NM_LPlim)

This parameter determines the maximum value for the lowpass to detect continous tones as speech and to activate the echosuppressor.

Range: 0 dB to 47 dB

DSP range: $00_H$ to $3F_H$

Coding: limit [dB] = NM_LPlim x 0.7525

### Noise Monitor Offset (NM_OFF)

Specifies a level threshold between signal and noise.

Range: 0 dB to 47 dB

DSP range: $00_H$ to $3F_H$

Coding: limit [dB] = NM_OFF x 0.7525

### Noise Monitor Lowpass Fade Constant (NM_LPfade)

The fade constant enables the fast discharge of the noise monitor lowpass after the end of speech recognition.

Range: 1 ms to 170 ms

Coding: refer to table **9** (SD_LP)

### Noise Monitor Lowpass Rise Time (NM_LPrise)

This time constant determines the time the noise monitor is charged after speech is recognized

Range: 4 s to 58 s

Coding: refer to table **10**

**Table 10 Values for the Time Constant of the Noise Monitor Lowpass**

| Hex Value | time in ms | Hex Value | time in ms | Hex Value | time in ms | Hex Value | time in ms |
|---|---|---|---|---|---|---|---|
| 00 | 4.10 | 0D | 8.46 | 1C | 17.48 | 2C | 34.95 |
| 01 | 5.46 | 11 | 10.92 | 21 | 21.85 | 31 | 43.69 |
| 02 | 6.55 | 12 | 13.11 | 22 | 26.21 | 32 | 52.43 |
| 04 | 7.71 | 13 | 14.56 | 24 | 30.84 | 33 | 58.25 |

### 3.16.6 Echo Suppressor

**Echosuppressor Attenuation (ES_ATT)**

The parameter ES_ATT determines the level of attenuation ATT (refer to figure **15**) in the receive path if speech has been detected in the transmit path and the estimation of receive power is below specified limit.

Range: 0 dB to -16 dB

DSP range: $80_H$ to $14_H$

Coding: suppressor attenuation [dB] = 20 x log (ES_ATT / 128)

**Echosuppressor Delay (ES_DLY)**

ES_DLY specifies the delay time $t_{dly}$ between the disappearance of speech in the transmit path (speechdetector = no speech) and the start of the fall time of the echosuppressor.

Range: 4 ms to 1020 ms

DSP range: $00_H$ to $FF_H$

Coding: $t_{dly}$ [ms] = 4 x ES_DLY

**Echosuppressor Rise Time (ES_RISE)**

ES_TR specifies the rate at which attenuation is increased from 0 dB to the programmed value if speech was detected by the speech detector. This rate determines the rise time $t_R$ .

Range: 0.025 dB/ms to 5.6 dB/ms

Coding: refer to table **11**

**Table 11 Values for the rate determing the rise time**

| Hex Value | rate in db/ms | Hex Value | rate in db/ms | Hex Value | rate in db/ms | Hex Value | rate in db/ms |
|---|---|---|---|---|---|---|---|
| 7A | - 0.025 | 43 | - 0.306 | 22 | - 1.370 | 11 | - 3.336 |
| 61 | - 0.101 | 3C | - 0.510 | 21 | - 1.647 | 07 | - 4.520 |
| 53 | - 0.152 | 31 | - 0.819 | 1C | - 2.066 | 03 | - 5.066 |
| 51 | - 0.203 | 2C | - 1.025 | 12 | - 2.768 | 02 | - 5.652 |

### Echosuppressor Fall Time (ES_FALL)

This parameter determines the rate at which attenuation is decreased from the programmed value to 0 dB if speech in the transmit path disappeared or the power level in the receive path exceeded the specified value. This rate determines the fall time $t_F$.

Range: 0.01 dB/ms to 2.13 dB/ms

Coding: refer to table **12**

**Table 12 Values for the rate determing the fall time**

| Hex Value | rate in db/ms | Hex Value | rate in db/ms | Hex Value | rate in db/ms | Hex Value | rate in db/ms |
|---|---|---|---|---|---|---|---|
| 72 | 0.010 | 23 | 0.304 | 12 | 0.675 | 03 | 1.210 |
| 5B | 0.029 | 21 | 0.405 | 11 | 0.809 | 02 | 1.344 |
| 41 | 0.101 | 1C | 0.507 | 0C | 1.010 | 01 | 1.609 |
| 31 | 0.203 | 13 | 0.608 | 05 | 1.110 | 00 | 2.138 |

### Echosuppressor Reveice Power Level Delay (ES_PLdly)

This coefficient specifies the time constant for the power estimator of the receive signal.

Range: 180 µs to 16 ms

DSP range: $01_H$ to $07_H$ (only the 4 MSBs are used)

Coding: $t_{PLdly}$ [ms] = -0.125 / ln (1-$2^{-ES\_PLdly}$)

### Echosuppressor Reveice Power Level (ES_RxPL)

The ES_RxPL parameter specifies the power level threshold for receive direction. If the signal in the receive path exceeds the programmed value the attenuation added by the echosuppressor will be switched off after $t_{PLdly}$ has elapsed.

This guarantees that despite of echosuppression the participant on the other side of the line can switch off echosuppression by speaking loud.

Range: -∞ dB, -48 dB to 0 dB

DSP range: $00_H$ to $FF_H$

Coding: threshold [dB] = 20 x log (ES_RxPL / 256)

### 3.16.7 Fax/Modem Detection

**Fax/Modem Detection Center Frequency (MD_FREQ)**

The parameter MD_FREQ specifies the center frequency of the fax/modem tone that is to be detected.

Range: 1.5 kHz to 2.5 kHz

Coding: refer to table **13**

**Table 13 Values for the Fax/Modem Detection Center Frequency**

| Hex Value | Freq. in Hz | Hex Value | Freq. in Hz | Hex Value | Freq. in Hz | Hex Value | Freq. in Hz |
|---|---|---|---|---|---|---|---|
| 01 4E | 1500 | 1B 80 | 1800 | A2 62 | 2100 | 82 CC | 2400 |
| 02 CD | 1600 | 22 64 | 1900 | 93 07 | 2200 | 81 4F | 2500 |
| 0C 51 | 1700 | 01 80 | 2000 | 8C 4C | 2300 | | |

**Fax/Modem Detection Bandwidth (MD_BW)**

The parameter MD_BW specifies the range around the center frequency within the fax/modem tone detection is allowed.

Range: 1 Hz to 500 Hz

Coding: refer to table **14**

**Table 14 Values for the Fax/Modem Detection Bandwidth**

| Hex Value | Freq. in Hz | Hex Value | Freq. in Hz | Hex Value | Freq. in Hz | Hex Value | Freq. in Hz |
|---|---|---|---|---|---|---|---|
| C8 4C | 1.09 | 32 C5 | 50.03 | 13 30 | 200.83 | 0D BC | 350.04 |
| 49 EA | 10.06 | 22 B3 | 100.10 | 0A 36 | 250.19 | 04 17 | 400.17 |
| 45 85 | 20.01 | 1B B6 | 150.02 | 0B 2C | 300.39 | 02 23 | 500.37 |

**Fax/Modem Detection Lowpass (MD_LP)**

This parameter specifies the time constant for the power estimators in the fax/modem detection.

Range: 1 ms to 170 ms

Coding: refer to table **9**

### Fax/Modem Detection Limit (MD_LIM)

The level programmed in MD_LIM is compared with the output of the modem filter. If the level of the modem signal is above MD_LIM fax/modem detection can be activated.

Range: 0 dB to 96 dB

DSP range: $7F_H$ to $00_H$

Coding: limit [dB] = -96.32 + SD_LIM x 0.7525

### Fax/Modem Detection Break Time (MD_Tbreak)

Tone breaks less than the specified time are ignored.

Range: 0.5 ms to 127.5 ms

Resolution: $01_H$ to $FF_H$

Coding: time [ms] = 0.5 x MD_Tbreak

### Fax/Modem Detection Hold Time (MD_Thold)

MD_Thold specifies the time the detection conditions have to be valid for fax/modem detection.

Range: 8 ms to 2 s

Resolution: $01_H$ to $FF_H$

Coding: time [ms] = 8 x MD_Thold

### Fax/Modem Detection Difference (MD_DIFF)

This parameter specifies the difference the outputs of the bandpass and the notch filter have to exceed. If the difference of the signal energy in the modem frequency band and out of the modem frequency band is larger than MD_DIFF a modem signal can be detected.

Range: - 96 dB to 96 dB

DSP range $00_H$ to $FF_H$

Coding: delta [dB] = sign (MD_DIFF) x | MD_DIFF | x 0.7525
| MD_DIFF | are the 7 LSBs of the RAM location.

### Fax/Modem Detection Level (MD_LEV)

MD_LEV determines the threshold below which noise or signals are ignored.

Range: 0 dB to 96 dB

Resolution: $00_H$ to $7F_H$

Coding: level [dB] = MD_LEV x 0.7525

### Fax/Modem End of Detection Level (MD_LEVe)

The parameter specifies the level for the end of the fax/modem detection.

Range: 0 dB to 96 dB

Resolution: $00_H$ to $7F_H$

Coding: level [dB] = MD_LEV x 0.7525

### Fax/Modem End of Detection Time (MD_TIMe)

The parameter specifies the timing conditions for the end of the fax/modem detection.

Range: 8 ms to 2 s

Resolution: $01_H$ to $FF_H$

Coding: time [ms] = 8 x MD_TIME

# 4 Electrical Characteristics

## 4.1 Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | Unit |
|---|---|---|---|
| Ambient temperature under bias: PEB<br>PEF | $T_A$<br>$T_A$ | 0 to 70<br>– 40 to 85 | °C<br>°C |
| Storage temperature | $T_{stg}$ | – 65 to 125 | °C |
| Voltage on any pin with respect to ground | $V_S$ | – 0.3 to $V_{DD}$ + 0.3 | V |
| Maximum voltage on any pin | $V_{max}$ | 7 | V |

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## 4.2 DC Characteristics

PEB: $T_A$ = 0 to 70 °C; $V_{DD}$ = 5 V ± 5 %, $V_{SS}$ = 0 V
PEF: $T_A$ = – 40 to 85 °C; $V_{DD}$ = 5 V ± 5 %, $V_{SS}$ = 0 V

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| High level input voltage | $V_{IH}$ | 2.0 | | $V_{DD}$ + 0.3 | V | |
| Low level input voltage | $V_{IL}$ | – 0.3 | | 0.8 | V | |
| Low level input leakage current | $I_{LL}$ | – 1 | | | µA | $V_{IN} = V_{SS}$<br>$T_A \geq 0°$ C<br>all pins except XTAL1 |
| | | – 10 | | | µA | $V_{IN} = V_{SS}$<br>– 40° C ≤ $T_A$ < 0° C<br>all pins except XTAL1 |
| High level input leakage current | $I_{LH}$ | | | 1 | µA | $V_{IN} = V_{DD}$<br>$T_A \geq 0°$ C<br>all pins except XTAL1 |
| | | | | 10 | µA | $V_{IN} = V_{DD}$<br>– 40° C ≤ $T_A$ < 0° C<br>all pins except XTAL1 |
| XTAL1 leakage current | $I_{LX}$ | | | 10 | µA | 0 V < $V_{IN}$ < $V_{DD}$ to 0 V<br>whole temperature range |
| High level output voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = - 400 µA |
| Low level output voltage | $V_{OL}$ | | | 0.45 | V | $I_{OL}$ = 7 mA<br>(pins $\overline{DOC}$, DOU, $\overline{INT}$)<br>$I_{OL}$ = 2 mA<br>(all other pins) |
| Power supply current | $I_{CC}$ | | 60 | | mA | operational |
| | | | 10 | | mA | both DSPs in power down mode |

*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A$ = 25°C and the given supply voltage.*

## 4.3 Capacitances

$T_A$ = 25 °C; $V_{DD}$ = 5 V ± 5 %, $V_{SS}$ = 0 V

| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| Input capacitance | $C_{IN}$ | | 10 | pF |
| Output capacitance | $C_{OUT}$ | | | pF |
| I/O capacitance | $C_{I/O}$ | | | pF |

## 4.4 AC Characteristics

Ambient temperature under bias range, $V_{DD}$ = 5 V ± 5 %.

Inputs are driven at 2.4 V for a logical ’1’ and at 0.4 V for a logical ’0’. Timing measurements are made at 2.0 V for a logical ’1’ and at 0.8 V for a logical ’0’. The AC testing input/output waveforms are shown below.

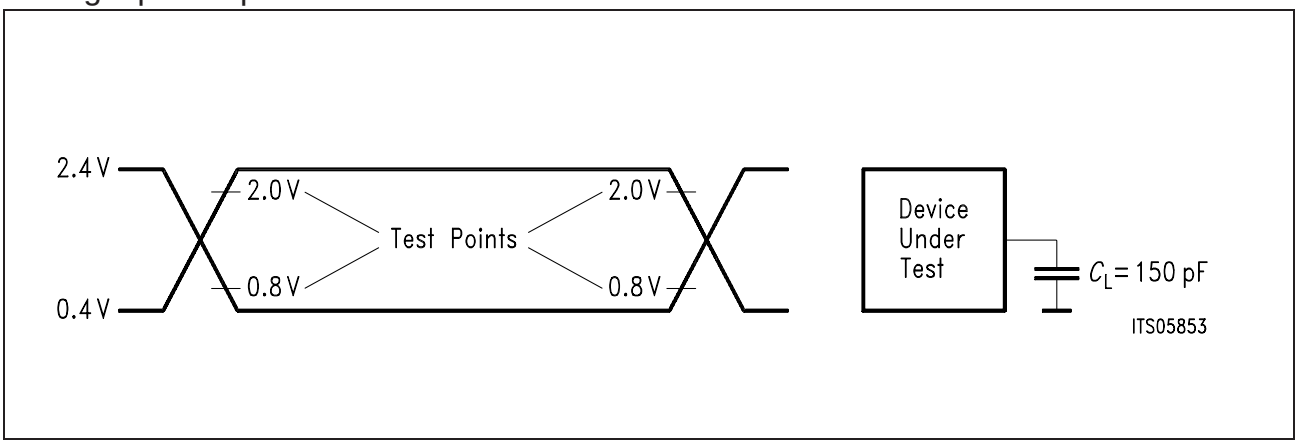



**Figure 28 I/O Waveforms for AC Tests**

### 4.4.1 PCM Interface Timing

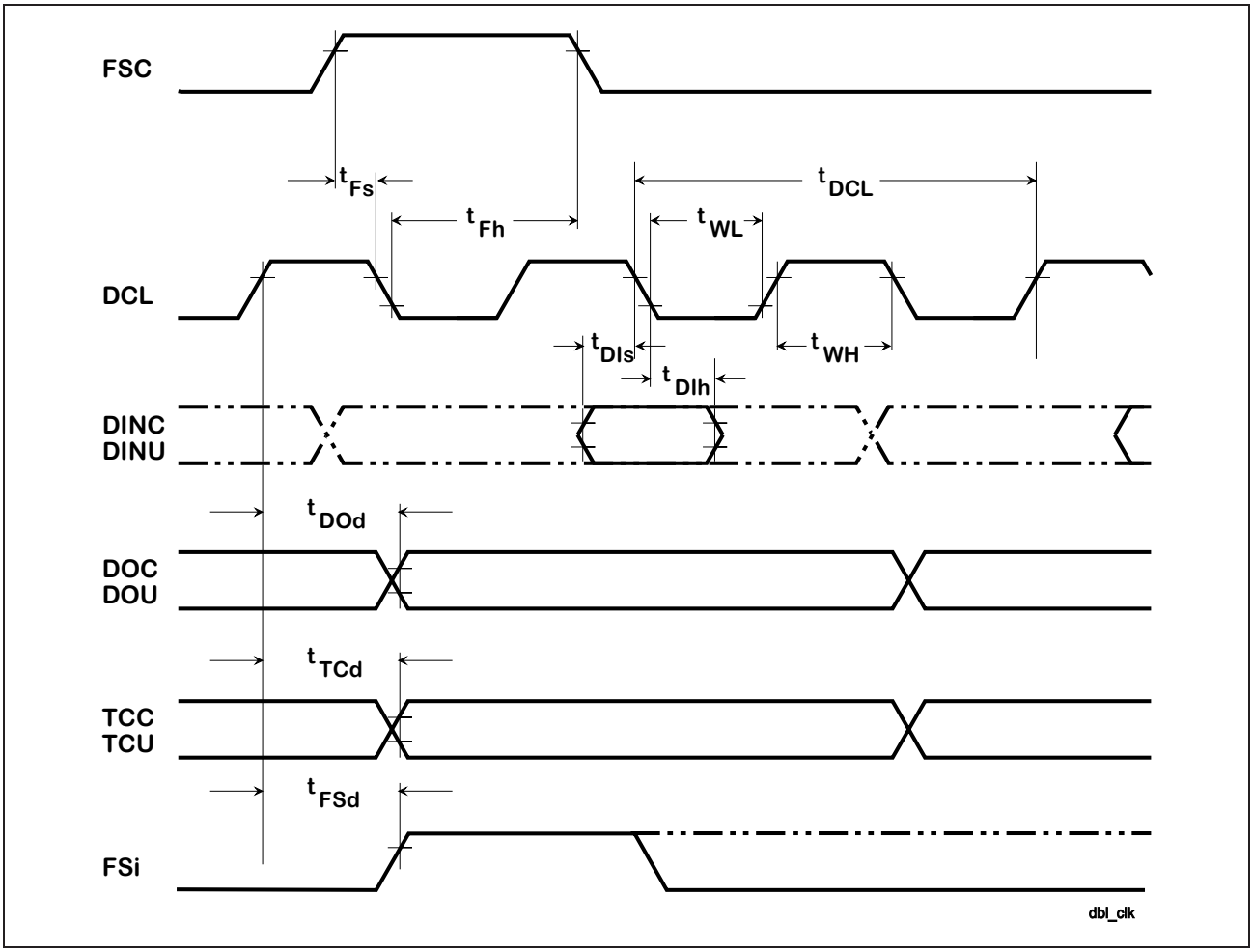



**Figure 29 PCM Interface Timing in Double Clocking Model**

| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| DCL clock period | $t_{DCL}$ | 244 | | ns |
| DCL pulse width | $t_{WL}$, $t_{WH}$ | 53 | | ns |
| FSC setup time | $t_{Fs}$ | 20 | | ns |
| FSC hold time | $t_{Fh}$ | 10 | | ns |
| Data Out delay | $t_{DOd}$ | | 60 | ns |
| Data In setup time | $t_{DIs}$ | 73 | | ns |
| Data In hold time | $t_{DIh}$ | 50 | | ns |
| Tristate Control delay | $t_{TCd}$ | | 50 | ns |
| Frame Strobe delay | $t_{FSd}$ | | 50 | ns |

### 4.4.2 Serial Microcontroller Interface Timing

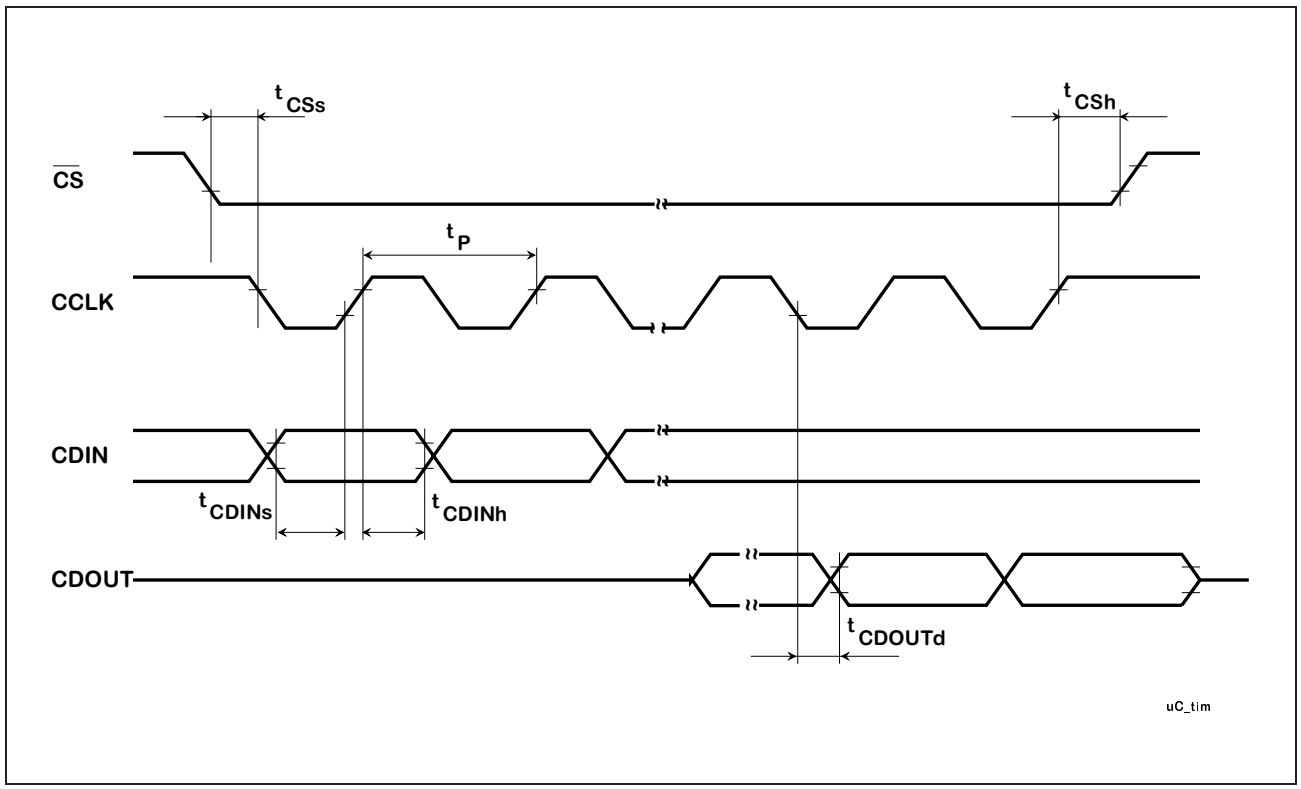



**Figure 30 Serial µC Interface Timing**

| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| Clock period | $t_P$ | 130 | | ns |
| Chip Select setup time | $t_{CSs}$ | 0 | | ns |
| Chip Select hold time | $t_{CSh}$ | 10 | | ns |
| CDIN setup time | $t_{CDINs}$ | 20 | | ns |
| CDIN hold time | $t_{CDINh}$ | 20 | | ns |
| CDOUT data out delay | $t_{CDOUTd}$ | | 40 | ns |

### 4.4.3 Boundary Scan Timing

| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| Test clock period | $t_{TCP}$ | 100 | - | ns |
| Test clock period low | $t_{TCPL}$ | 40 | - | ns |
| Test clock period high | $t_{TCPH}$ | 40 | - | ns |
| TMS set-up time to TCK | $t_{MSS}$ | 20 | - | ns |
| TMS hold time from TCK | $t_{MSH}$ | 20 | - | ns |
| TDI set-up time to TCK | $t_{DIS}$ | 20 | - | ns |
| TDI hold time from TCK | $t_{DIH}$ | 20 | - | ns |
| TDO valid delay from TCK | $t_{DOD}$ | - | 40 | ns |

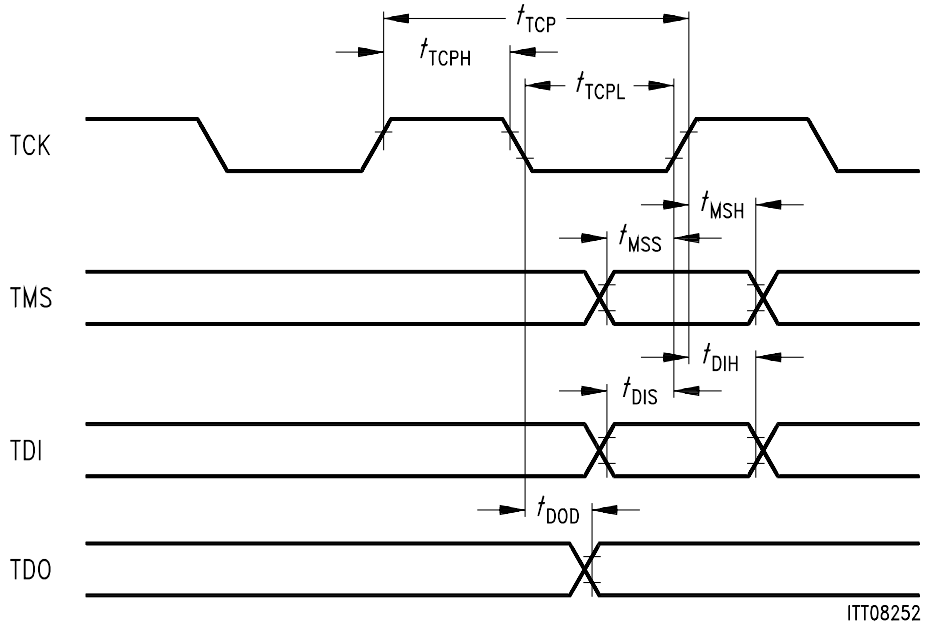



**Figure 31 Boundary Scan Timing**

### 4.4.4 BCL Timing

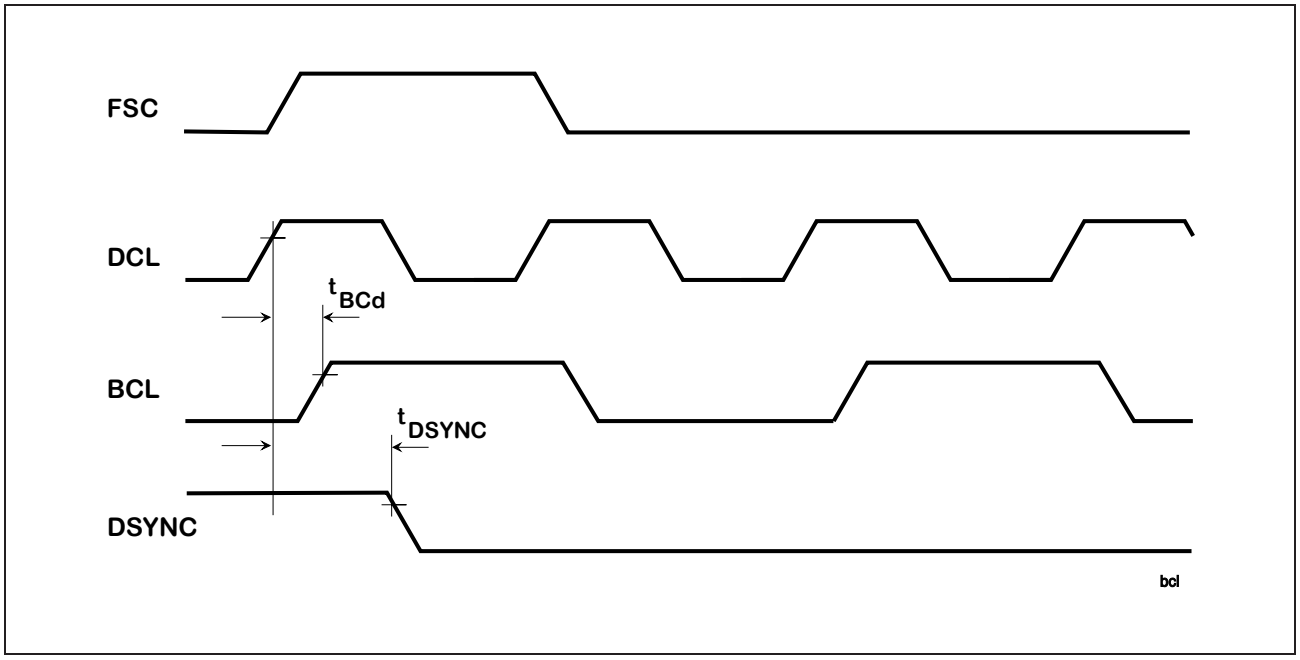
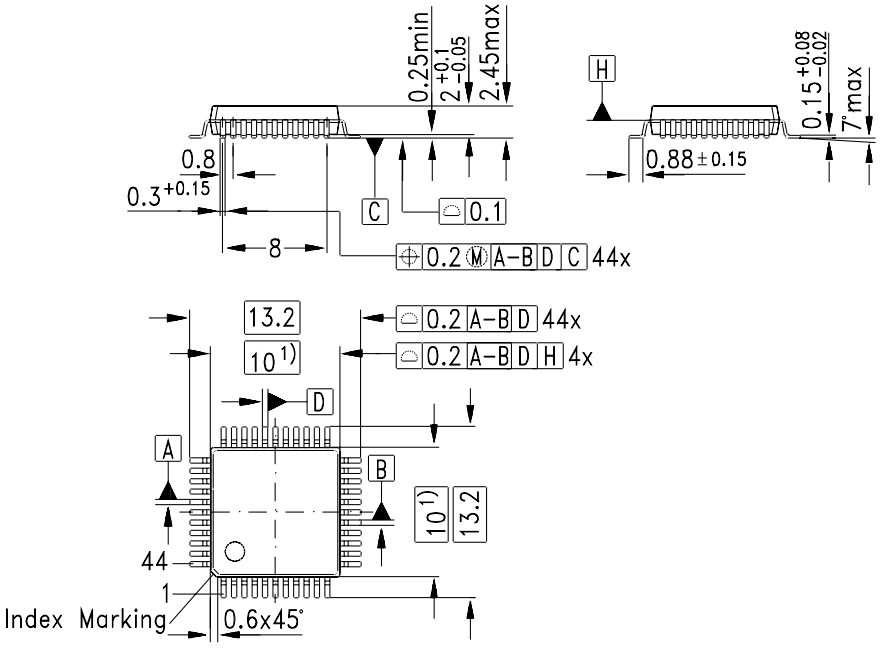



**Figure 32 Bit Clock Timing**

| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| Bit Clock delay | $t_{BCd}$ | | 25 | ns |
| DSYNC delay | $t_{DSYNC}$ | | 80 | ns |

## 5 Package Outlines

**Plastic Package, P-MQFP-44**
(Plastic Metric Quad Flat Package)




1) Does not include plastic or metal protrusions of 0.25 max per side

# 6 Appendix

## 6.1 Proposed Default Values for DSP Locations

| RAM Adress (hex) | Function | proposed value (hex) | effect |
|---|---|---|---|
| 00 | tone generator | 0D 99 | CT_FREQ = 425 Hz |
| 01 | | 22 08 | CT_LEV = -10 dB, CT_GAIN = -6 dB |
| 02 | tone filter | FA BC | TF_BW = -0.99, TF_RES = 423 Hz |
| 03 | | F1 09 | TF_ATT = 48 dB, TF_SAT = 0 dB |
| 04 | artificial echo loss | 00 4C | AEL_GAIN = -24.64 dB |
| 05 | speech detector | 10 4A | NM_LPlim = 12 dB, SD_LIM = -40 dB |
| 06 | | 1E 08 | SD_LP = 4 ms, NM_OFF = 6 dB |
| 07 | | 41 44 | NM_LPfade = 21 ms, SD_PDN = 30 ms |
| 08 | | 00 62 | NM_LPrise = 4s, SD_PDS = 102 ms |
| 09 | echo suppressor | 20 10 | ES_ATT = -12 dB, ES_DLY = 64 ms |
| 0A | | 11 21 | ES_RISE = -3.3 dB/ms<br>ES_FALL = 0.4 dB/ms |
| 0B | | 50 51 | ES_PLdly = 4 ms, ES_RxPL = -10 dB |
| 0C | modem detection | A2 62 | MD_FREQ = 2100 Hz |
| 0D | | 22 B3 | MD_BW = 100 Hz |
| 0E | | 31 00 | MD_LP = 10 ms, MD_LIM = -96 dB |
| 0F | | 02 32 | MD_Tbreak = 1 ms, MD_Thold =0.4 s |
| 10 | | 10 45 | MD_DIFF = 12 dB, MD_LEV =-44 dB |
| 11 | | 3B 3E | MD_LEVE = -44 dB, MD_TIME = 0.5 s |

## 6.2 Working Sheet for Register Programming

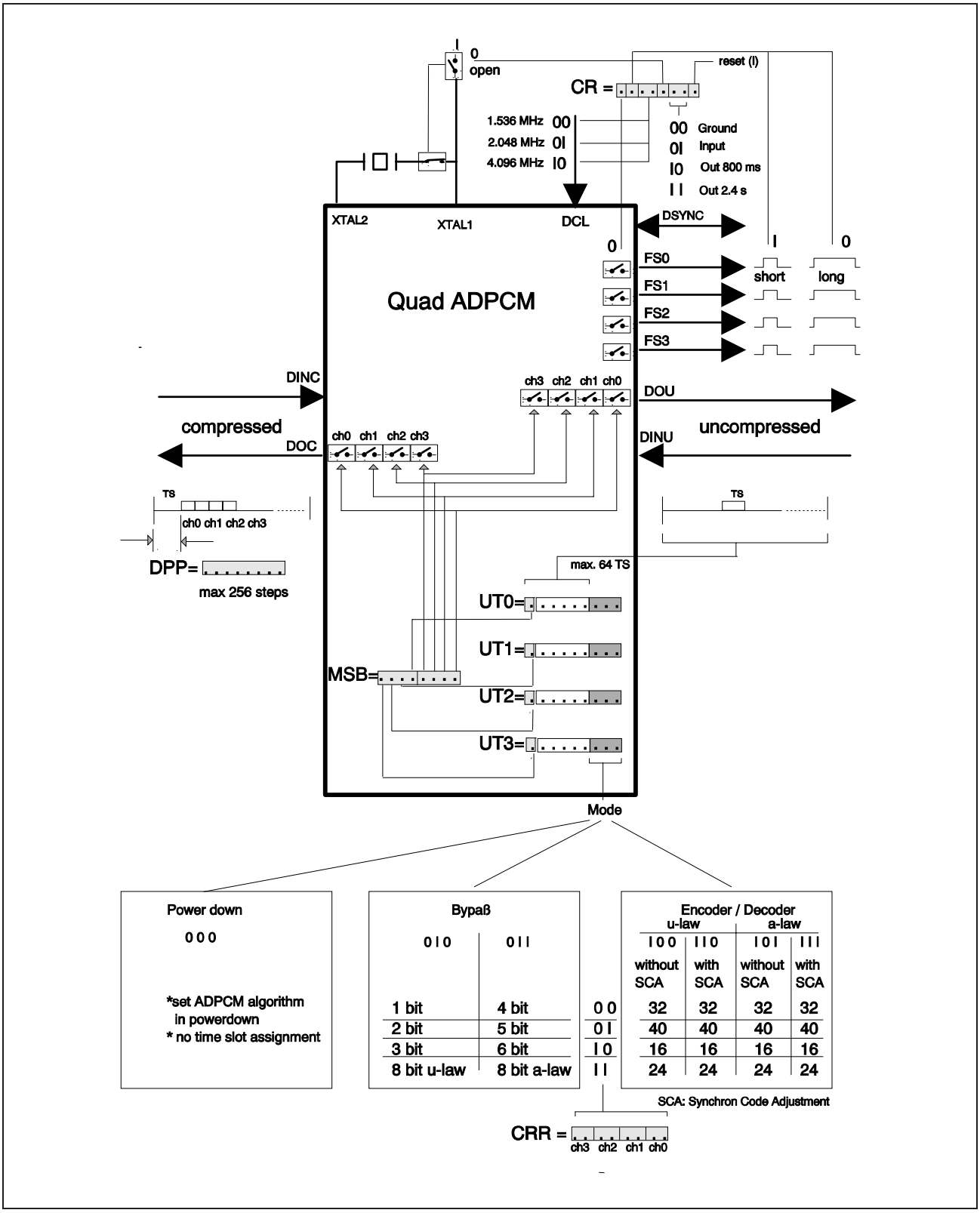



**Figure 33 Working Sheet for Register Programming**

## 6.3 Development Tools

### 6.3.1 STSI 4000 PCM-4 Userboard Kit

| Description | Part Number | Ordering Code |
|---|---|---|
| PCM-4 Userboard Kit | STSI 4000 | Q67100-H6865 |

The STSI 4000 Kit consists of a Remote Terminal (RT) board and a Central Office Terminal (COT) board to set up a fully operational PCM-4 demonstration. These boards can be combined with standard analog telephones and a standard analog PBX to have a complete system. The principle of STSI 4000 is shown in **figure 34**.

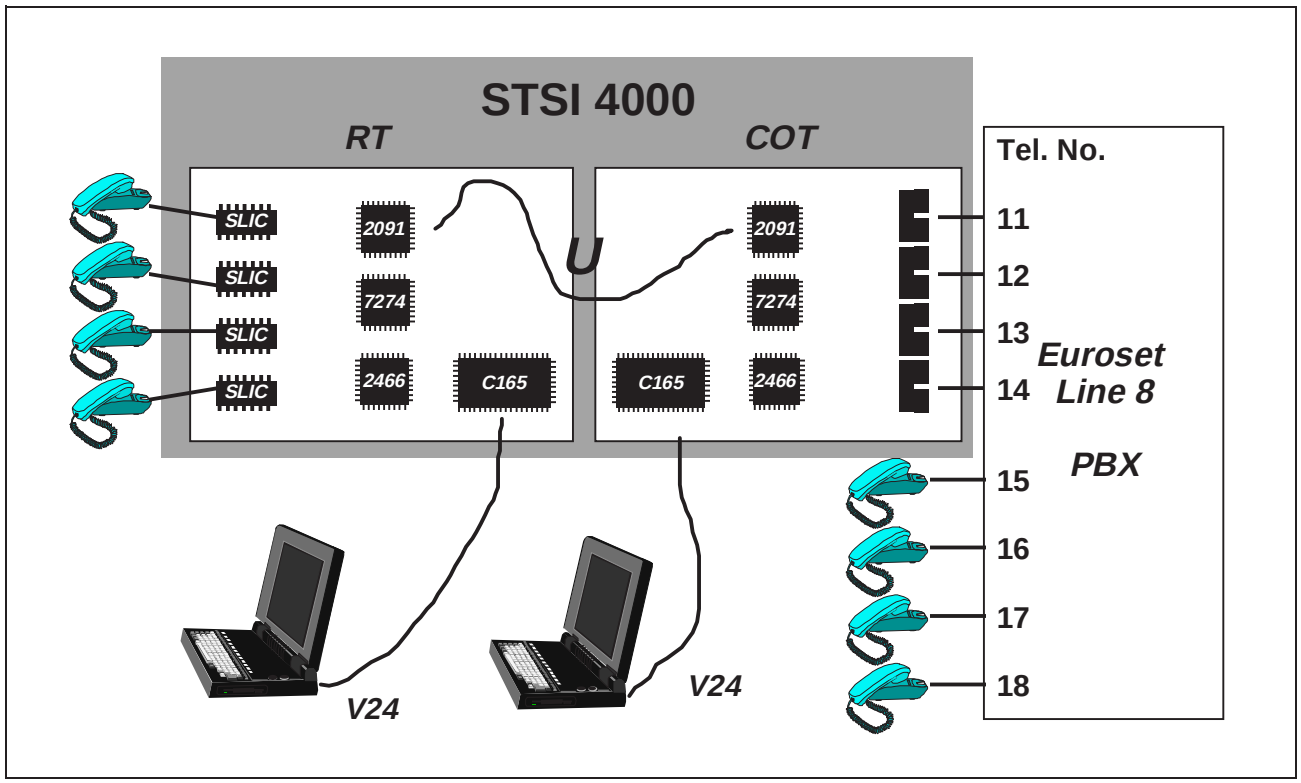



**Figure 34 STSI 4000 PCM4 Userboard Kit (Euroset not included in Kit)**

Via a V.24 connection it is possible to read and write to all PEB 7274 and PEB 2091 V5.x registers. Addtional commands allow to control and monitor PEB 2466 specific functions like hook on/off detection, channel allocation etc. This allows to program very efficiently different configurations and test device functionality. Alternatively the user can download his own C165 program to test realtime behavior. From mid 1997 onwards additionally a software package including sourcecode will be available which provides basic modules to operate the STSI 4000 as a PCM-4 system without the need for external V.24 interfaces.

The STSI 4000 boards contains all hardware required in typical PCM-4 system with the exception of phantom power-supply & feeding and ringing / TTX generation.

### 6.3.2 SIPB 7274 Quad ADPCM Kit

| Description | Part Number | Ordering Code |
|---|---|---|
| Quad ADPCM Kit | SIPB 7274 | Q67100-H6866 |

The SIPB 7274 Quad ADPCM Kit consists of a SIPB 7274 board containing two Quad ADPCM controllers operating back-to-back, a EVC50 microcontroller board based on a C513 processor and the EVC50 bus to connect optionally (not included in SIPB 7274 kit) a PEB 2465/6 evaluation board (e.g. SIPS 2466). This configuration allows fast testing of all PEB 7274 features.

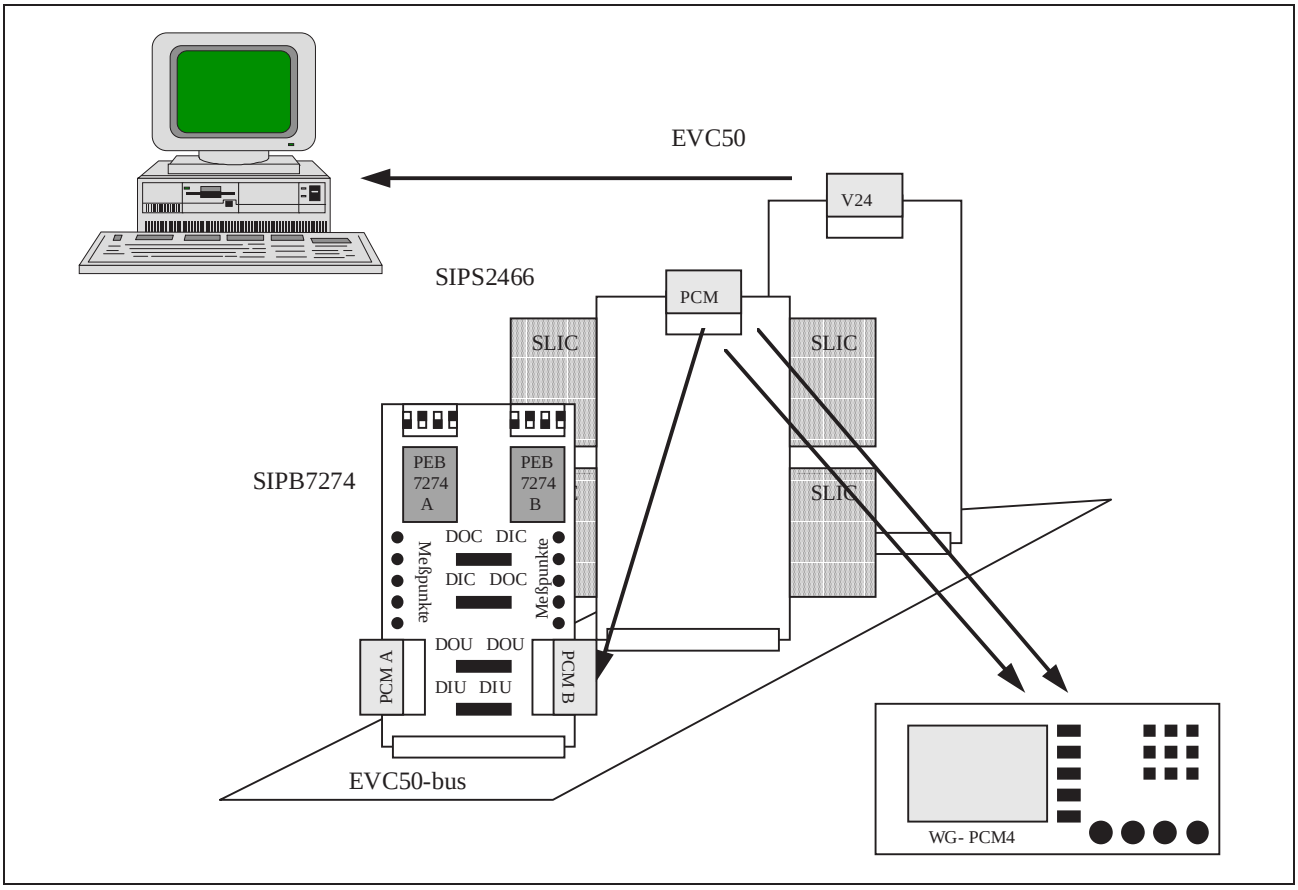



**Figure 35 SIPB 7274 Quad ADPCM Kit**

PCM coded (uncompressed) data is extracted/inserted at PCM A connector and compressed by PEB 7274 (A). Optionally the compressed in- and outputs of PEB 7274 (B) can directly connected to those of PEB 7274 (A) to provide a back-to back operation of device 'A' and device 'B'. The uncompressed data of PEB 7274 (B) can be extracted/ inserted at connector PCM B. Numerous access points on the board allow easy monitoring of all PEB 7274 signals.