REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Redrawn with changes made under NOR No. 5962-R116-92 Revision B and NOR No. 5962-R004-93 Revision C. Added vendor CAGE numbers 65896 and OK6N4 to the drawing as sources of supply. Added device types 10UX, 10YX, 11UX, 11YX, and 12UX, 12YX. Removed vendor CAGE number 0BYV4 from drawing as source of supply. Removed vendor cage number 61772 as a source of supply for devices 01ZX, 02ZX, 03ZX, 05XX, 05YX, 05ZX, 05UX, 06ZX, 07XX, 07YX, 07ZX, 07UX, 08XX, 08YX, 08ZX, 08UX, 09XX, 09YX, 09ZX, and 09UX. Added vendor cage 61772 as a source of supply for devices 01MX, 01NX, 02MX, 02NX, 03MX, 03NX, 04NX, 04MX, 06MX, and 06NX. Removed vendor cage 34649 as a source of supply for devices 02XX, 02YX, 04XX, and 04YX. Editorial changes throughout.	94-01-04	M. A. FRYE

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV			D	D															
SHEET	15	16	17	18															

REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D				
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
3 June 1988

REVISION LEVEL
D

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 32K X 8 STATIC RANDOM ACCESS MEMORY (SRAM) LOW POWER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88552
A	67268	

SHEET 1 OF 18

DESC FORM 193
JUL 91

5962-E468-93

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.4	32K x 8 low power CMOS SRAM	100 ns
02, 07			70 ns
03, 08			55 ns
04, 09			45 ns
05			35 ns
06			25 ns
10			20 ns
11			17 ns
12			15 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	CDFP3-F28	28	Flat pack
U	CDIP3-T28 or GDIP4-T28	28	Dual-in-line
T	CDFP4-F28	28	Flat pack
M	CQCC3-N28	28	Rectangular leadless chip carrier
N	GDFP2-F28	28	Flat pack

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc 2/
Input voltage range	-0.5 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+150°C 3/
Power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-BUL- 103.
2/ All voltages referenced to V_{CC}.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc 1/
Ground voltage (V_{SS})	0 V dc
Input high voltage (V_{IH})	+2.2 V dc to V_{CC} +0.5 V dc
Input low voltage (V_{IL})	-0.5 V dc to .8 V dc
Case operating temperature (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

1/ All voltages referenced to V_{CC}.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current	I_{LI}	V_{CC} = max, V_{IN} = GND to V_{CC}	1,2,3	All		10	µA
Output leakage current	I_{LO}	V_{CC} = max, V_{OUT} = GND to V_{CC} $\overline{CE} \ge V_{IH}$; $\overline{WE} \le V_{IL}$	1,2,3	All		10	µA
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1,2,3	All		.4	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4 mA, V_{IL} = 0.8 V, V_{IH} = 2.2 V	1,2,3	All	2.4		V
Data retention voltage	V_{DR}		1,2,3	All	2.0		V
Operating supply current (active)	I_{CC1}	V_{CC} = 5.5 V, f = f max 1/, $\overline{CE}$ = V_{IL}, outputs open, all other inputs at V_{IL}	1,2,3	01,02,07		100	mA
				03,08		125	
				04,09		135	
				05		145	
				06,11		155	
				10		150	
				12		160	
Standby power supply current (TTL)	I_{CC2}	$\overline{CE} \ge V_{IH}$, outputs open V_{CC} = 5.5 V, f = 0 MHz	1,2,3	01-04		3	mA
				05-09		5	
				10-12		10	
Standby power supply current (CMOS)	I_{CC3}	$\overline{CE} \ge (V_{CC}$-0.2 V), f = 0 MHz, outputs open, V_{CC} = 5.5 V all other inputs $\le$ 0.2 V or $\ge$ (V_{CC} -0.2 V)	1,2,3	05, 07-09		900	µA
				01-04, 06		1.5	mA
				10-12		5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data retention current	I_{CC4} 2/	V_{CC} = 3.0 V, $\overline{CE} \ge (V_{CC} - 0.2\ V)$ f = 0 MHz, outputs open, all other inputs $\le$ 0.2 V or $\ge (V_{CC} - 0.2\ V)$	1,2,3	05, 07-09		350	µA
				01-04, 06		800	
				10-12		750	
Input capacitance	C_I 2/	V_I = 5.0 V or GND, f = 1 MHz, T_C = +25°C, See 4.3.1c	4	All		12	pF
Output capacitance	C_O 2/	V_O = 5.0 V or GND, f = 1 MHz, T_C = +25°C, See 4.3.1c	4	All		12	pF
Read cycle time	t_{AVAV}	3/	9,10,11	01	100		ns
				02,07	70		
				03,08	55		
				04,09	45		
				05	35		
				06	25		
				10	20		
				11	17		
				12	15		
Address access time	t_{AVQV}		9,10,11	01		100	ns
				02,07		70	
				03,08		55	
				04,09		45	
				05		35	
				06		25	
				10		20	
				11		17	
				12		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, $4.5 V \le V_{CC}$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip-enable access time	t_{ELQV}		9,10,11	01		100	ns
				02,07		70	
				03,08		55	
				04,09		45	
				05		35	
				06		25	
				10		20	
				11		17	
				12		15	
Output hold from address change	t_{AVQX}		9,10,11	All	3		ns
Output enable to output valid	t_{OLQV}		9,10,11	01		60	ns
				02-04, 07-09		35	
				05,06		20	
				10,11		10	
				12		8	
Chip select to output in low Z	t_{ELQX} 2/ 4/		9,10,11	All	3		ns
Chip deselect to output in high Z	t_{EHQZ} 2/ 4/	3/	9,10,11	01-04, 07,09		35	ns
				05,06		20	
				10-12		10	
Output disable to output in high Z	t_{OHQZ} 2/ 4/		9,10,11	01-04, 07,09		35	ns
				05,06		20	
				10-12		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{SS} = 0 V, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write enable to output in high Z	t_{WLQZ} 2/ 4/		9,10,11	01		50	ns
				02-04, 07-09		35	
				05,06		20	
				10-12		10	
Output enable to output in low Z	t_{OLQX} 2/ 4/		9,10,11	All	0		ns
Retention time	t_{cdr}	$\overline{CE} \ge V_{CC}$ -0.2 V	9,10,11	All	0		ns
Operation recovery time	t_R 2/	$\overline{CE} \ge V_{CC}$ -0.2 V	9,10,11	All	t_{AVAV}		ns
Data valid to end of write	t_{DVWH} t_{DVEH}		9,10,11	01-04, 07-09	35		ns
				05,06	15		
				10-12	10		
Data hold time	t_{WHDX} t_{EHDX}		9,10,11	01-09	3		ns
				10-12	0		
Output active from end of write	t_{WHQX} 2/ 4/		9,10,11	01-09	3		ns
				10-12	0		
Write cycle time	t_{AVAV}		9,10,11	01	100		ns
				02,07	70		
				03,08	55		
				04,09	45		
				05	35		
				06	25		
				10,11	20		
				12	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, $4.5\ V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip select to end of write	t_{ELWH}	3/	9,10,11	01	90		ns
				02,07	60		
				03,08	50		
				04,09	40		
				05	30		
				06	20		
				10,11	15		
				12	12		
Address valid to end of write	t_{AVWH}		9,10,11	01	85		ns
				02,07	60		
				03,08	50		
				04,09	40		
				05	30		
				06	20		
				10,11	15		
				12	12		
Address-setup time	t_{AVEL}		9,10,11	All	0		ns
Write pulse width	t_{WLWH}		9,10,11	01	55		ns
				02,07	45		
				03,08	40		
				04,09	35		
				05	30		
				06	25		
				10,11	15		
				12	12		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V $\le V_{CC}$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write recovery time	t_{WHAX}		9,10,11	01-09	7		ns
	t_{EHAX}			10-12	0		

1/ f max = $1/t_{AVAV}$.
2/ This parameter tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in table I.
3/ For output load circuits see figure 3 and for timing waveforms see figure 4.
4/ Transition is measured ±500 mV from steady state voltage.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

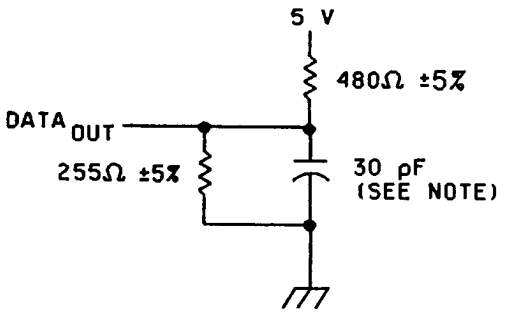
Device types	All	
Case outlines	X, Z, U, T, M, and N	Y
Terminal numbers	Terminal symbol	
1	A_{14}	NC
2	A_{12}	A_{14}
3	A_7	A_{12}
4	A_6	A_7
5	A_5	A_6
6	A_4	A_5
7	A_3	A_4
8	A_2	A_3
9	A_1	A_2
10	A_0	A_1
11	I/O_1	A_0
12	I/O_2	NC
13	I/O_3	I/O_1
14	GND	I/O_2
15	I/O_4	I/O_3
16	I/O_5	GND
17	I/O_6	NC
18	I/O_7	I/O_4
19	I/O_8	I/O_5
20	$\overline{CE}$	I/O_6
21	A_{10}	I/O_7
22	$\overline{OE}$	I/O_8
23	A_{11}	$\overline{CE}$
24	A_9	A_{10}
25	A_8	$\overline{OE}$
26	A_{13}	NC
27	$\overline{WE}$	A_{11}
28	V_{CC}	A_9
29	---	A_8
30	---	A_{13}
31	---	$\overline{WE}$
32	---	V_{CC}

NC = No connection

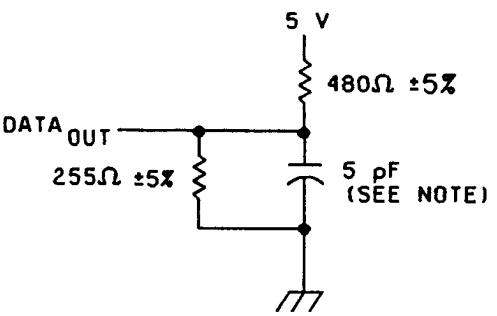
FIGURE 1. Terminal connections.

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Function
H	X	X	High Z	Standby (I_{CC2})
$\geq V_{CC}$ -0.2 V	X	X	High Z	Standby (I_{CC3})
L	H	H	High Z	Output disable
L	H	L	Data out	Read
L	L	X	Data in	Write

FIGURE 2. Truth table.



CIRCUIT A
OUTPUT LOAD



CIRCUIT B
(FOR t_{OLQX}, t_{ELQX}, t_{OHQZ}, t_{WLQZ}, t_{EHQZ}, t_{WHQX})

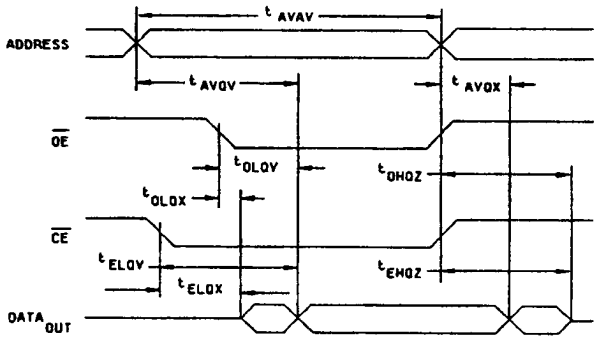
NOTE: Including scope and jig.
(minimum values)

AC test conditions

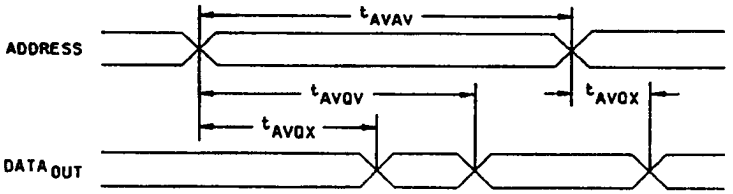
Input pulse levels	GND to 3.0 V
Input rise fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit.

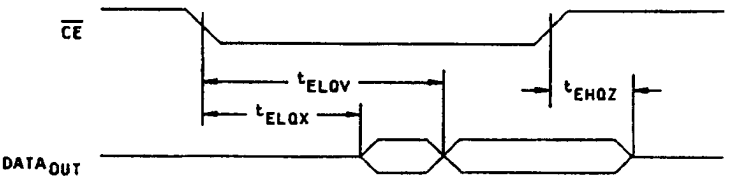
Timing waveform of read cycle number 1 (see note 1)



Timing waveform of read cycle number 2 (see notes 1, 2, and 4)



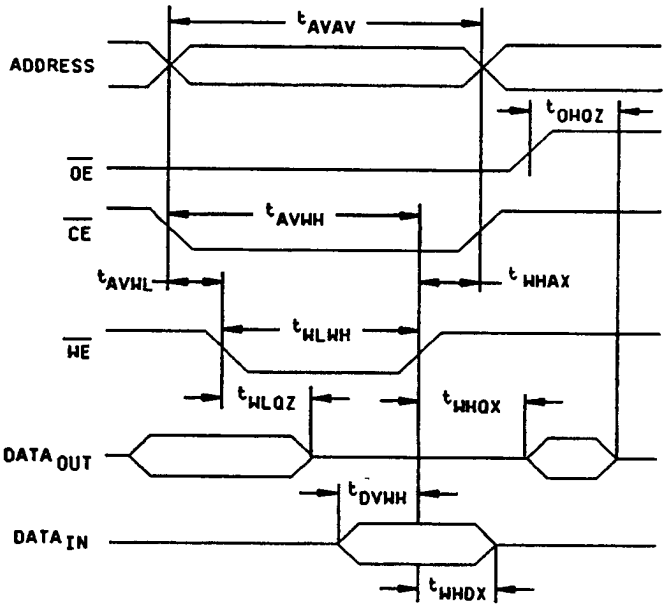
Timing waveform of read cycle number 3 (see notes 1, 3, and 4)



NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected. $\overline{CE} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±500 mV from steady state with 5 pF load (including scope and jig).

FIGURE 4. Timing waveforms.

Timing waveform of write cycle number 1 ($\overline{WE}$ controlled timing) (see notes 1, 2, 3, 6, and 7)



Timing waveform of write cycle number 2 ($\overline{CE}$ controlled timing) (see notes 1, 2, 3, and 5)

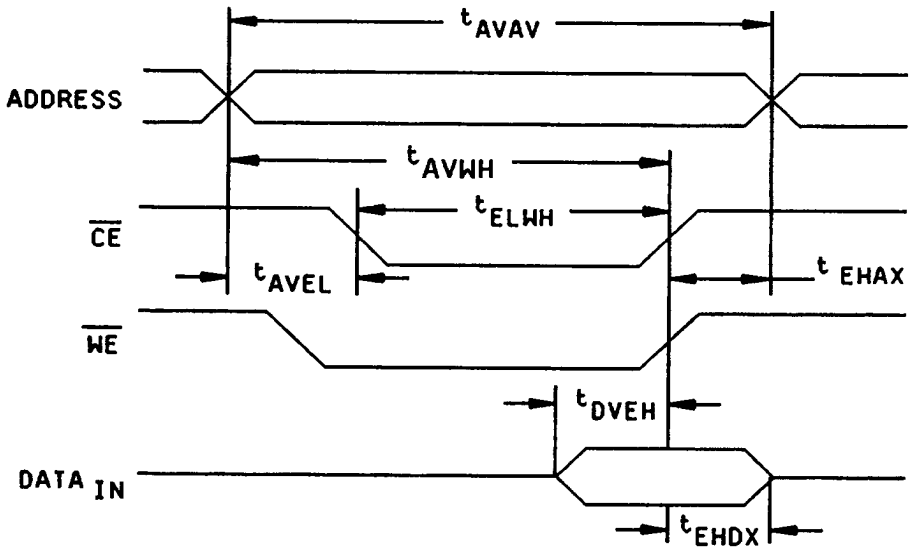


FIGURE 4. Timing waveforms - Continued.

NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{ELWH} or t_{WLWH}) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WHAX} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500 mV from steady state with a 5 pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WLWH} or (t_{WLQZ} + t_{DVWH}) to allow the I/O drivers to turn off and data to be placed on the bus for required t_{DVWH}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, This requirement does not apply and the write pulse can be as short as the specified t_{WLWH}.

FIGURE 4. Timing waveforms - Continued.

Low V_{CC} retention waveform

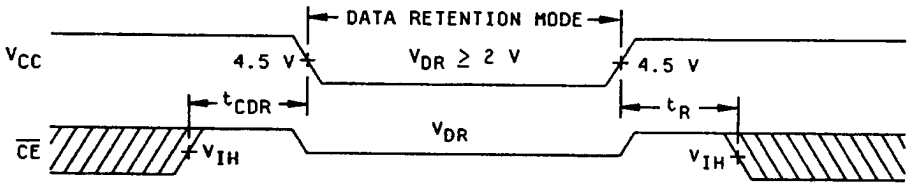


FIGURE 4. Timing waveforms - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7***, 8***, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8

* PDA applies to subgroup 1 and 7.
** See 4.3.1c.
*** See 4.3.1d.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_O measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.