General-purpose Operational Amplifier/Comparator

Low Voltage CMOS Operational Amplifier

BU7261G,BU7261SG, BU7241G,BU7241SG, BU7262F/FVM,BU7262S F/FVM, BU7242F/FVM,BU7242S F/FVM

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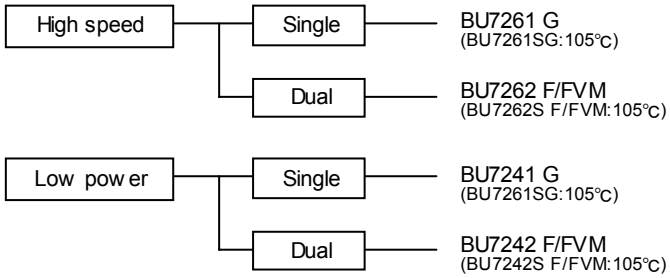
● Description

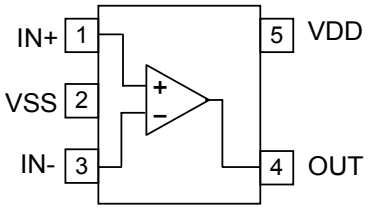
CMOS op-amp BU7261/BU7241 family and BU7262/BU7242 family are input and output full swing op-amp. These ICs integrate one op-amp or two independent op-amps and phase compensation capacitor on a single chip.
The features of these ICs are low operating supply Voltage +1.8V to +5.5V(single supply) and low supply current, extremely low input bias current.

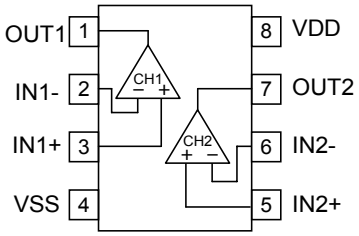


● Features

1) Low operating supply voltage (＋1.8[V]～＋5.5[V])
2) ＋1.8 [V] to＋5.5[V](single supply)
   ±0.9[V] to±2.75[V](split supply)
3) Input and Output full swing
4) Internal phase compensation
5) High slew rate(BU7261 family, BU7262 family)
6) Low supply current(BU7241 family, BU7242 family)
7) High large signal voltage gain
8) Internal ESD protection
   Human body model (HBM) ±4000[V](Typ.)
9) Wide temperature range
   －40[℃] to＋85[℃]
   (BU7261G,BU7262 family, BU7241G,BU7242 family)
   －40[℃] to＋105[℃]
   (BU7261SG,BU7262S family, BU7241SG,BU7242S family)

● Pin Assignments





SSOP5

BU7261G
BU7261SG
BU7241G
BU7241SG

SOP8

BU7262F
BU7262SF
BU7242F
BU7242SF

MSOP8

BU7262FVM
BU7262SFVM
BU7242FVM
BU7242SFVM

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● Absolute maximum rating (Ta=25[℃])

Parameter	Symbol	Rating		Uni
		BU7261G, BU7262 F/FVM BU7241G, BU7242 F/FVM	BU7261SG, BU7262S F/FVM BU7241SG, BU7242S F/FVM	
Supply Voltage	VDD-VSS	+7		V
Differential Input Voltage(*1)	Vid	VDD−VSS		V
Input Common-mode voltage range	Vicm	(VSS−0.3) to VDD+0.3		V
Operating Temperature	Topr	−40 to+85	−40 to+105	℃
Storage Temperature	Tstg	−55 to+125		℃
Maximum junction Temperature	Tjmax	+125		℃

Note: Absolute maximum rating item indicates the condition which must not be exceeded.
Application of voltage in excess of absolute maximum rating or use out absoluted maximum rated temperature environment may cause deterioration of characteristics.
(*1) The voltage difference between inverting input and non-inverting input is the differential input voltage.
Then input terminal voltage is set to more then VEE.

● Electrical characteristics

○BU7261 series, BU7262series (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

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Parameter	Symbol	Temperature Range	Guaranteed limit						Unit	Condition
			BU7261G BU7261SG			BU7262 F/FVM BU7262S F/FVM				
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage (*2)(*4)	Vio	25℃	-	1	9	-	1	9	mV	VDD=1.8 to 5.5[V], VOUT=VDD/2
		Full range	-	-	10	-	-	10		
Input offset Current (*2)	Iio	25℃	-	1	-	-	1	-	pA	−
Input Bias Current (*2)	Ib	25℃	-	1	-	-	1	-	pA	−
Supply current (*4)	IDD	25℃	-	250	550	-	550	1100	μA	RL=∞ All Op-Amps AV=0[dB],VIN=1.5[V]
		Full range	-	-	600	-	-	1200		
High level output voltage	VOH	25℃	VDD-0.1	-	-	VDD-0.1	-	-	V	RL=10[kΩ]
Low level output voltage	VOL	25℃	-	-	VSS+0.1	-	-	VSS+0.1	V	RL=10[kΩ]
Large single voltage gain	AV	25℃	70	95	-	70	95	-	dB	RL=10[kΩ]
Input common-mode voltage range	Vicm	25℃	0	-	3	0	-	3	V	VDD-VSS=3[V]
Common-mode rejection ratio	CMRR	25℃	45	60	-	45	60	-	dB	−
Power supply rejection ratio	PSRR	25℃	60	80	-	60	80	-	dB	−
Output source current (*3)	IOH	25℃	4	10	-	4	10	-	mA	VDD-0.4[V]
Output sink current (*3)	IOL	25℃	5	12	-	5	12	-	mA	VSS+0.4[V]
Slew rate	SR	25℃	-	1.1	-	-	1.1	-	V/μs	CL=25[pF]
Gain bandwidth product	FT	25℃	-	2	-	-	2	-	MHz	CL=25[pF], AV=40[dB]
Phase margin	θ	25℃	-	50°	-	-	50°	-	−	CL=25[pF], AV=40[dB]
Total harmonic distortion	THD	25℃	-	0.05	-	-	0.05	-	%	VOUT=1[Vp-p],f=1[kHz]
Channel separation	CS	25℃	-	-	-	-	100	-	dB	Av=40[dB]

(*2) Absolute value
(*3) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal shot circuits are continuously output, the output current is reduced to climb to the temperature inside IC.
(*4) Full range： BU7261, BU7262：Ta=-40[℃] to +85[℃] BU7261S, BU7262S：Ta=-40[℃] to +105[℃]

● Electrical characteristics

○BU7241 series, BU7242 series (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature Range	Guaranteed limit						Unit	Condition
			BU7241G BU7241SG			BU7242F/FVM BU7242S F/FVM				
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage (*5)(*7)	Vio	25℃	-	1	9	-	1	9	mV	VDD=1.8 to 5.5[V], VOUT=VDD/2
		Full range	-	-	10	-	-	10		
Input offset Current (*5)	Iio	25℃	-	1	-	-	1	-	pA	−
Input Bias Current (*5)	Ib	25℃	-	1	-	-	1	-	pA	−
Supply current (*7)	IDD	25℃	-	70	150	-	180	360	μA	RL=∞ All Op-Amps AV=0[dB],VIN=1.5[V]
		Full range	-	-	250	-	-	600		
High level output voltage	VOH	25℃	VDD-0.1	-	-	VDD-0.1	-	-	V	RL=10[kΩ]
Low level output voltage	VOL	25℃	-	-	VSS+0.1	-	-	VSS+0.1	V	RL=10[kΩ]
Large single voltage gain	AV	25℃	70	95	-	70	95	-	dB	RL=10[kΩ]
Input common-mode voltage range	Vicm	25℃	0	-	3	0	-	3	V	VDD-VSS=3[V]
Common-mode rejection ratio	CMRR	25℃	45	60	-	45	60	-	dB	−
Power supply rejection ratio	PSRR	25℃	60	80	-	60	80	-	dB	−
Output source current (*6)	IOH	25℃	4	10	-	4	10	-	mA	VDD-0.4[V]
Output sink current (*6)	IOL	25℃	5	12	-	5	12	-	mA	VSS+0.4[V]
Slew rate	SR	25℃	-	0.4	-	-	0.4	-	V/μs	CL=25[pF]
Gain bandwidth product	FT	25℃	-	0.9	-	-	0.9	-	MHz	CL=25[pF], AV=40[dB]
Phase margin	θ	25℃	-	50°	-	-	50°	-	−	CL=25[pF], AV=40[dB]
Total harmonic distortion	THD	25℃	-	0.05	-	-	0.05	-	%	VOUT=1[Vp-p],f=1[kHz]
Channel separation	CS	25℃	-	-	-	-	100	-	dB	Av=40[dB]

(*5) Absolute value
(*6) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal shot circuits are continuously output, the output current is reduced to climb to the temperature inside IC.
(*7) Full range： BU7241, BU7242：Ta=-40[℃] to +85[℃] BU7241S, BU7242S：Ta=-40[℃] to +105[℃]

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●Example of electrical characteristics

○BU7261 family

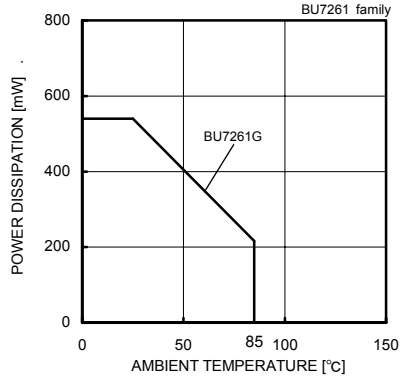

Fig.1
Derating curve

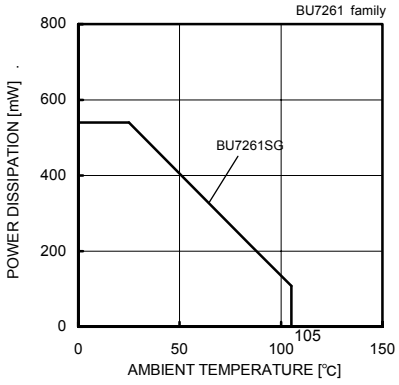

Fig.2
Derating curve

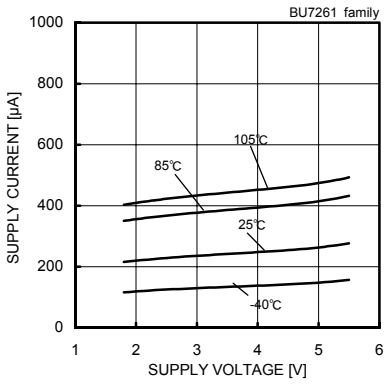

Fig.3
Supply Current – Supply Voltage

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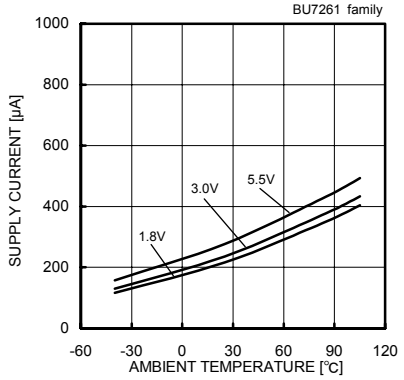

Fig.4
Supply Current – Ambient Temperature

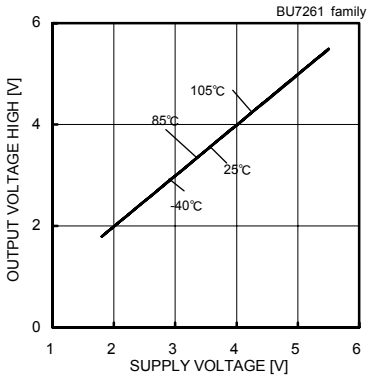

Fig.5
Output Voltage High – Supply Voltage
(RL=10[kΩ])

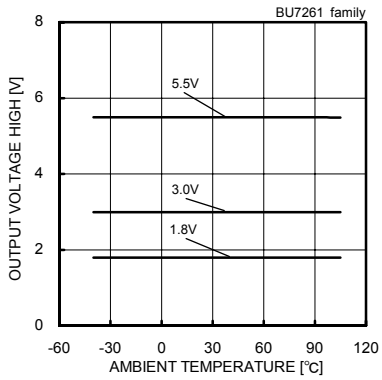

Fig.6
Output Voltage – Ambient Temperature
(RL=10[kΩ])

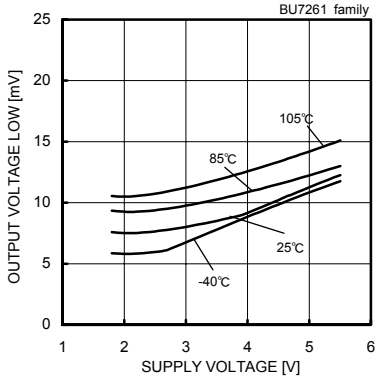

Fig.7
Output Voltage – Supply Voltage
(RL=10[kΩ])

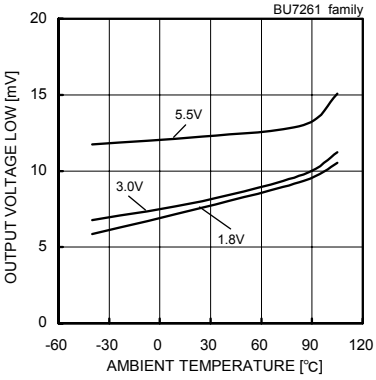

Fig.8
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

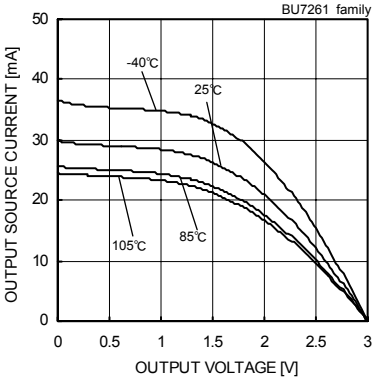

Fig.9
Output Source Current – Output Voltage
(VDD=3.0[V])

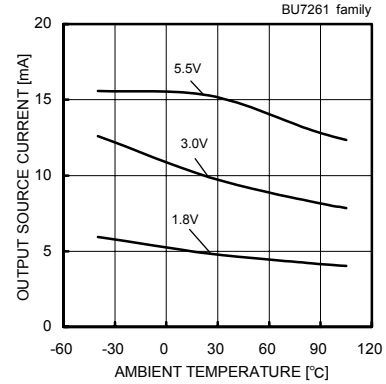

Fig.10
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

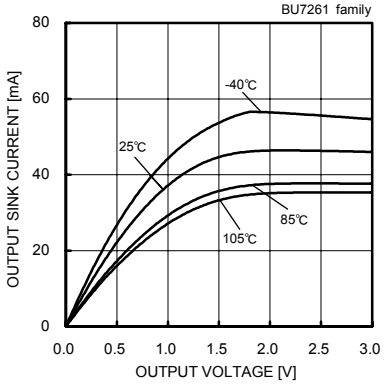

Fig.11
Output Sink Current – Output Voltage
(VDD=3[V])

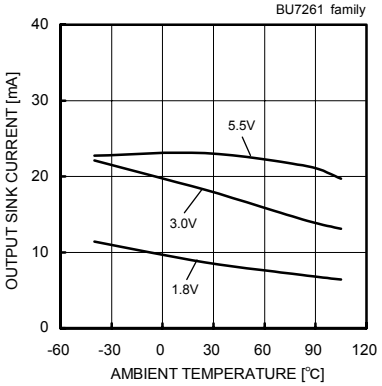

Fig.12
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*) The above date is ability value of sample, it is not guaranteed. BU7261G : −40[℃] to+85[℃] BU7261SG : −40[℃] to+105[℃]

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○BU7261 family

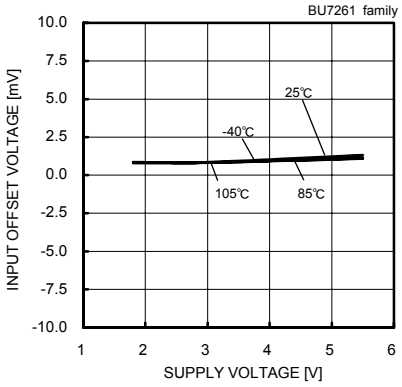

Fig.13
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=1.5[V])

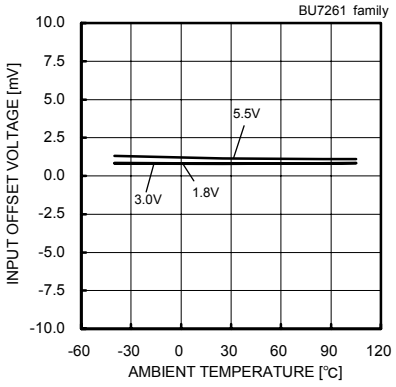

Fig.14
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=1.5[V])

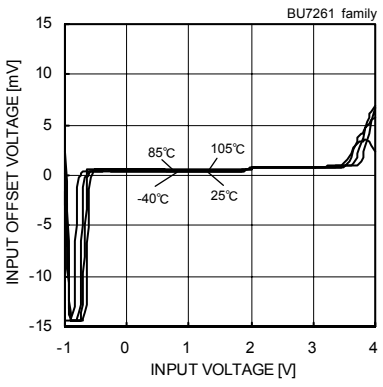

Fig.15
Input Offset Voltage – Input Voltage
(VDD=3[V])

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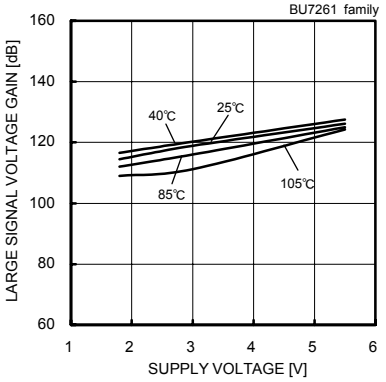

Fig.16
Large Signal Voltage Gain – Supply Voltage

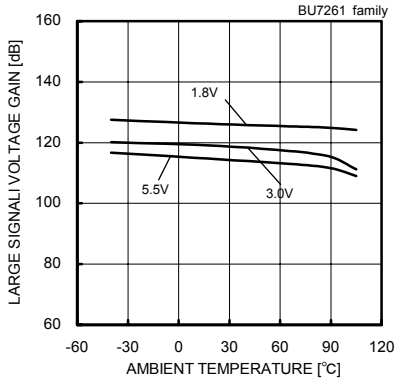

Fig.17
Large Signal Voltage Gain – Ambient Temperature

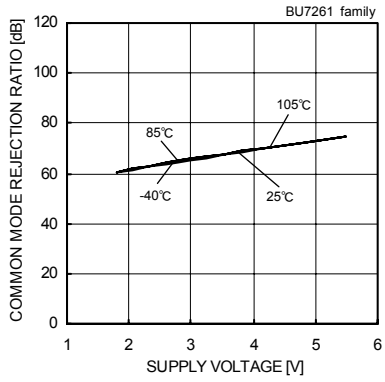

Fig.18
Common Mode Rejection Ratio – Supply Voltage
(VDD=3[V])

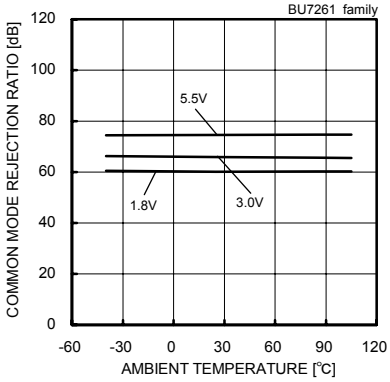

Fig.19
Common Mode Rejection Ratio
– Ambient Temperature
(VDD=3[V])

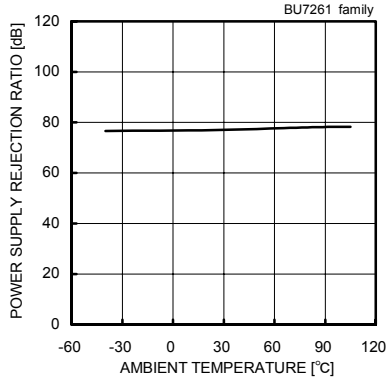

Fig.20
Power Supply Rejection Ratio
– Ambient Temperature

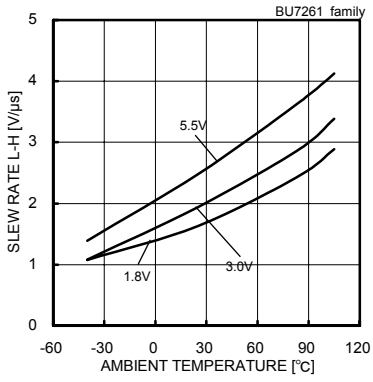

Fig.21
Slew Rate L-H – Ambient Temperature

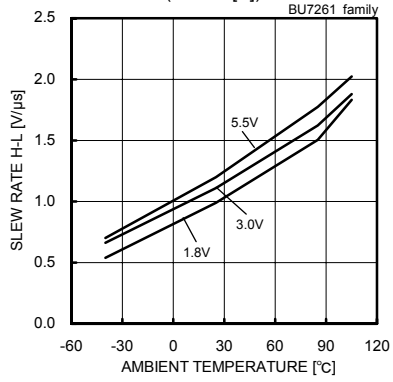

Fig.22
Slew Rate H-L – Ambient Temperature

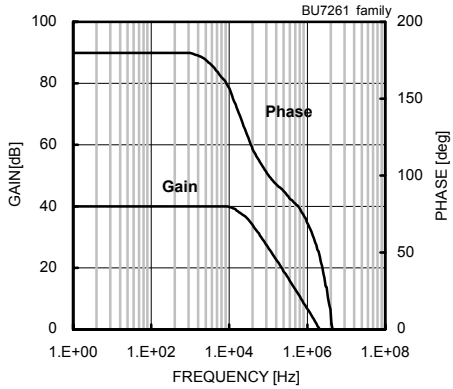

Fig.23
Gain - Frequency

(*) The above date is ability value of sample, it is not guaranteed. BU7261G : −40[℃] to+85[℃] BU7261SG : −40[℃] to+105[℃]

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○BU7262 family

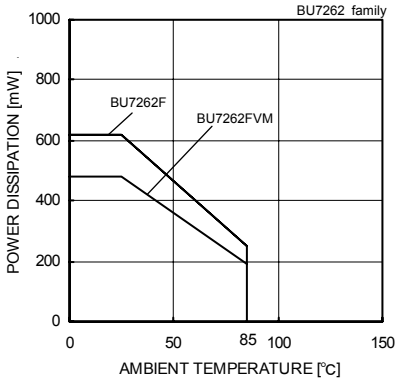

Fig.1
Derating curve

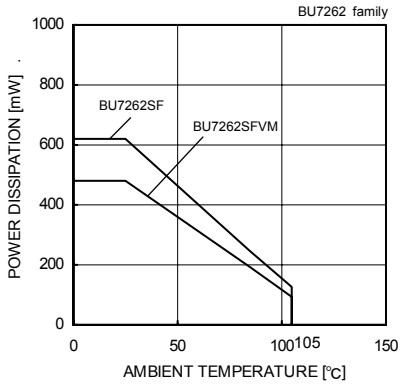

Fig.2
Derating curve

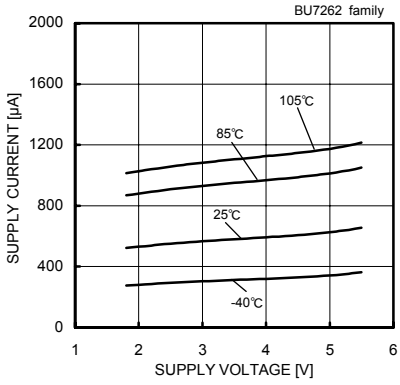

Fig.3
Supply Current – Supply Voltage

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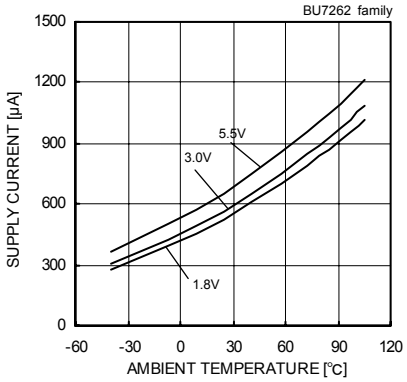

Fig.4
Supply Current – Ambient Temperature

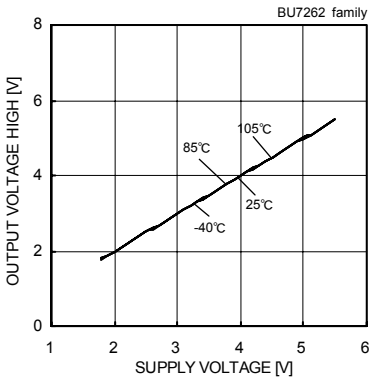

Fig.5
Output Voltage High – Supply Voltage
(RL=10[kΩ])

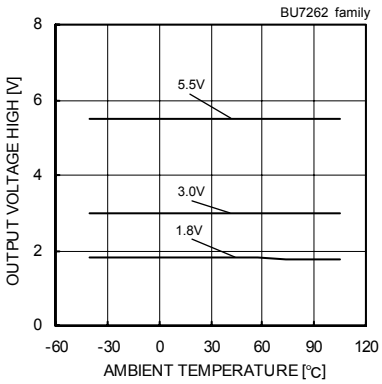

Fig.6
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

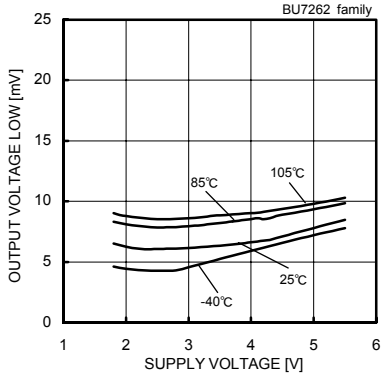

Fig.7
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

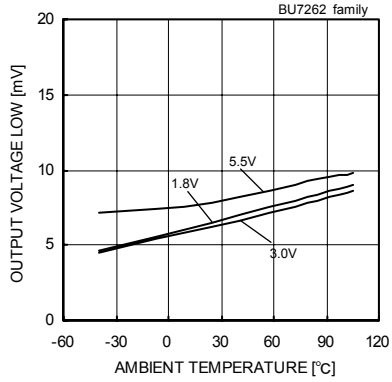

Fig.8
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

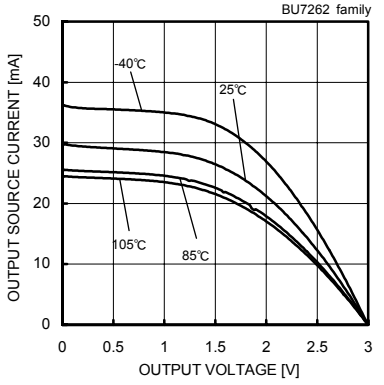

Fig.9
Output Source Current – Output Voltage
(VDD=3.0[V])

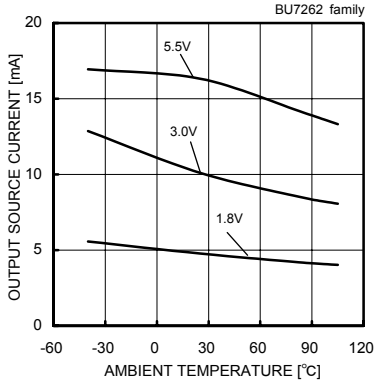

Fig.10
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4V)

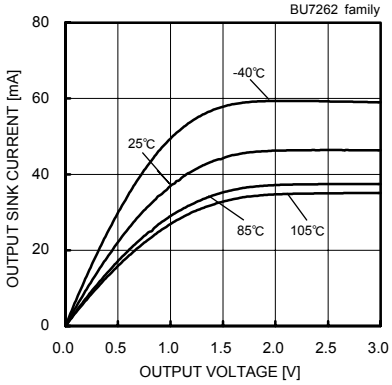

Fig.11
Output Sink Current-Output Voltage
(VDD=3[V])

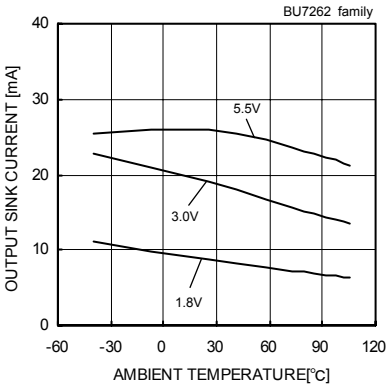

Fig.12
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*) The above date is ability value of sample, it is not guaranteed. BU7262 F/FVM : −40[℃] to+85[℃] BU7262S F/FVM : −40[℃] to+105[℃]

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○BU7262 family

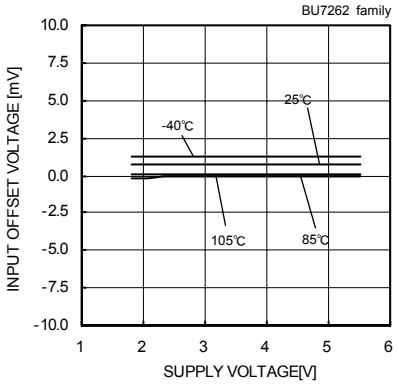

Fig.13
Input Offset Voltage – Supply voltage
(Vicm=VDD,VOUT=1.5[V])

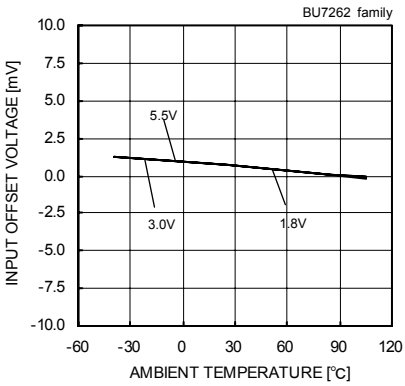

Fig.14
Input Offset Voltage – Ambient Temperature
(Vicm=VDD,VOUT=1.5[V])

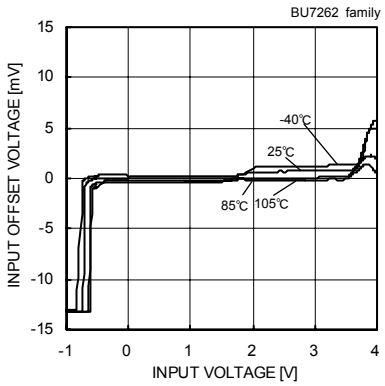

Fig.15
Input Offset Voltage – Input Voltage
(VDD=3[V])

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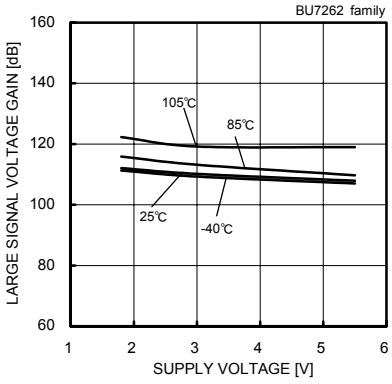

Fig.16
Large Signal Voltage Gain

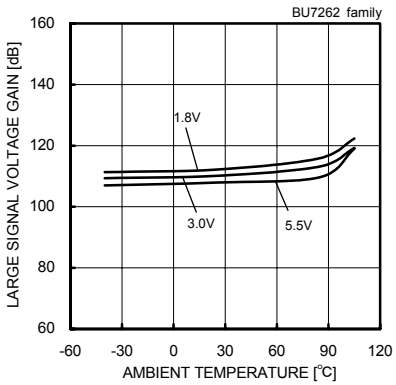

Fig.17
Large Signal Voltage Gain – Ambient Temperature

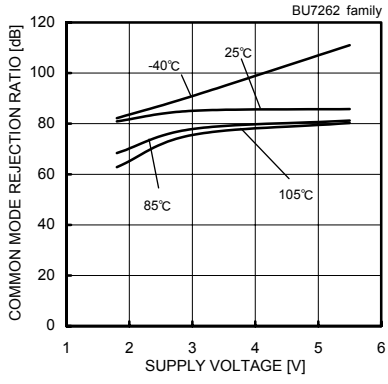

Fig.18
Common Mode Rejection Ratio
– Supply Voltage(VDD=3[V])

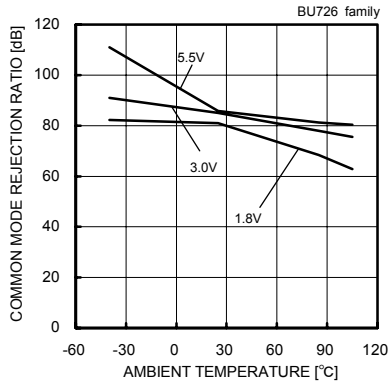

Fig.19
Common Mode Rejection ratio –
Ambient Temperature (VDD=3[V])

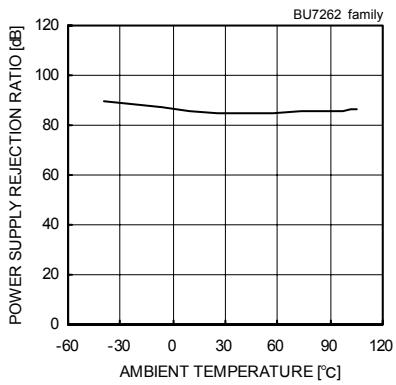

Fig.20
Power Supply Rejection Ratio –
Ambient temperature

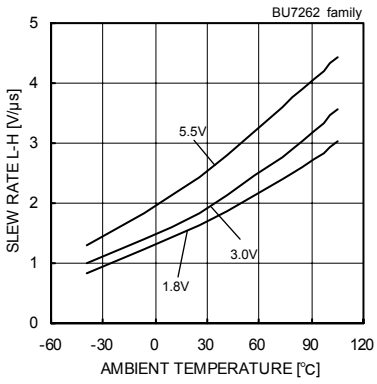

Fig.21
Slew Rate L-H – Ambient Temperature

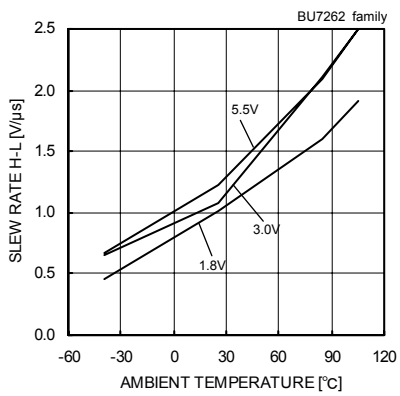

Fig.22
Slew Rate H-L – Ambient Temperature

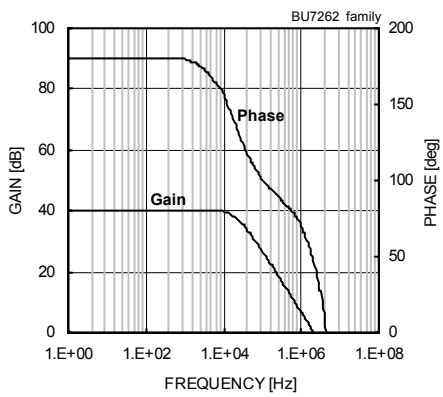

Fig.23
Gain - Frequency

(*) The above date is ability value of sample, it is not guaranteed. BU7262 F/FVM : −40[℃] to+85[℃] BU7262S F/FVM : −40[℃] to+105[℃]

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○BU7241 family

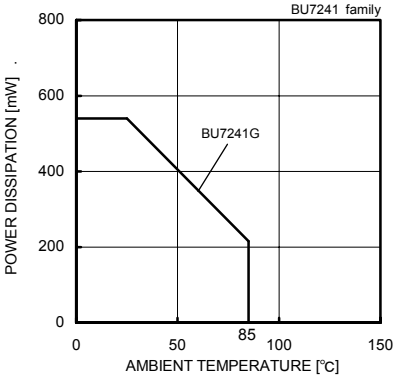

Fig.1
Derating curve

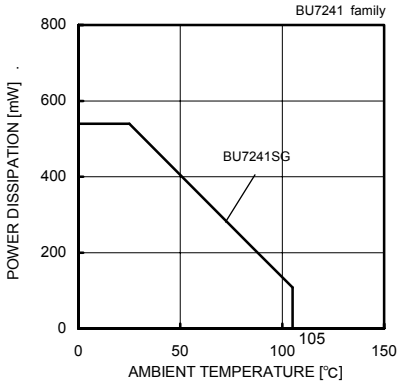

Fig.2
Derating curve

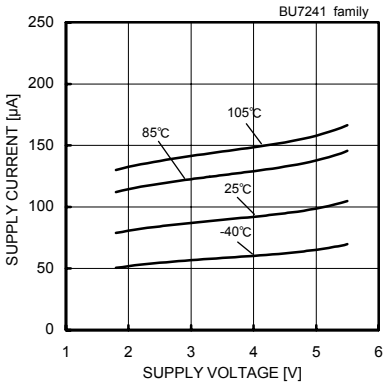

Fig.3
Supply Current – Supply Voltage

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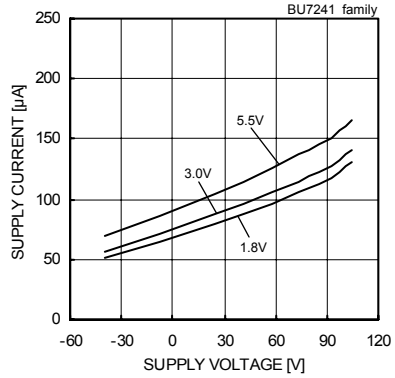

Fig.4
Supply Current – Supply Voltage

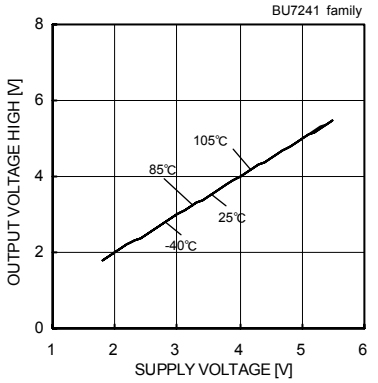

Fig.5
Output Voltage High – Supply Voltage
(RL=10[kΩ])

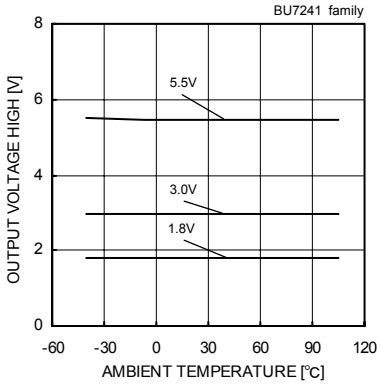

Fig.6
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

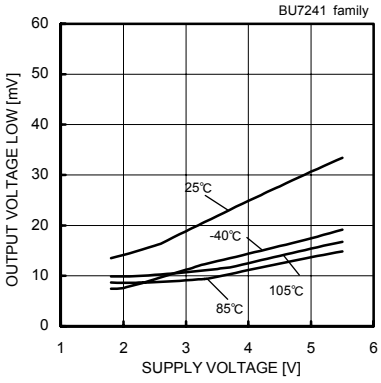

Fig.7
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

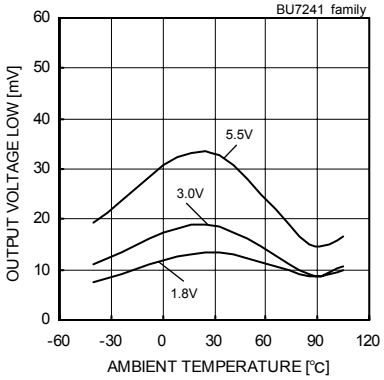

Fig.8
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

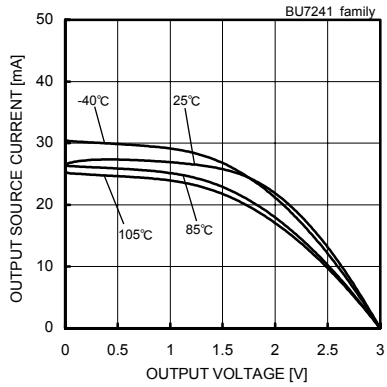

Fig.9
Output Source Current – Output Voltage
(VDD=3.0[V])

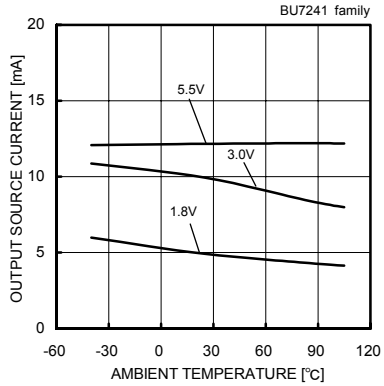

Fig.10
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

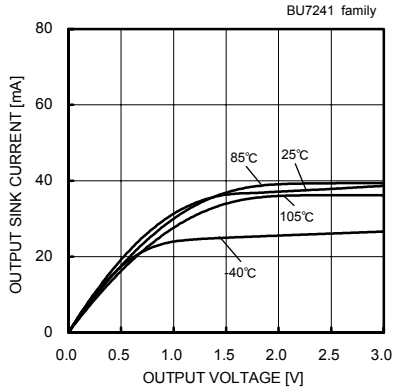

Fig.11
Output Sink Current – Output Voltage
(VDD=3[V])

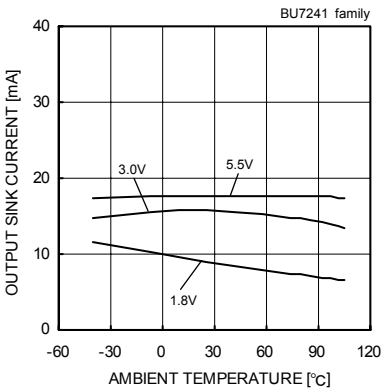

Fig.12
Output Sink current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*) The above date is ability value of sample, it is not guaranteed. BU7241G : −40[℃] to+85[℃] BU7241SG : −40[℃] to+105[℃]

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○BU7241 family

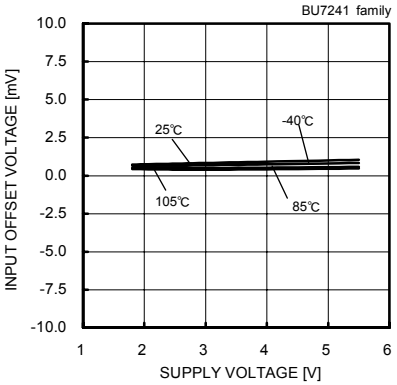

Fig.13
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=1.5[V])

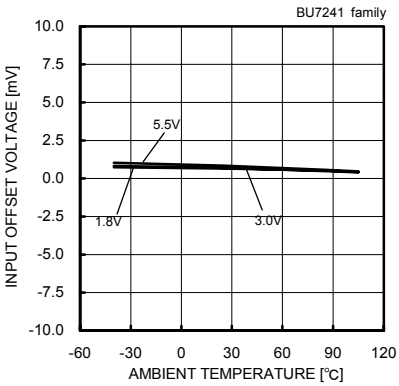

Fig.14
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=1.5[V])

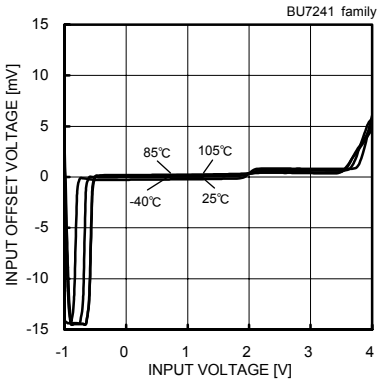

Fig.15
Input Offset Voltage – Input Voltage
(VDD=3[V])

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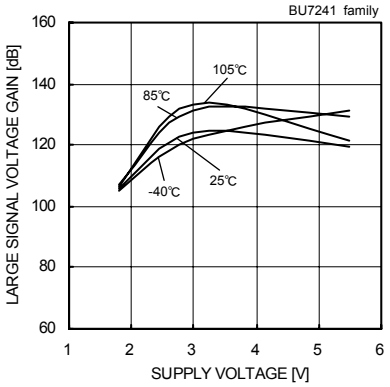

Fig.16
Large Signal Voltage Gain
– Supply Voltage

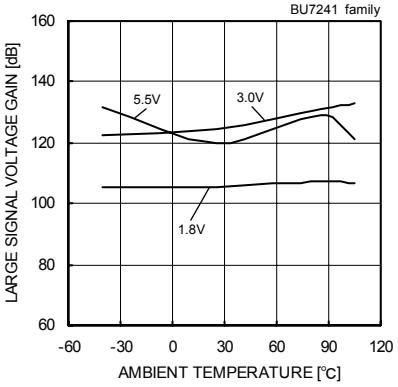

Fig.17
Large Signal Voltage Gain
– Ambient Temperature

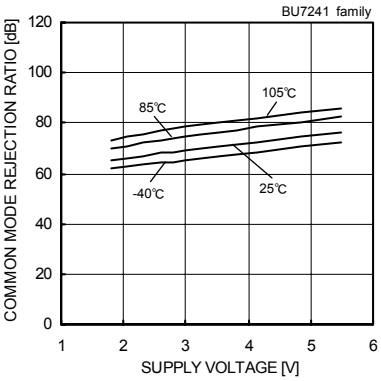

Fig.18
Common Mode Rejection Ratio
– Supply Voltage (VDD=3[V])

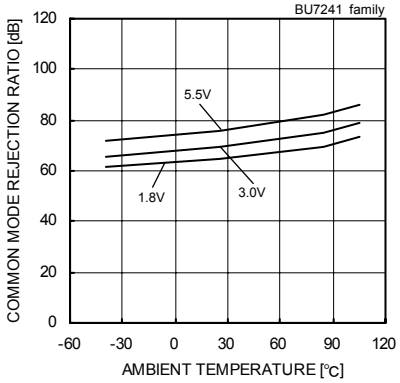

Fig.19
Common Mode Rejection Ratio
(VDD=3[V])

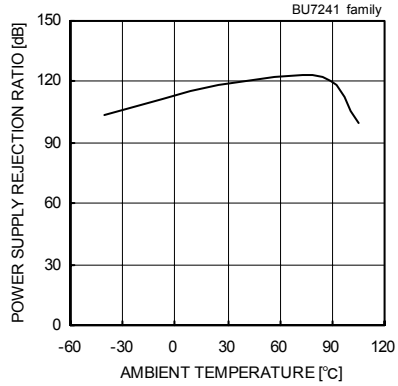

Fig.20
Power Supply Rejection Ratio –
Ambient Temperature

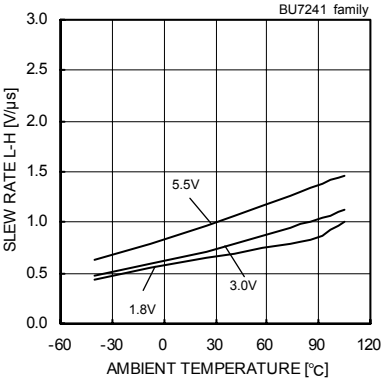

Fig.21
Slew Rate L-H – Ambient Temperature

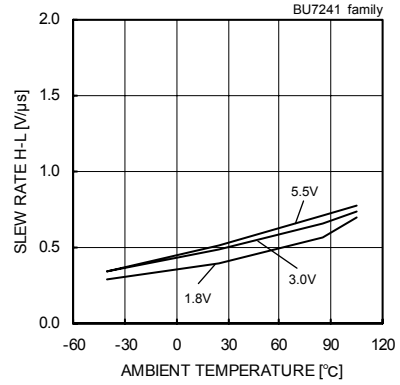

Fig.22
Slew Rate H-L – Ambient Temperature

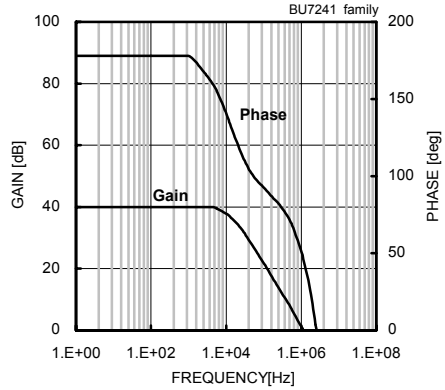

Fig.23
Gain - Frequency

(*) The above date is ability value of sample, it is not guaranteed. BU7241G : −40[℃] to+85[℃] BU7241SG : −40[℃] to+105[℃]

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○BU7242 family

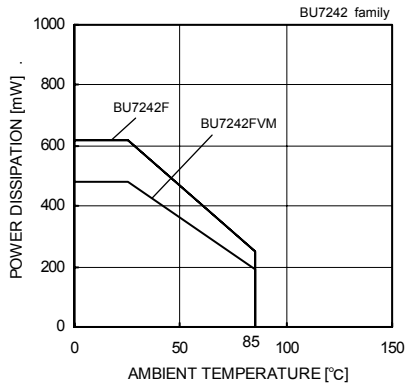

Fig.1
Derating curve

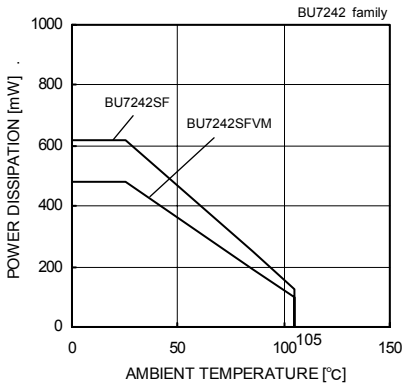

Fig.2
Derating curve

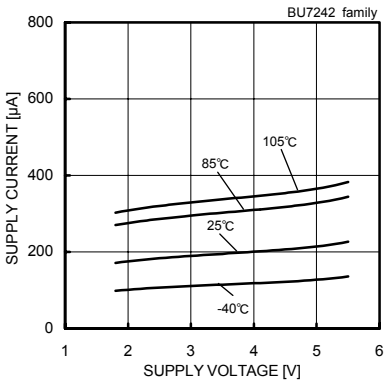

Fig.3
Supply Current – Supply Voltage

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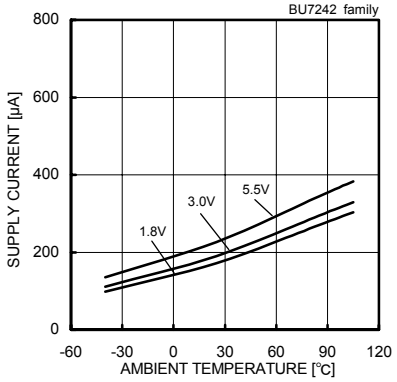

Fig.4
Supply Current – Ambient Temperature

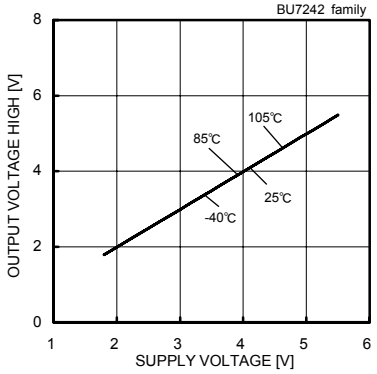

Fig.5
Output Voltage High – Supply Voltage
(RL=10[kΩ])

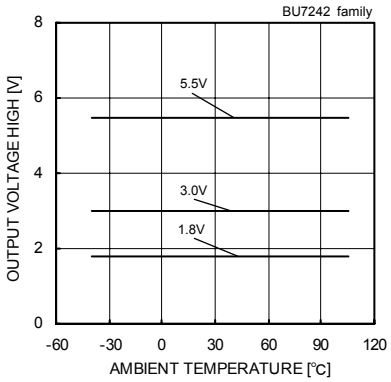

Fig.6
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

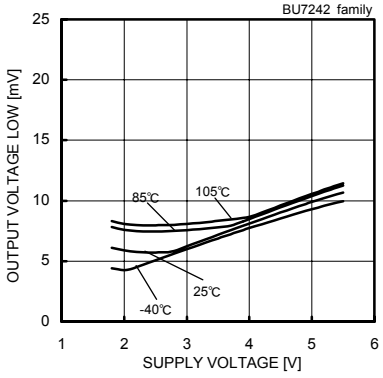

Fig.7
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

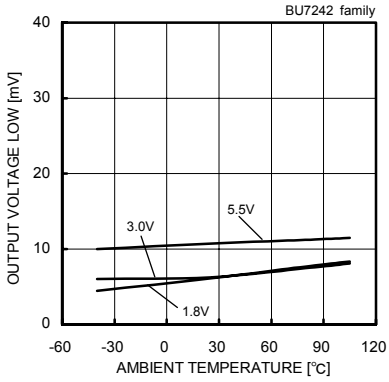

Fig.8
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

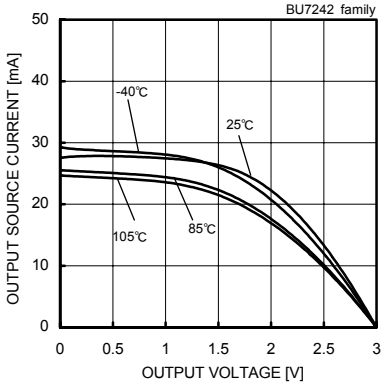

Fig.9
Output Source Current – Output Voltage
(VDD=3.0[V])

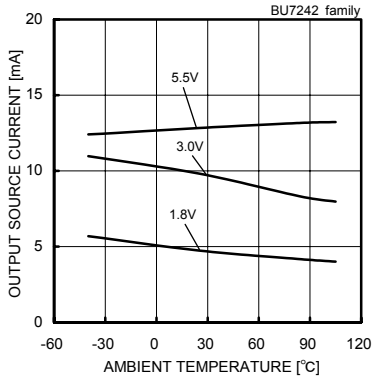

Fig.10
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

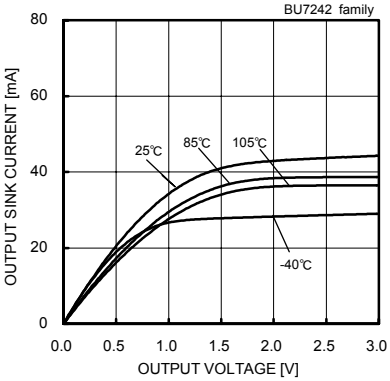

Fig.11
Output Sink Current – Output Voltage
(VDD=3[V])

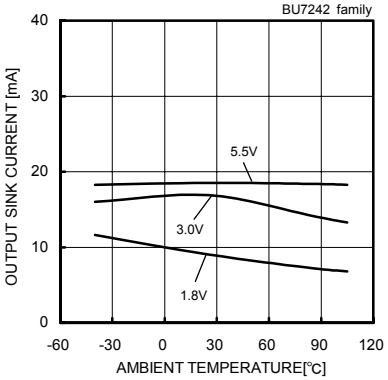

Fig.12
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*) The above date is ability value of sample, it is not guaranteed. BU7242F/FVM : −40[℃] to+85[℃] BU7242SF/FVM : −40[℃] to+105[℃]

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○BU7242 family

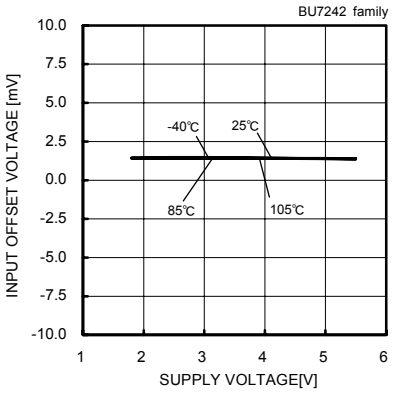

Fig.13
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=1.5[V])

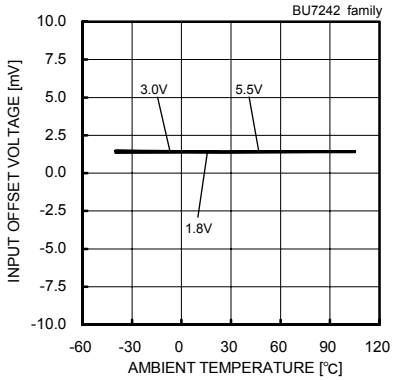

Fig.14
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=1.5[V])

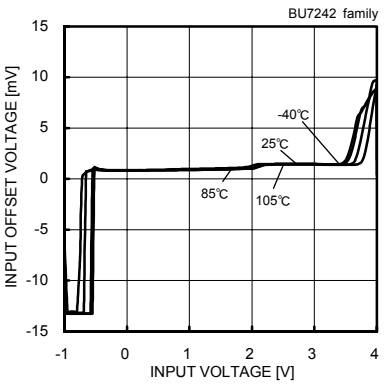

Fig.15
Input Offset Voltage – Input Voltage
(VDD=3[V])

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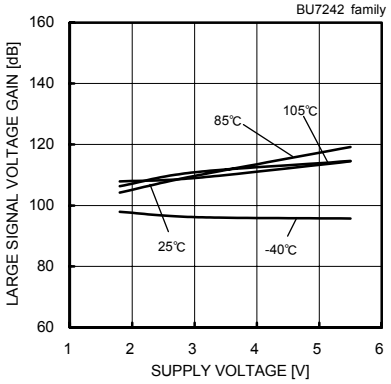

Fig.16
Large Signal Voltage – Supply Voltage

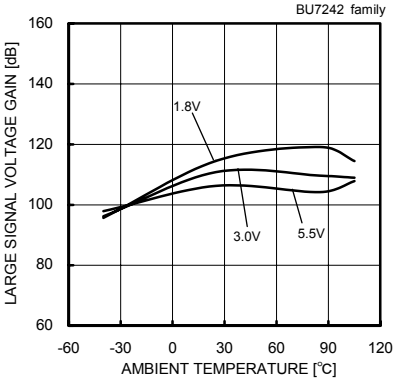

Fig.17
Large Signal Voltage – Ambient Temperature

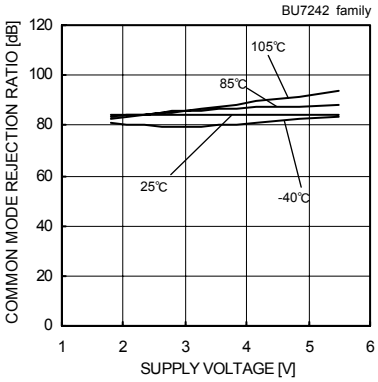

Fig.18
Common Mode Rejection Ratio – Supply Voltage
(VDD=3[V])

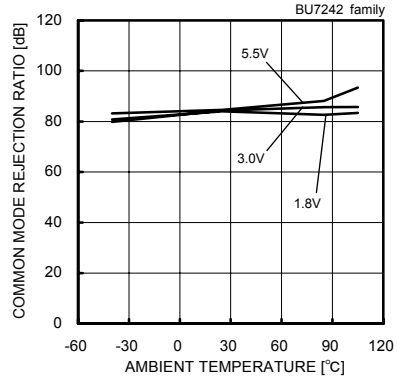

Fig.19
Common Mode Rejection Ratio –
Ambient Temperature(VDD=3[V])

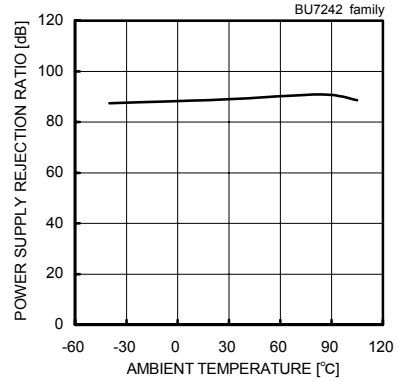

Fig.20
Power Supply Rejection Ratio –
Ambient Temperature

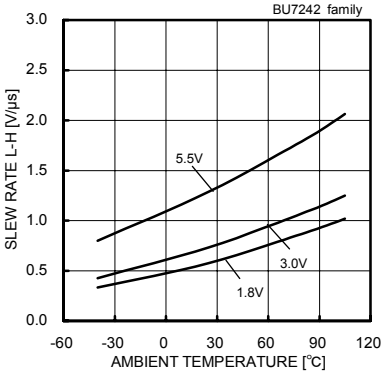

Fig.21
Slew Rate L-H – Ambient Temperature

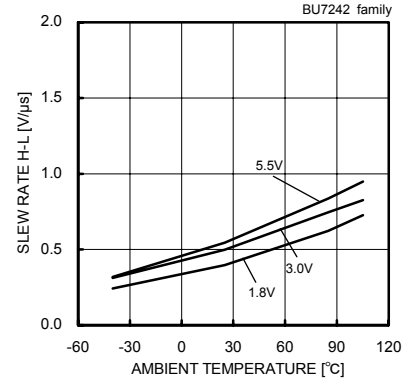

Fig.22
Slew Rate H-L – Ambient Temperature

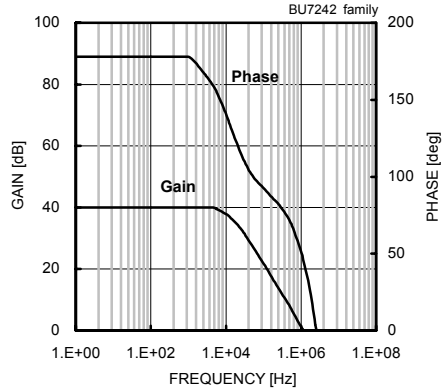

Fig.23
Gain - Frequency

(*) The above date is ability value of sample, it is not guaranteed. BU7242F/FVM : −40[℃] to+85[℃] BU7242SF/FVM : −40[℃] to+105[℃]

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● Schematic diagram

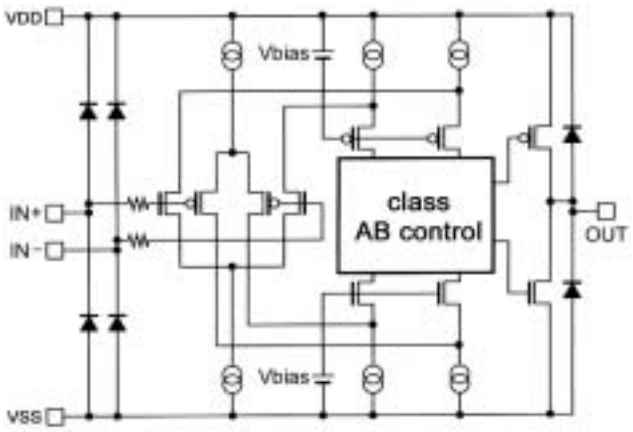

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Fig.1 simplified schematic

● Test circuit1 NULL method

VDD,VSS,EK,Vicm Unit : [V]

Parameter	VF	S1	S2	S3	VDD	VSS	EK	Vicm	Calculation
Input offset voltage	VF1	ON	ON	OFF	3	0	-1.5	3	1
Large signal voltage gain	VF2	ON	ON	ON	3	0	-0.5	1.5	2
	VF3						-2.5		
Common-mode rejection ratio (Input common-mode voltage range)	VF4	ON	ON	OFF	3	0	-1.5	0	3
	VF5							3	
Power supply rejecyion ratio	VF6	ON	ON	OFF	1.8	0	-0.9	0	4
	VF7				5.5				

– Calculation –

1. Input offset Voltage (Vio) $Vio = \frac{|VF1|}{1+Rf/Rs}$ [V]

2. Large signal voltage gain (Av) $Av = 20Log \frac{2\times(1+Rf/Rs)}{|VF2-VF3|}$ [dB]

3. Common-mode rejection ratio (CMRR) $CMRR = 20Log \frac{3\times(1+Rf/Rs)}{|VF4-VF5|}$ [dB]

4. Power supply rejection ratio (PSRR) $PSRR = 20Log \frac{3.7\times(1+Rf/Rs)}{|VF6-VF7|}$ [dB]

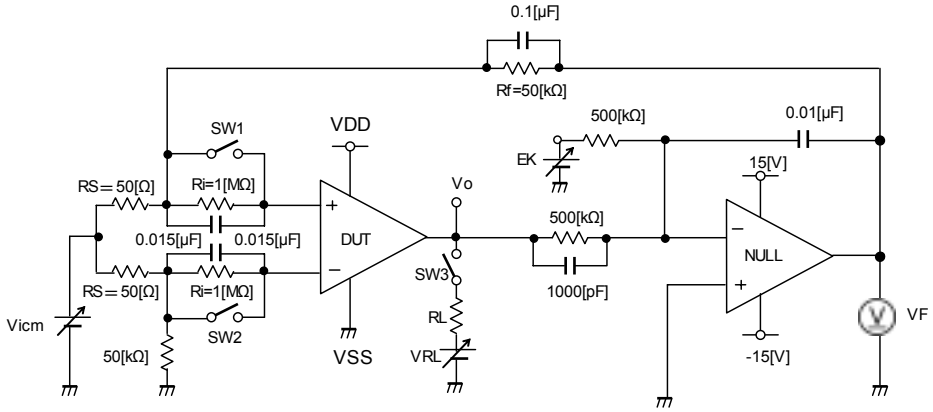

Fig.2 Test Circuit 1 (one channel only)

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● Test circuit2 switch condition

Unit: [V]

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12
Supply current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
maximum output voltage RL=10 [kΩ]	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
output current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
maximum frequency	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

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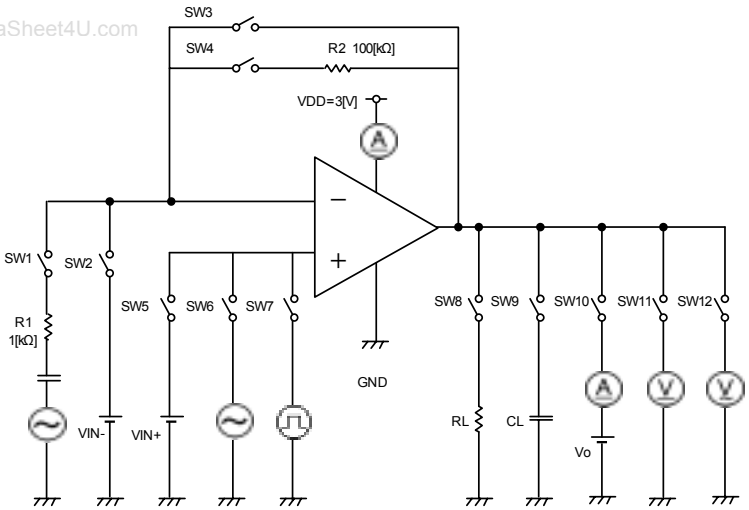

Fig3. Test circuit2 (one channel only)

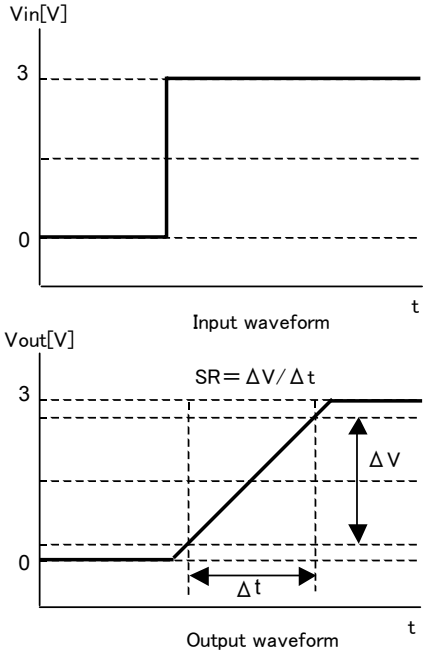

Fig4. Slew rate input output wave

● Test circuit3 Channel separation

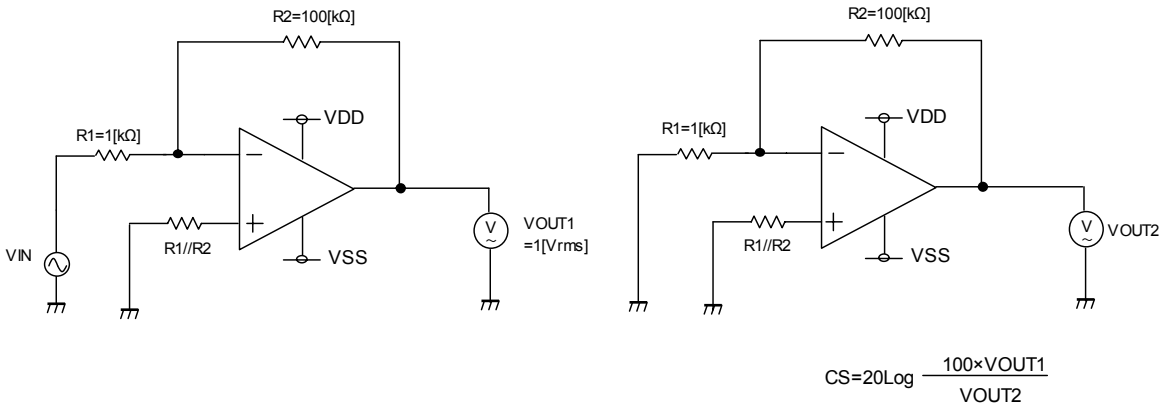

Fig5. Test circuit3

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● Description of electrical characteristics

Described here are the terms of electric characteristics used in this technical note. Items and symbols used are also shown.
Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute Maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of dharacteristics.

1.1 Power supply voltage (VDD/VSS)

Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

1.2 Differential input voltage (Vid)

Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

1.3 Input common-mode voltage range (Vicm)

Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assure normal operation of IC. When normal Operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

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1.4 Power dissipation (Pd)

Indicates the power that can be consumed by specified mounted board at the ambient temperature 25℃(normal temperature). As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature) and thermal resistance of the package

2. **Electrical characteristics item**

2.1 Input offset voltage (Vio)

Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 [V]

2.2 Input offset current (Iio)

Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

2.3 Input bias current (Ib)

Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

2.4 Circuit current (ICC)

Indicates the IC current that flows under specified conditions and no-load steady status.

2.5 High level output voltage / Low level output voltage (VOH/VOL)

Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into high-level output voltage and low-level output voltage. High-level output voltage indicates the upper limit of output voltage. Low-level output voltage indicates the lower limit.

2.6 Large signal voltage gain (AV)

Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
Av = (Output voltage fluctuation) / (Input offset fluctuation)

2.7 Input common-mode voltage range (Vicm)

Indicates the input voltage range where IC operates normally.

2.8 Common-mode rejection ratio (CMRR)

Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of Input common-mode voltage) / (Input offset fluctuation)

2.9 Power supply rejection ratio (PSRR)

Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.
PSRR= (Change of power supply voltage) / (Input offset fluctuation)

2.10 Channel separation (CS)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

2.11 Slew rate (SR)

Indicates the time fluctuation ratio of voltage output when step input signal is applied

2.12 Unity gain frequency (ft)

Indicates a frequency where the voltage gain of Op-Amp is 1.

2.13 Total harmonic distortion + Noise (THD+N)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel

2.14 Input referred noise voltage (Vn)

Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal

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● Derating curve

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25℃(normal temperature).IC is heated when it consumed power, and the temperature of IC ship becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θj-a[℃/W]. The temperature of IC inside the package can be estimated by this thermal resistance. Fig.6 (a) shows the model of thermal resistance of the package. Thermal resistance θja, ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below :

$$\theta ja = (Tj - Ta) / Pd \quad [℃/W] \qquad \cdots\cdots \quad (I)$$

Derating curve in Fig.6 (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient iis determined by thermal resistance θja. Thermal resistance θja depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig7(c)-(f) show a derating curve for an example of BU7261series, BU7262series, BU7241,BU7242series.

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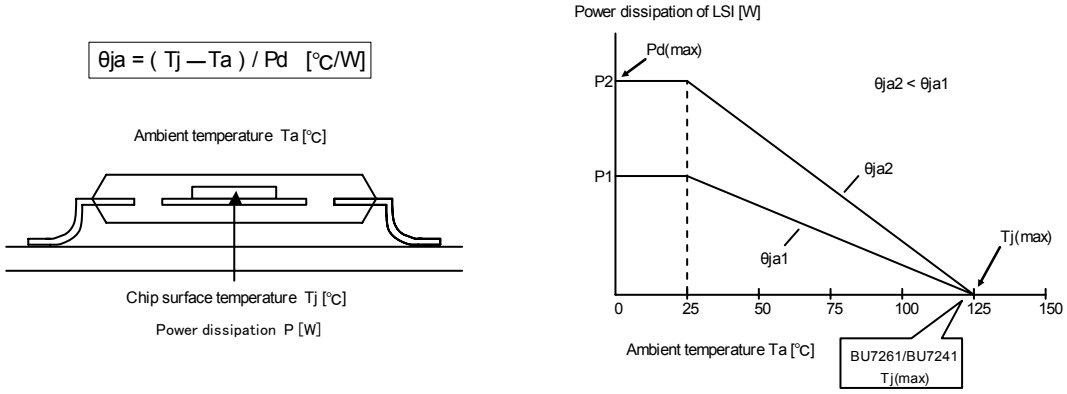
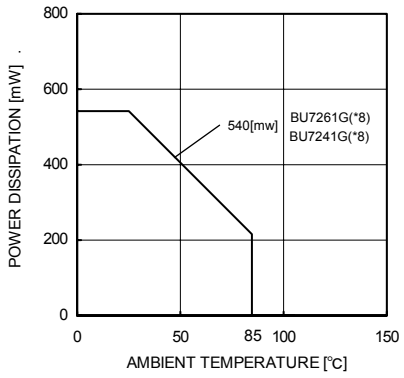
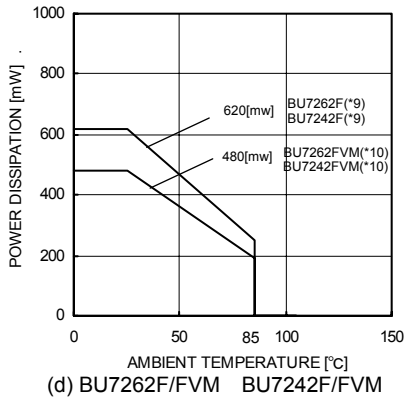


(a) Thermal resistance (b) Derating curve

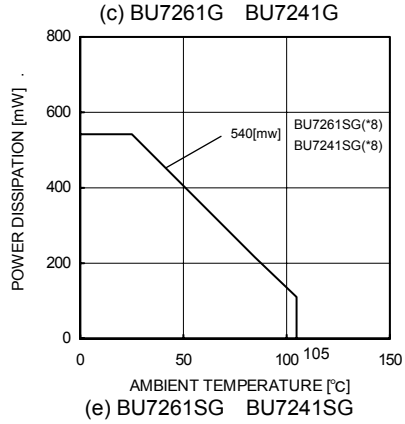
Fig.6 Thermal resistance and derating



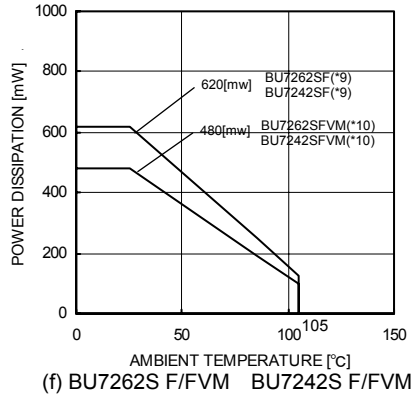
(c) BU7261G BU7241G



(d) BU7262F/FVM BU7242F/FVM



(e) BU7261SG BU7241SG



(f) BU7262S F/FVM BU7242S F/FVM

(*8)	(*9)	(*10)	Unit
5.4	6.2	4.8	[mW/℃]

When using the unit above Ta=25[℃], subtract the value above per degree[℃]. Permissible dissipation is the value when FR4 glass epoxy board 70[mm]×70[mm]×1.6[mm] (cooper foil area below 3[%]) is mounted.

Fig.7 Derating Curve

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● Cautions on use

1) Absolute maximum ratings
Absolute maximum ratings are the values which indicate the limits, within which the given voltage range can be safely charged to the terminal. However, it does not guarantee the circuit operation.

2) Applied voltage to the input terminal
For normal circuit operation of voltage comparator, please input voltage for its input terminal within input common mode voltage VDD+0.3[V].
Then, regardless of power supply voltage,VSS-0.3[V] can be applied to input terminals without deterioration or destruction of its characteristics.

3) Operating power supply (split power supply/single power supply)
The voltage comparator operates if a given level of voltage is applied between VDD and VSS. Therefore, the operational amplifier can be operated under single power supply or split power supply.

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4) Power dissipation (pd)
If the IC is used under excessive power dissipation. An increase in the chip temperature will cause deterioration of the radical characteristics of IC.
For example, reduction of current capability. Take consideration of the effective power dissipation and thermal design with a sufficient margin. Pd is reference to the provided power dissipation curve.

5) Short circuits between pins and incorrect mounting
Short circuits between pins and incorrect mounting when mounting the IC on a printed circuits board, take notice of the direction and positioning of the IC.
If IC is mounted erroneously, It may be damaged. Also, when a foreign object is inserted between output, between output and VDD terminal or VSS terminal which causes short circuit, the IC may be damaged.

6) Using under strong electromagnetic field
Be careful when using the IC under strong electromagnetic field because it may malfunction.

7) Usage of IC
When stress is applied to the IC through warp of the printed circuit board,
The characteristics may fluctuate due to the piezo effect.
Be careful of the warp of the printed circuit board.

8) Testing IC on the set board
When testing IC on the set board, in cases where the capacitor is connected to the low impedance, make sure to discharge per fabrication because there is a possibility that IC may be damaged by stress.
When removing IC from the set board, it is essential to cut supply voltage.
As a countermeasure against the static electricity, observe proper grounding during fabrication process and take due care when carrying and storage it.

9) The IC destruction caused by capacitive load
The transistors in circuits may be damaged when VDD terminal and VSS terminal is shorted with the charged output terminal capacitor.When IC is used as a operational amplifier or as an application circuit, where oscillation is not activated by an output capacitor,the output capacitor must be kept below 0.1[μF] in order to prevent the damage mentioned above.

10) Decupling capacitor
Insert the deculing capacitance between VDD and VSS, for stable operation of operational amplifier.

11) Latch up
Be careful of input vltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up operation. And protect the IC from abnormaly noise

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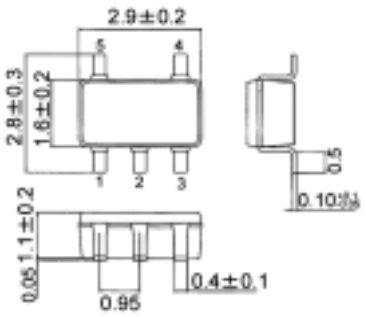
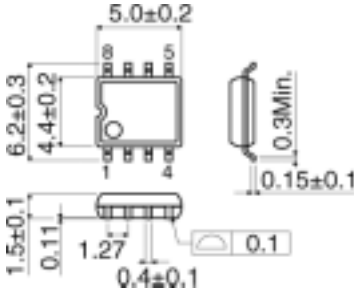
● Dimensions

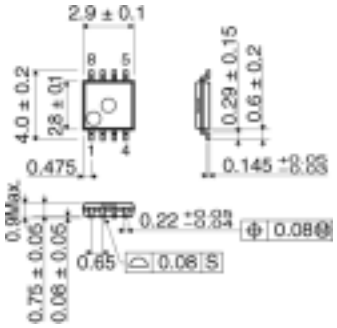
SSOP5



SOP8



MSOP8



● Model number construction

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- Specify the product by the model number when placing an order.
- Make sure of the combinations of items.
- Start with the leftmost space without leaving any empty space between characters.

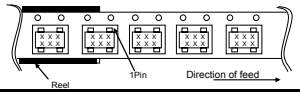
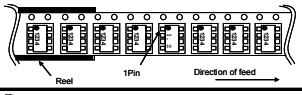
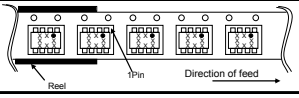
B	U	7	2	6	2	S	F	-	E	2

ROHM product name
- BU7261 BU7261S
- BU7241 BU7241S
- BU7262 BU7262S
- BU7242 BU7242S

Package type
- G : SSOP5
- F : SOP8
- FVM : MSOP8

E2 Embossed tape on reel with pin 1 near far when pulled out
TR Embossed tape on reel with pin 1 near far when pulled out

Packing specification reference

Package	Packing specification name	Quantity	Embossed carrier tape
SSOP5	TR	3000	
SOP8	E2	2500	
MSOP8	TR	3000	

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