SONY CXA1356M/N

1GHz Band PLL IC for Mobile Communications

Preliminary

SONY CORP/COMPONENT PRODS

Description

The CXA1356M/N are frequency synthesizer PLL ICs which have developed for 1GHz mobile communication systems. These ICs have low current consumption, small package and are appropriate for portable sets of cellular units, etc.

CXA1356M
16 pin SOP (Plastic)

CXA1356N
16 pin VSOP (Plastic)

Features

- Low current consumption Icc=13.5mA (Vcc=5.0V)
- Maximum operating frequency 1.8GHz (typ.)
- High input sensitivity
- Ultra small 16-pin VSOP package

Applications

1GHz mobile communication equipment for cellular, etc.

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	7	V
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	300	mW

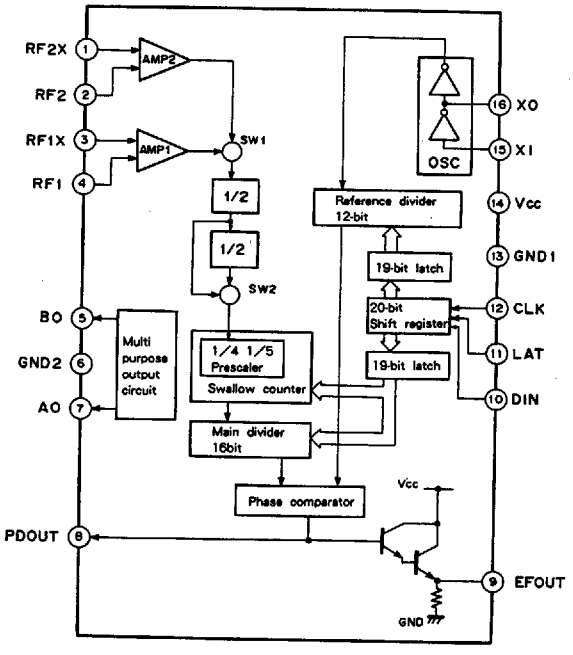
Structure

Bipolar silicon monolithic IC

Operating Conditions

• Supply voltage	Vcc	4.5 to 5.5	V
• Operating temperature	Topr	−35 to +85	°C

Block Diagram and Pin Configuration



Electrical Characteristics

(Ta=25°C, Vcc=5V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption		Icc			13.5		mA
Maximum operating frequency		fiMAX			1800		MHz
DIN CLK LAT	"H" input voltage	VIH			3		V
	"L" input voltage	VIL			2		V
	"H" input current	IIH			0.1		µA
	"L" input current	IIL			–0.1		µA
PD OUT	"H" output current	IOH	VPDOUT=2.5V		–240		µA
	"L" output current	IOL	VPDOUT=2.5V		240		µA

Description of Operation

Control Signal and Control System

The CXA1356M/N is designed to work with a controller which consists of general 4-bit/8-bit microprocessor. It has 3 pins of CLK, LAT and DIN as the control data input pins. As the output pins for control, two pins of AO and BO are also available. A simple, multi-function system can be implemented by taking advantage of these pins.

[1] Control Signal Input Process

The signal input process is comprised of two different data modes, DATA READ mode (normal mode) and DATA CHECK mode.

(a) DATA READ mode (normal mode)

To completely initialize this IC two 20 bit data streams, for a total of 40 bits of data, must be input in this mode. First, make the LAT pin in the LOW state and input data at the DIN pin in synchronization with the clock. The data is read into the shift register one bit at a time with each clock pulse.

After 20 bits of data have been stored in the shift register, the data is latched by making the LAT pin HIGH while holding the CLK pin HIGH. (After the data is latched return the LAT pin to LOW. If the CLK or DIN pins change while the LAT pin is HIGH the stored data may change. So take care.)

As explained in detail below, the data is input into the main divider or reference divider according to the value of C bit. In order to actually use this IC, at first input the 20 bits of input data which represent the reference divider division number, input pin selection, and AO and BO output pin data from the controller by the above sequence. At this time, the last C bit data should be LOW.

Next, set up the main divider data using the same method with 20 bits of input data. At this time, make C bit high. After this the IC is completely initialized. If only the main divider division number need to be changed, by repeating the latter sequence (C bit; HIGH), a new set of data can be stored.

(b) DATA CHECK mode

This mode is provided to verify the correctness of data which is input into the shift register by the controller. Immediately after input data is latched and the LAT pin is returned LOW (remembering to keep CLK HIGH), the data can be output to pin BO one bit at a time with each clock pulse. At that time, the T1 and T2 bits must be held HIGH and LOW respectively in order to output the shift register data to pin BO. T1 and T2 bits are explained in the "Control Data Structure" section.

[2] Control Data Structure

Control data for the CXA1356M/N is constructed a 20-bit data stream. The last two bits represent the function code which recognizes the purpose of the data stream. Selecting the TEST mode is also provided for using this code. As explained later, the first bit of two data stream is the LSB of a binary value of the main divider or reference divider division number.

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(a) Control input data for reference divider (C=LOW)

As this data is called initialization data, whenever the power is turned on this input sequence is mandatory. The data format is assigned below.

←	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	PI3	PI4	PI1	PI2	A	B	T1	C

- R0 to R11 : Reference divider divisor. (Binary value with R0 as LSB).
  In practice, there is an offset component between the actual division number and the input data. Their relationship is as follows.
  (Actual divider division number) = (Input data) +2

- PI1 to PI4 : Input signal pin selection.

PI1	PI2	PI3	PI4	
L	H	L	L	RF1 input
H	H	L	L	RF2 input

- A, B, T1 : Each of the AO and BO pins has two functions which are switched depending on the T1 value. When T1 is LOW, A and B are output to the AO and BO pins respectively.
  When T1 is HIGH, the AO pin outputs the LOCK/UNLOCK state signal of the phase comparator.
  AO pin: H : LOCK
  L : UNLOCK
  The BO pin outputs the shift register contents in the DATA CHECK mode in synchronization with the clock pulse. See [1] (b)

- C : This is a code to determine the latch direction of the input data. Input LOW for this mode.

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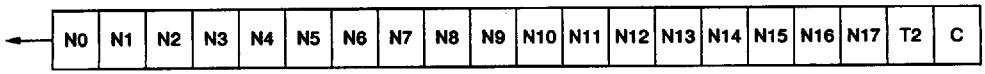
(b) Control input data for main divider (C=HIGH)
Sets up main divider division number data.



• N0 to N17 : Main divider division number (Binary value with N0 as LSB). Main divider has a 1/4 fixed divider circuit at the input, and the actual divisor is shown in the following relationship (PI3=PI4=LOW) :

Range of Division Input Data N	Relation Between N and True Division Number	Range of True Division Number
4 to 262,143	ND=4 • (N+8)	48 to 1,048,604

• T2 : Used to select test mode. Normal user should input a LOW value.
When the main divider output and reference divider output must be checked, make this T2 bit and the T1 bit HIGH and input a LOW for A and B. The AO and BO output pins will output the reference divider output and main divider output respectively.

• C : As described before. Input HIGH for this mode.

Input data				AO output	BO output
T1	T2	A	B		
L	L			A	B
H	L			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output

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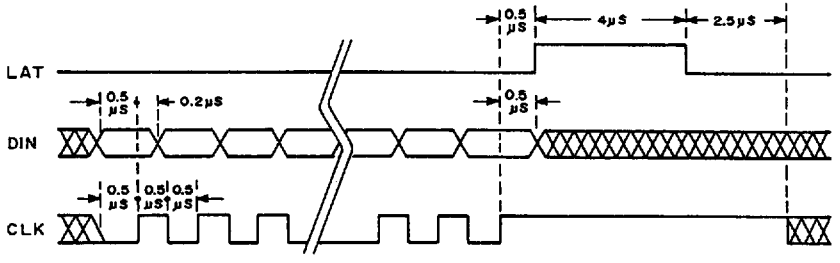
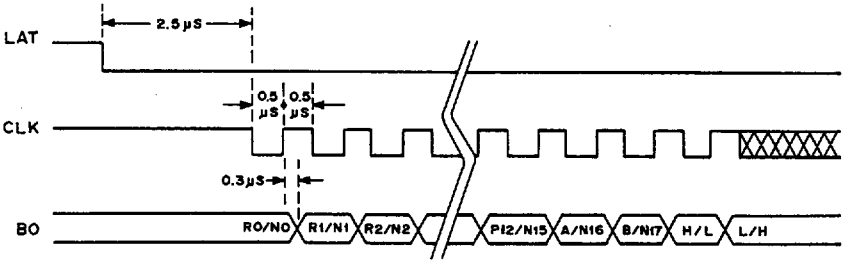
[3] Data Input and Control Signal Timing

(a) DATA READ mode (normal mode)



(b) DATA CHECK mode (shift register data check)



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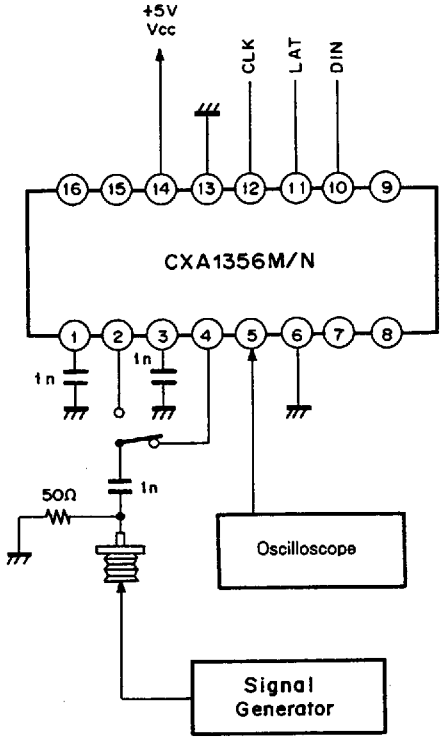
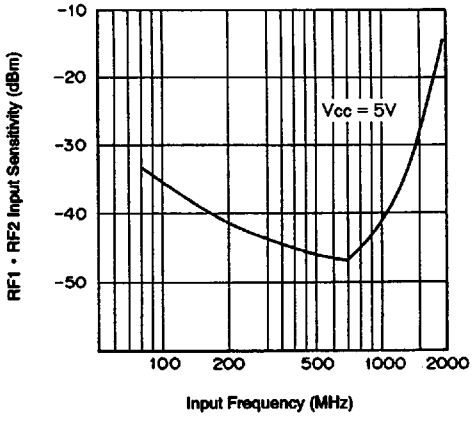
Electrical Characteristic Test Circuit
High Frequency Input Sensitivity Test Circuit



Example of Representative Characteristics

RF1 and RF2 Input Sensitivity vs. Input Frequency Characteristics



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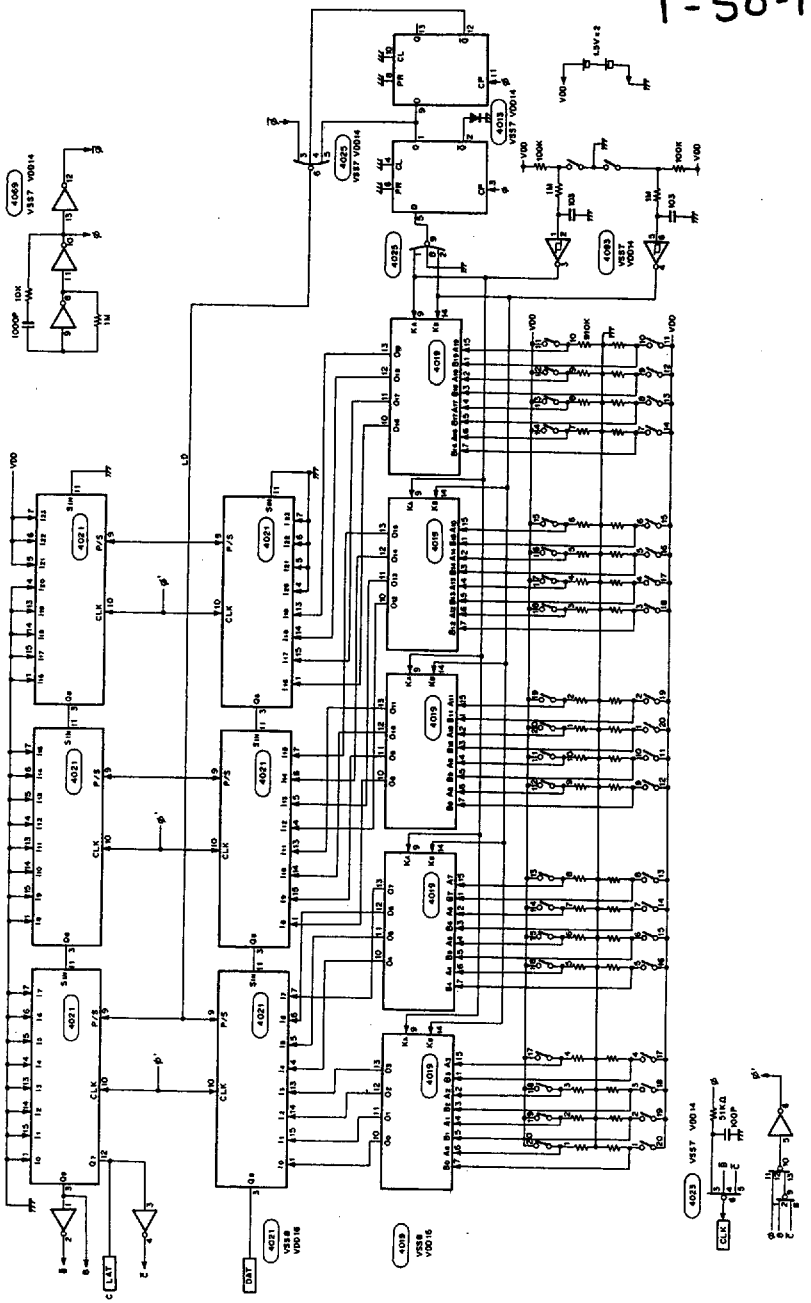

DATA, CLK, LATCH INPUT CIRCUIT

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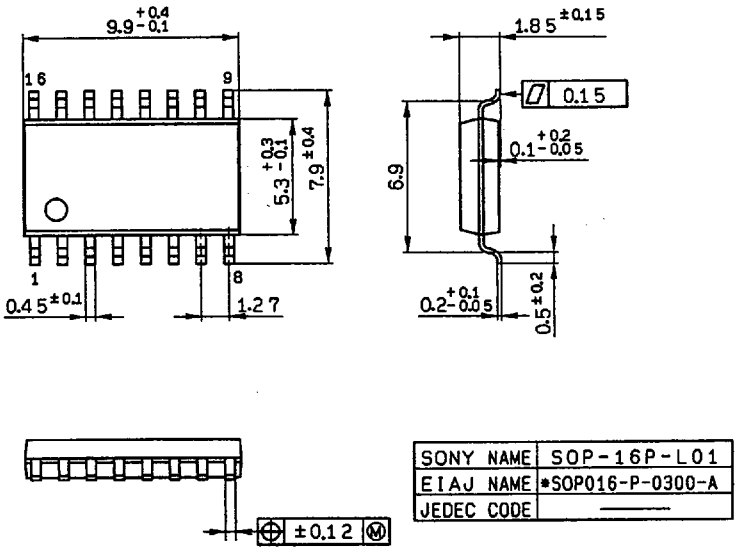
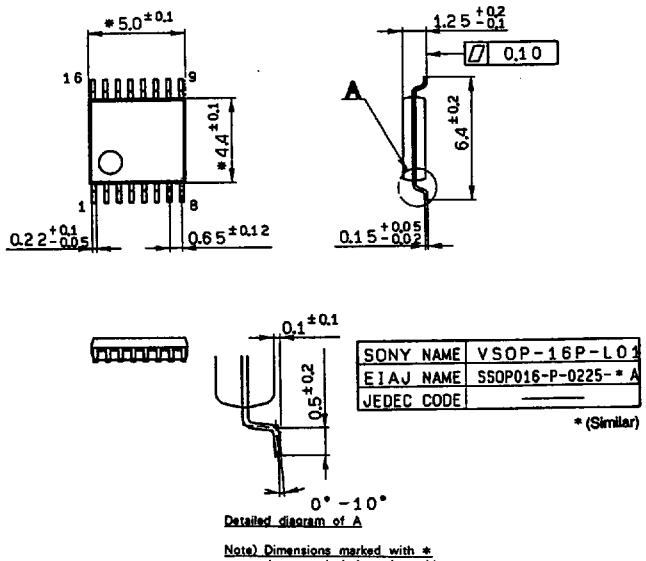
Package Outline Unit : mm

CXA1356M 16pin SOP (Plastic) 300mil 0.2g



SONY NAME	SOP-16P-L01
EIAJ NAME	*SOP016-P-0300-A
JEDEC CODE	———

CXA1356N 16pin VSOP (Plastic) 225mil



SONY NAME	VSOP-16P-L01
EIAJ NAME	SSOP016-P-0225-*A
JEDEC CODE	———

* (Similar)

Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.

Package Name

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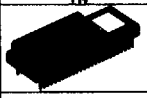
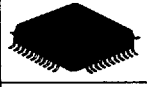
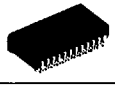
Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN-LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG-ZAG IN-LINE PACKAGE		P	2.54mm (100MIL) Zig-Zag in-line	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1.778mm (70MIL) Zig-Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT L-LEADED PACKAGE		P C	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE L-LEADED PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0.55mm)	Gull-Wing	2-direction
	Standard chip carrier	QFJ	QUAD FLAT J-LEADED PACKAGE		P	1.27mm (50MIL)	J-Lead	4-direction
		QFN	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

*P·····Plastic, C·····Ceramic