ISO²-CMOS ST-BUS™ FAMILY MT8992/3B
Digital Telephone with HDLC
(H-Phone)

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Features

- Integrated digital telephone circuit
- μ-Law/A-Law codec and filters
- Programmable receive gain
- DTMF/Tone generator and tone ringer
- Speakerphone operation
- Interface to standard telephony transducers
- Sense/drive ports
- Single 5 volt power supply
- Intel/Motorola bus interface
- ST-BUS compatible
- X.25 (CCITT) Level 2 HDLC data formatting

Applications

- Featured digital telephone sets
- Voice/Data terminals
- Cellular radio sets

Ordering Information

MT8992/3BC μ-Law/A-Law 40 Pin Cerdip

0 °C to + 70 °C

Description

The MT8992/3B is an integrated digital telephone circuit which provides an on-chip HDLC data formatter (H-Phone). Conversion of analog signals to digital PCM and vice versa is accomplished with an on-chip filter codec. Digital signal processing techniques provide speakerphone operation and generation of ringing tone and DTMF signals. The H-Phone incorporates a bus interface compatible with Intel or Motorola microprocessors and includes an ST-BUS serial interface.

The device is fabricated in Mitel's ISO²-CMOS technology which ensures low power consumption and high reliability.

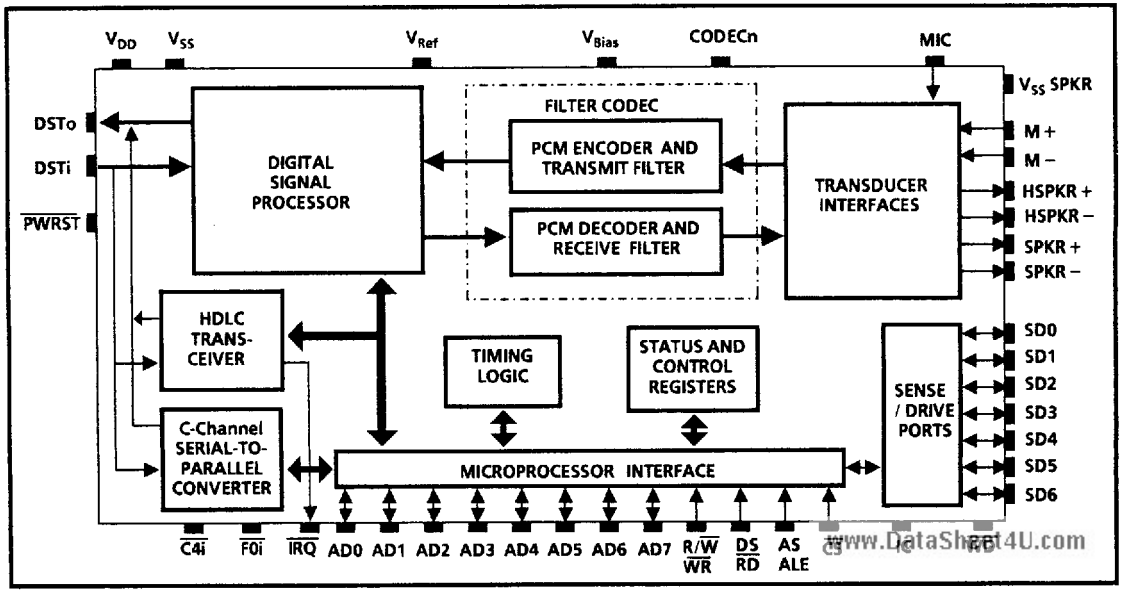

Figure 1 - Functional Block Diagram

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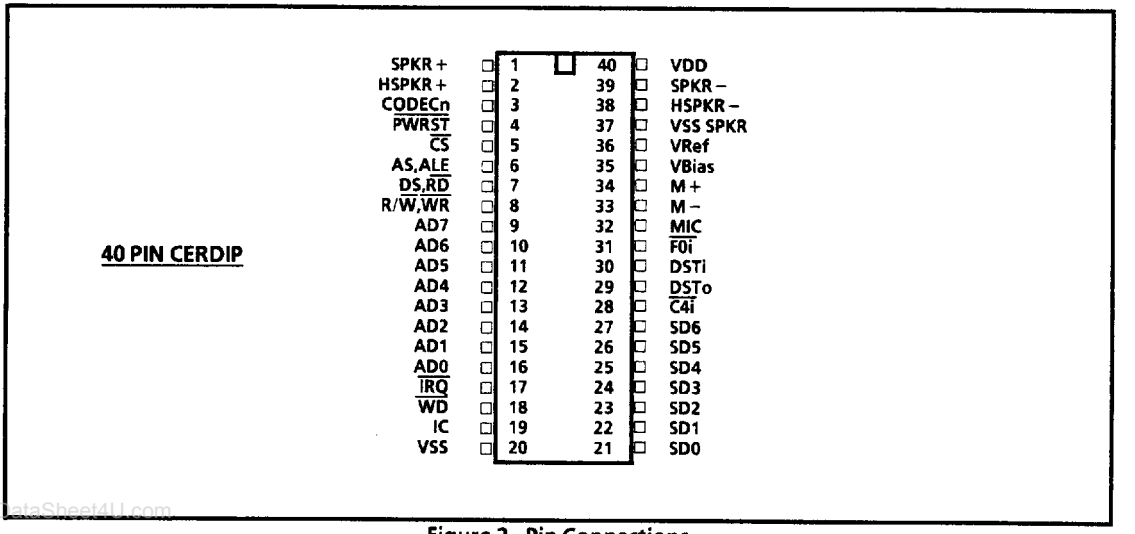

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	SPKR+	**Non-Inverting Speaker (Output).** Output to the speakerphone speaker (balanced).
2	HSPKR+	**Non-Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
3	CODECn	**CODEC Auto-null (Output).** Auto-null point for codec input. Connect 0.1 µF capacitor to V_{SS}.
4	$\overline{PWRST}$	**Power-up Reset (Input).** CMOS compatible input with Schmitt trigger (active low).
5	$\overline{CS}$	**Chip Select (Input).** TTL level compatible (active low). This input signal is used to select the device.
6	AS, ALE	**Address Strobe, Address Latch Enable (Input).** TTL level compatible. The falling edge of AS or ALE causes the address to be latched within the device.
7	DS, $\overline{RD}$	**Data Strobe, Read (Input).** TTL level compatible. When used with Motorola microprocessors, DS is a positive pulse and is commonly referred to as DS (data strobe), E (enable) or $\Phi 2$ (phase 2). Functions as Intel Read strobe also.
8	R/$\overline{W}$, $\overline{WR}$	**Read/Write, Write (Input).** TTL level compatible. This pin functions as a Read/Write input with Motorola microprocessors or as a Write strobe with Intel microprocessors.
9-16	AD0-AD7	**Multiplexed Address/Data bus (Bidirectional).** TTL level compatible.
17	$\overline{IRQ}$	**Interrupt Request (Open Drain).** An output indicating an unmasked HDLC interrupt.
18	$\overline{WD}$	**Watchdog (Output).** Watchdog timer output. Active Low
19	IC	**Internal Connection.** Tied to V_{SS} for normal operation.
20	V_{SS}	**Ground.** Nominally 0 V.
21-27	SD0-SD6	**General Purpose Sense/Drive Points (Bidirectional, open drain).** Input mode is TTL compatible.
28	$\overline{C4i}$	**4096 kHz Clock (Input).** TTL level compatible.
29	DSTo	**ST-BUS™ Serial Stream (Output).** 2048 kbit/s output stream composed of 32 eight bit channels. The H-Phone sources digital signals during the appropriate channel, time coincident with the channels used for DSTi.

Pin Description (continued)

Pin #	Name	Description
30	DSTi	**ST-BUS™ Serial Stream (Input).** 2048 kbit/s input stream composed of 32 eight bit channels; the first five of which may be used by the H-Phone for one of the following functions: 1) a transparent port 2) a PCM channel for the codec (B-channel). Input level is TTL compatible.
31	$\overline{F0i}$	**Frame Pulse (Input).** Input TTL level compatible. This input is for the frame synchronization pulse for the 2048 kbit/s ST-BUS stream.
32	MIC	**Microphone (Input).** Single-ended input to microphone amplifier.
33	M –	**Inverting Microphone (Input).** Inverting input to microphone amplifier from the handset microphone.
34	M +	**Non-Inverting Microphone (Input).** Non-inverting input to microphone amplifier from the handset microphone.
35	V_{Bias}	**Bias Voltage (Input).** ($V_{DD}/2$) volts is applied at this pin. Connect 0.1 µF capacitor to V_{SS}. (see Figure 3)
36	V_{Ref}	**Reference voltage for codec (Output).** Nominally [($V_{DD}/2$)–2] volts. Used internally. Connect 0.1 µF capacitor to V_{SS} (see Figure 3). Enabled when one or more transducers enabled.
37	V_{SS} SPKR	**Power Supply Rail for Speaker Driver.** Nominally 0 Volts.
38	HSPKR –	**Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
39	SPKR –	**Inverting Speaker (Output).** Output to the speakerphone speaker (balanced).
40	V_{DD}	**Positive Power Supply (Input).** Nominally 5 volts.

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Functional Description

The trend in the telecommunications industry is to use digital transmission over the loop between switching equipment and the subscriber equipment. Digitization of the subscriber loop creates a need for Integrated Circuits (IC's) that manipulate digitally encoded audio to perform functions traditionally done mechanically or by analog circuitry. The MT8992/3 H-Phone IC is designed for this purpose. The major functions that the H-Phone provides are:

i) A codec for analog-to-digital and digital-to-analog conversion (Pulse Code Modulation - PCM).

ii) Digital gain control in the receive direction (digital-to-analog direction).

iii) Provision of sidetone.

iv) Generation of Dual Tone Multi-Frequency (DTMF) signals for signalling purposes.

v) A tone ringer to replace the mechanical bell in telephone sets.

vi) A speakerphone algorithm for handsfree telephone operation.

vii) Handset and speakerphone transducer interfaces.

viii) Sense/drive ports for keyboard scanning and driving a display.

ix) X.25 compatible HDLC data transceiver.

A block diagram of the H-Phone is shown in Figure 1. The chip is controlled via an 8-bit multiplexed address/data bus (AD0-AD7) which is compatible with the MOTEL interface specification for operation via both Motorola and Intel style microcontroller busses. There are thirteen 8-bit control registers through which the H-Phone is programmed plus one 8-bit register for the HDLC receive and transmit fifo's.

The Filter Codec section provides conversion between the voiceband analog signals of a telephone subscriber loop and the digital format required in a digital PCM switching system. PCM data is encoded using either μ-Law (MT8992B) rules or A-Law (MT8993B) rules.

In the transmit direction the analog signal is input to the Transmit Filter from either the handset microphone or the speakerphone microphone. The analog signal is then input to the codec circuitry for digital encoding.

Received analog signals can be routed to the handset and/or the speakerphone speaker drivers after being decoded by the codec circuitry. The Receive Filter has programmable gain.

A Digital Signal Processor (DSP) section executes three programs: a speakerphone algorithm, a tone ringer algorithm, and a DTMF/Tone generator algorithm. The DSP processes the PCM streams between the codec and a serial interface. The serial interface is used to transfer information to and from an external digital transmission device (MT8972 DNIC or MT8930 SNIC).

An HDLC transceiver provides X.25, Level 2, packet switching protocol as defined by CCITT. Depacketized data is passed to and from the transceiver via the micro-processor port. To buffer the data flow an 11 byte fifo is provided in the transmit and in the receive direction. The data channel bit rate is selectable from 8, 16, 48 and 64 kbit/s.

The serial interface complies with the serial architecture, defined by Mitel Semiconductor, called the ST-BUS (see MSAN-126). The ST-BUS is a Time Division Multiplexed (TDM) serial bus for intercomponent communication. The microprocessor has access, through the H-Phone's microprocessor port, to a control and status channel on the ST-BUS. This control channel may be used for controlling the digital transmission device mentioned above.

The microprocessor can control or read sense/drive ports (SD0-SD6) through the microprocessor port. These sense/drive ports are intended for keyboard scanning and display functions.

Filter Codec

The Filter Codec section performs analog-to-digital and digital-to-analog conversion and provides the necessary filtering for voice frequency applications. The two variants of the codec function are indicated by the last number in the IC code. The MT8992B complies with the μ-Law companding code and the MT8993B complies with the A-Law companding code.

Analog signals in the transmit path enter at the microphone input pins (MIC or M+, M−), are filtered, and then sampled and converted by the codec. The samples are quantized and assigned 8-bit digital values defined by the PCM encoding law

BIT	NAME	DESCRIPTION
7	HPF	A logic "1" enables a transmit highpass function with a 3dB point at 400 Hz and also moves the transmit filter low end notch from 60 Hz to 120 Hz. This bit must be enabled when the DSP is selected for speakerphone mode, in order for the switching algorithm to perform properly.
6 - 4	Receive Filter Gain	These three bits control the gain of the Receive Filter. Receive Filter gain may be altered in 1 dB increments. Gain settings are as follows: Bit 6 Bit 5 Bit 4 Gain Setting (dB) 0 0 0 0 0 0 1 −1 0 1 0 −2 0 1 1 −3 1 0 0 −4 1 0 1 −5 1 1 0 −6 1 1 1 −7
3 - 0	Receive Digital Gain	These four bits control the Receive Digital Gain in the DSP. Receive Digital Gain may be altered in 6 dB increments. Gain settings are as follows: Bit 3 Bit 2 Bit 1 Bit 0 Gain Setting (dB) 0 1 1 1 +42 0 1 1 0 +36 0 1 0 1 +30 0 1 0 0 +24 0 0 1 1 +18 0 0 1 0 +12 0 0 0 1 +6 0 0 0 0 0 1 0 0 0 0 1 0 0 1 −6 1 0 1 0 −12 1 0 1 1 −18 1 1 0 0 −24 1 1 0 1 −30 1 1 1 0 −36 1 1 1 1 −42

Table 1 - Receive Gain Control Register (Address $0B_H$ - Read/Write)

BIT	NAME	DESCRIPTION
7, 6		Not Used, set to 00_b.
5	DIAL	When set to '1', this bit enables a first order lowpass filter in the Receive Filter with the corner frequency (3 dB point) at 1 kHz.
4	SIDE	When '1', this bit turns on sidetone. When '0', this bit turns off sidetone.
3	HSMIC	When '1' this bit turns on and powers up the handset microphone. When '0' this bit turns off and powers down the handset microphone.
2	SPMIC	When '1' this bit turns on and powers up the speakerphone microphone. When '0' this bit turns off and powers down the speakerphone microphone.
1	SPSKR	When '1' this bit turns on and powers up the speakerphone speaker. When '0' this bit turns off and powers down the speakerphone speaker.
0	HSSKR	When '1' this bit turns on and powers up the handset speaker. When '0' this bit turns off and powers down the handset speaker.

Table 2 - Transducer Control Register (Address $0A_H$ - Read/Write)

being used. After encoding, the digital data is transferred to the DSP.

In the Receive direction the digital data is transferred from the DSP to the codec for digital-to-analog conversion. After digital decoding and filtering the analog signals leave the H-Phone at SPKR+, SPKR– and/or HSPKR+, HSPKR– . Input and output functions are selected via the respective bits in the Transducer Control Register (Table 2).

The switched capacitor filter sections are used for bandlimiting prior to digital encoding in the transmit path and after digital decoding in the receive path.

Receive Filter

The receiver filter is peaked to compensate for the (sin x)/x attenuation caused by the codec's 8 kHz sampling rate. In addition, a first order lowpass filter with the corner frequency at 1 kHz is included in the Receive Filter. When this filter is enabled it reduces the high end of the filter characteristic by a maximum of 5 dB and removes the peaking. This improves the sound of a dial tone signal. The lowpass filter may be enabled or disabled through bit 5 (DIAL) in the Transducer Control Register (see Table 2). The receive filter gain is adjustable (see next section).

Overall Receive Gain Control

The overall gain in the receive direction can be controlled in two sections of the device; the Receive Filter section, and the DSP digital gain control section. The combination of these two gain controls allows received audio to be amplified by a maximum of +42 dB or attenuated by a maximum of –49 dB.

The Receive Filter Gain can be adjusted from 0 to – 7 dB, in 1 dB steps. The Receive Filter Gain is controlled by Receive Gain Control Register bits 6, 5 and 4 as shown in Table 1.

The DSP receive digital gain control section provides gain in the range of +42 dB to–42 dB, programmable in 6 dB steps. The Receive Digital Gain is controlled by Receive Gain Control Register bits 3, 2, 1 and 0 as shown in Table 1. Note that this gain control section is active even when the DSP is disabled (DSPEN=0 in the DSP Control Register - see Table 3). This means that the Receive Digital Gain may be used to amplify or attenuate audio from the serial port regardless of the DSP enable state.

The Receive Gain Control Register is reset to all zeros on power-up. This corresponds to an overall receive gain of 0 dB within the DSP and Filter/Codec sections.

Transmit Filter

Analog signals at the MIC and M+, M– inputs must be bandlimited to 512 kHz to provide the necessary anti-aliasing for the transmit lowpass filter which is clocked at 512 kHz (derived from the 4096 kHz clock signal). A first order lowpass filter with a corner frequency below 25 kHz should be added externally to perform this bandlimiting function. This gives an attenuation of 26 dB at 512 kHz and results in a 0.1 dB drop across the passband in the transmit path. A programmable highpass function is required to enhance speakerphone switching (see bit 7, Table 1).

V_{Bias}

The codec must be biased externally by applying a voltage ($V_{DD}/2$) at the V_{Bias} input. $V_{DD}/2$ may be derived by the simple voltage divider shown in Figure 3. Notice that V_{Bias} and V_{Ref} decoupling capacitors are physically grounded at the same point.

For optimum performance of the codec, it is necessary to ensure that the power supply (V_{DD}) has low noise levels. For line powered applications, where DC to DC conversion is implemented using high frequency switching techniques, additional filtering may be required to minimize ripple voltages.

Noise on V_{Bias} will affect the H-Phone acoustic parametric performance. To decrease V_{Bias} noise, a tantalum capacitor (33 µF) may have to be added in parallel to the voltage divider resistance tied to V_{SS}.

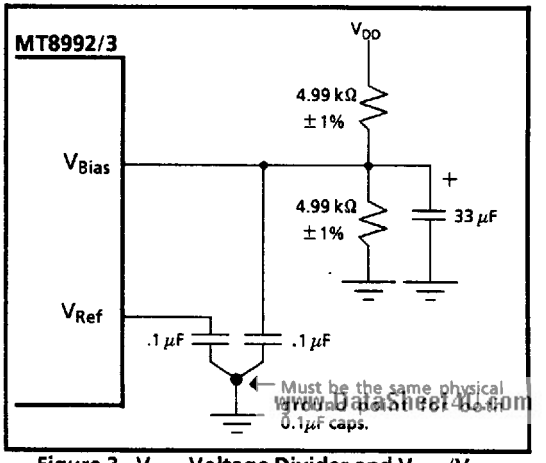

Figure 3 - V_{Bias} Voltage Divider and V_{Bias}/V_{Ref} Decoupling

Transducer Interfaces

In a telephone set, interfaces to the handset and the speakerphone are required. There are four transducer interfaces in the H-Phone. These are the handset microphone interface, handset speaker interface, speakerphone microphone interface and speakerphone speaker interface. The signals output from either microphone are routed to the Transmit Filter and the signal to the speaker drivers is output from the Receive Filter. Note that both inputs need to be bandlimited to 512 kHz. Refer to the Transmit Filter section for details.

In addition, a fixed sidetone is available which, if enabled, routes the signals input from either microphone to the speakers. Sidetone is turned on/off by bit 4 (SIDE) in the Transducer Control Register (see Table 2).

All of these transducer interfaces can be powered down independently under software control via the Transducer Control Register bits 3-0 as shown in Table 2. When powered down, the outputs go into a high impedance state.

Telephone Handset Speaker Output

This is a balanced differential drive section that is capable of driving the network shown in Figure 4. The output pins are (HSPKR+ and HSPKR–). Two 0.33 µF capacitors must be used to compensate the speaker driver amplifier. The 75 ohm resistors and 1000 pF capacitors are required to filter out high frequency components coupled from external

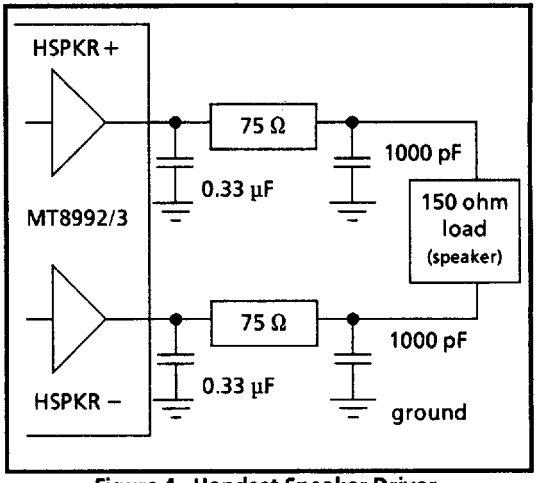

Figure 4 - Handset Speaker Driver

sources. For more details (eg., gain) refer to AC Electrical Characteristic of the Handset Speaker.

Speakerphone Speaker Output

This is another balanced differential drive section. The output pins are (SPKR+ and SPKR–). The speaker can be connected directly to the output pins. For more details (eg., gain) refer to A/C Electrical Characteristic - Speakerphone Speaker.

Telephone Handset Microphone Input

The telephone handset microphone interface is a differential input circuit. The input pins are M+ and M–. Figure 5 shows the recommended

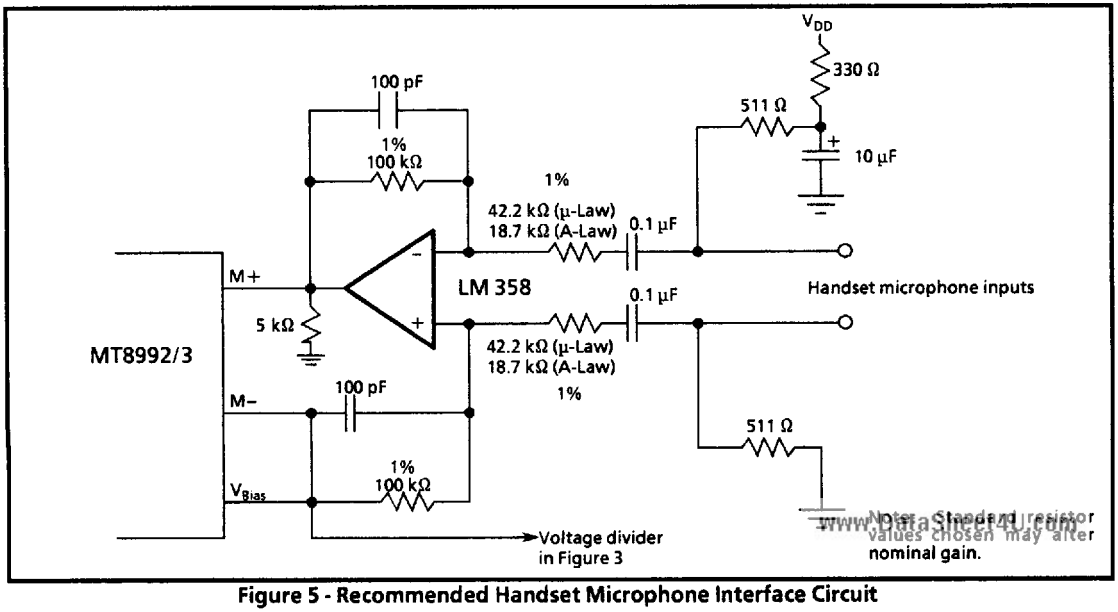

Figure 5 - Recommended Handset Microphone Interface Circuit

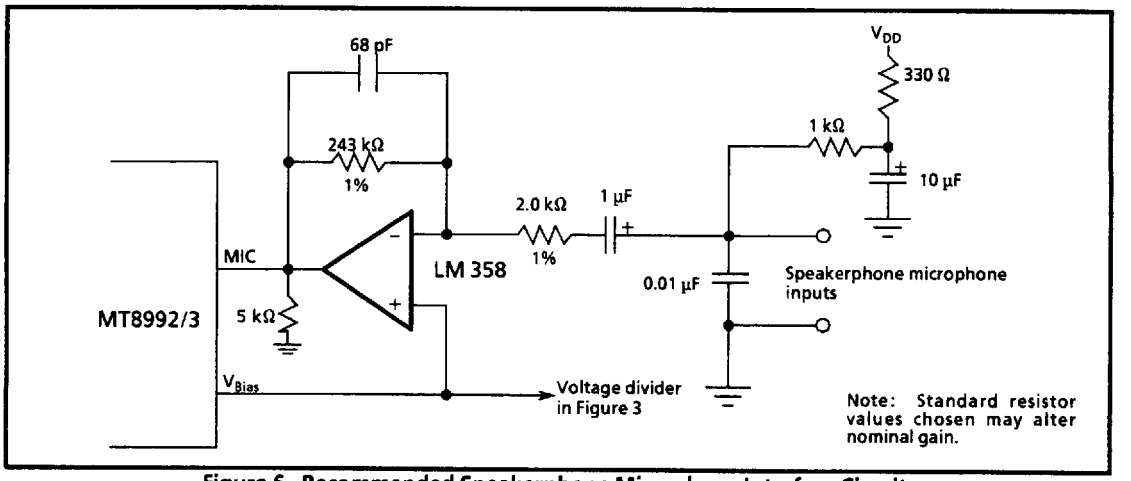

Figure 6 - Recommended Speakerphone Microphone Interface Circuit

telephone handset microphone interface circuit. This circuit has a gain of 7.3 dB (µ-Law) and 16.7 dB (A-Law).

Speakerphone Microphone Input

The speakerphone microphone interface is a single ended input (MIC). Figure 6 shows the recommended speakerphone microphone interface circuit. This circuit has a gain of 41.6 dB

Digital Signal Processor (DSP)

The DSP processes PCM as it is transferred between the codec and the serial port (causing a 125 µs delay). The DSP can also generate PCM sequences independently and send this information to the codec and/or the serial port. Alternatively, the DSP may pass PCM transparently between the serial port and the codec (Receive Digital Gain may be applied in the Receive direction). The DSP implements the following functions needed for telephone set operation:

i) Programmable dual sinewave generation for DTMF signalling and generating call progress tones.

ii) Programmable frequency shifted squarewave generation for a Tone Ringer function.

iii) A speakerphone algorithm for handsfree telephone operation.

The operation of the DSP is controlled by three registers which can be accessed by the µP. The overall function of the DSP is controlled by the DSP Control Register. Table 3 describes the allowable states of the DSP Control Register. The other two registers, Tone Register 1 and Tone Register 2, are programmed with frequency coefficients for the tone generator programs.

Dual Tone Generator

When the DSP section is operating in the Dual Tone Generator mode a dual sinewave is generated (digitally) and routed to the codec and/or the serial port. Either of these paths may be disabled by DSP Control Register bit 6 (CPCMEN) and bit 5 (DPCMEN). See Table 3.

The Dual Tone Generator is programmed as follows:

i) Disable DSP via DSP Control Register (DSPEN, bit 0=0);

ii) Write frequency coefficients to the two DSP tone registers (Tone Register 1 and Tone Register 2);

iii) Select Dual Tone Generator function, enable DSP and destinations for the tones via the DSP Control Register.

The coefficients for Tone Register 1 and Tone Register 2 are calculated as follows:

Coefficient (Hex) = HEX (10^{-3} x 128 x F)

where F is the desired frequency in Hz. and HEX( ) represents conversion to Hex. The frequency generated by a coefficient is given by:

Frequency = DEC (Coefficient) ÷ 0.128

where DEC( ) represents conversion from Hex to Decimal.

BIT	NAME	DESCRIPTION
7		Not Used, set to 0_b.
6	CPCMEN†	When '1', this bit enables the PCM link from the DSP to the codec. When '0', a zero signal level, PCM equivalent, sent to the codec.
5	DPCMEN†	When '1', this bit enables the PCM link from the DSP to the serial interface. When '0', a zero signal level, PCM equivalent, sent to the serial interface.
4, 3	Function Select Bits	The operation of the Function Select Bits is as follows: Bit 4 Bit 3 Function 0 0 No Program Executed 0 1 Dual Tone Generator 1 0 Tone Ringer 1 1 Speakerphone algorithm
2	CADENCE	When '1' this bit turns the Tone Ringer on. A '1' to '0' transition causes the Tone Ringer output to decay to zero with a time constant of approximately 100 ms.
1	WR/NS	The function of this bit is dependent on the setting of the Function Select Bits. When Tone Ringer is selected, this bit controls the rate of warble. A '1' sets the warble rate (frequency shift rate) to 16 Hz. A '0' sets the warble rate to 10 Hz. When the speakerphone application is selected, a '1' enables automatic noise suppression (noise will not be transmitted in the absence of a valid signal).
0	DSPEN	When '1', the DSP is enabled and program execution will start on the next Frame Pulse. When '0', the DSP is disabled and PCM is passed transparently between the codec and the serial port. The Receive Digital Gain may still be used.

Table 3 - DSP Control Register (Address 09_H - Read/Write)

† PCM is delayed 125 µsec (one ST-BUS frame) through the DSP

Low-group Frequency	Tone Register 1 † Coefficient	Frequency Generated
697 Hz	59 Hex	695.3 Hz
770 Hz	63 Hex	773.4 Hz
852 Hz	6D Hex	851.6 Hz
941 Hz	78 Hex	937.5 Hz
High-group Frequency	**Tone Register 2 ‡ Coefficient**	**Frequency Generated**
1209 Hz	9B Hex	1210.9 Hz
1336 Hz	AB Hex	1335.9 Hz
1477 Hz	BD Hex	1476.6 Hz
1633 Hz	D1 Hex	1632.8 Hz

Table 4 - DTMF Signals Generation

† Tone Register 1 Address = '07' Hex Write Only
‡ Tone Register 2 Address = '08' Hex Write Only

The range of frequencies that may be generated is from 7.8 Hz to 1992 Hz. The programmable frequency resolution is within ±3.9 Hz of the desired frequency. Tones generated from Tone Register 2 are approximately 2.5 dB greater in amplitude than tones generated by Tone Register 1. This provides the negative twist required if the tones are intended for DTMF signalling. Negative twist is specified for DTMF signalling to compensate for high group attenuation over analog transmission facilities, therefore the high group frequencies must be programmed in Tone Register 2. Table 4 shows the values of the coefficients in Tone Register 1 and Tone Register 2 required to generate DTMF signals.

The level of the composite dual tone signal in the Receive direction is controlled by the Receive Digital Gain bits 3-0 in the Receive Gain Contol Register. The total power for the dual tone is fixed at −4 dBm0 for µ-Law and −9.9 dBm0 for A-Law. 0 dBm0 equals 0.948 V_{RMS} for µ-Law and 0.985 V_{RMS} for A-Law when V_{Ref} = 0.5 Volts and V_{Bias} = 2.5 Volts.

Tone Ringer

The Tone Ringer algorithm generates a frequency shifted squarewave. Frequency shifted means that the frequency of the waveform alternates between two programmable frequencies. Values in the two frequency coefficient registers determine the two frequencies of the squarewaves. The frequency range for the programmable squarewaves is from 15.7 Hz to 4000 Hz. The shift rate is selected by the state of the WR/NS bit in the DSP Control Register (bit 1). The frequency shift rate may be either 16 Hz or 10 Hz. The amplitude of the composite waveform

is programmed by the Receive Digital Gain bits 3-0 in the Receive Gain Control Register.

The Tone Ringer waveform may be routed to the codec, but it cannot be routed to the serial port. The PCM output from the codec is, however, passed transparently to the serial port.

The cadence (on/off duty cycle) of the Tone Ringer output is controlled by the external μP via the DSP Control Register. The CADENCE bit (bit 2) is used for this function. When bit 2 is changed to a '0', the squarewave amplitude decays to zero within approximately 100 ms. This 100 ms decay may be eliminated by setting CPCMEN bit 6 in the DSP Control Register to '0'. This causes the audio path, to the speaker, to be disconnected which cuts the tone ringer output off abruptly. The CPCMEN path must be re-enabled before the next burst of tone ringer can be produced. The micro controlled off and on time is independent of the Tone Ringer frequencies and totally under software control.

The Tone Ringer is programmed as follows:

i) Disable DSP via the DSP Control Register.

ii) Write the Tone Ringer frequency coefficients into Tone Register 1 and Tone Register 2.

iii) Select the speaker volume by writing to the Receive Gain Control Register.

iv) Enable DSP and Tone Ringer via the DSP Control Register.

v) Toggle CADENCE, bit 2 in the DSP Control Register, according to the desired Tone Ringer cadence.

The 8-bit Hex coefficients are calculated as follows:

$$\text{Coefficient (Hex)} = \text{HEX}\{[1/(F \times 2.5 \times 10^{-4})]-1\}$$

where F is the frequency of the squarewave (ringing tone) in Hz. HEX{ } represents conversion to Hex.

Speakerphone

The speakerphone algorithm provides handsfree telephone operation. The transmit (Tx - Analog-to-Digital) and receive (Rx - Digital-to-Analog) gain sections operate in a complementary, half-duplex manner. When the transmit signal is in control of the half-duplex channel, a zero signal level, PCM equivalent is sent to the codec from the DSP. When the received signal is in control of the half-duplex channel, a transmit PCM, attenuated by 18 dB, is sent from the DSP to the serial port.

The DSP determines which side should be given preference based upon the relative levels of the audio signals. A voice detector algorithm decides whether the audio signal is voice or background noise. The transmission of background noise is suppressed in the Tx direction when no other signal is present, if WR/NS (see Table 3) is '1'. Channel direction switching continues normally, determined by the relative level of the receive and transmit signals.

The speakerphone function is programmed via the DSP Control Register as follows:

i) Disable side-tone (SIDE) and enable the speakerphone speaker (SPSKR) and microphone (SPMIC) using the Transducer Control Register (Table 2).

ii) Select the speaker volume and enable the highpass filter (HPF) by writing to the Receive Gain Control Register (Table 1).

iii) Enable the DSP (DSPEN), Speakerphone algorithm (Function Select Bits 3,4), and PCM buffer (DPCMEN) and the CPCMEN bit via DSP Control Register (Table 3).

HDLC Transceiver

The HDLC Transceiver handles the bit oriented protocol structure and formats the data channel as per level 2 of the X.25 packet switching protocol defined by CCITT. It transmits and receives the packetized data (information or control) serially in a format shown in Figure 7, while providing data transparency by zero insertion and deletion. It generates and detects the flags, various link channel states and the abort sequence. Further, it provides a cyclic redundancy check on the data packets using the CCITT defined polynomial and includes a selectable 8, 16, 48 or 64 kbit/s data channel as well as an HDLC loopback (test register bit 2 DSTLB) from the transmit to the receive port. These features are enabled through the HDLC control register in D, B1, B2, B3 channels (see Table 5).

HDLC Frame Format

All frames start with an opening flag and end with a closing flag as shown in Figure 7. Between these two flags, a frame contains the data and the frame check sequence (FCS).

i) Flag

The flag is a unique pattern of 8 bits (01111110) defining the frame boundary. The transmit section

FLAG	DATA FIELD	FCS	FLAG
ONE BYTE	n BYTES (n≥2)	TWO BYTES	ONE BYTE

Figure 7. Frame Format

generates the flags and appends them automatically to the frame to be transmitted. The receive section searches the incoming packets for flags on a bit-by-bit basis and establishes frame synchronization. The flags are used only to identify and synchronize the received frame and are not transferred to the FIFO.

ii) Data

The data field refers to the Address, Control and Information fields defined in the CCITT recommendations. A valid frame should have a data field of at least 16 bits.

iii) Frame Check Sequence (FCS)

The 16 bits following the data field are the frame check sequence bits. The generator polynomial is:

$$G(x) = x^{16} + x^{12} + x^5 + 1$$

The transmitter calculates the FCS on all bits of the data field and transmits the complement of the FCS with most significant bit first. The receiver performs a similar computation on all bits of the received data but also includes the FCS field. The generating polynomial will assure that if the integrity of of the transmitted data was maintained, the remainder will have a consistent pattern and this can be used to identify, with high probability, any bit errors which occurred during transmission. The error status of the received packet is indicated by B5 and B4 bits in the HDLC Status Register.

iv) Zero Insertion and Deletion

The transmitter, while sending either data from the FIFO or the 16 bits FCS, checks the transmission on a bit-by-bit basis and inserts a ZERO after every sequence of five contiguous ONEs (including the last five bits of FCS) to ensure that the flag sequence is not imitated. Similarly the receiver examines the incoming frame content and discards any ZERO directly following the five contiguous ONE's.

v) Abort

The transmitter aborts a frame by sending eight consecutive ONEs. The FA bit in the HDLC Control Register along with a write to the HDLC Transmit FIFO enables the transmission of an abort sequence instead of the byte written to the register (to have a valid abort there must be at least two bytes in the packet). On the receive side, a frame abort is defined as seven or more contiguous ONE's

BIT	NAME	DESCRIPTION
B7		Not Used.
B6	RxDIS	A '0' enables the HDLC receiver for the selected channel. A '1' disables the HDLC receiver (i.e., an all 1's signal will be received).
B5	TxDIS	A '0' enables the HDLC transmitter for the selected channel. A '1' disables the HDLC transmitter (i.e., an all 1's signal will be sent).
B4	EOP(1)	A '1' will 'tag' the next byte written to the transmit FIFO and cause an end of packet sequence to be transmitted once it reaches the bottom of the FIFO.
B3	FA(1)	A '1' will 'tag' the next byte written to the transmit FIFO and cause an abort sequence to be transmitted once it reaches the bottom of the FIFO.
B2	IFTF	This bit selects the Inter Frame Time Fill. A '1' selects continuous flags. A '0' selects an all 1's idle state.
B1-B0		Bit Rate BRS1 / BRS0 / Data Rate / Bits Used 0 / 0 / 8 kbit/s / D0 1 / 1 / 16 kbit/s / D0, D1 0 / 1 / 48 kbit/s / D0-D5 1 / 0 / 64 kbit/s / D0-D7

Table 5. HDLC Control Register (Address 03H/Write)

Note 1: These bits will not be reset after a write to the TxFIFO

BIT	NAME	DESCRIPTION
B7	Int	If '1' an unmasked asynchronous interrupt has been detected.
B6	Idle	If '1', an idle channel state has been detected.
B5-B4	RxByte Status	These two bits indicate the status of the received byte which is ready to be read from the 11 deep received FIFO. The status is encoded as follows: B5 - B4 0 - 0 - Packet Byte 0 - 1 - Last Byte (Good FCS) 1 - 0 - First Byte 1 - 1 - Last Byte (Bad FCS)
B3-B2	TxFIFO Status	These two bits indicate the status of the 11 deep transmit FIFO as follows: B3 - B2 0 - 0 - Tx FIFO Full 0 - 1 - ≥4 Bytes 1 - 0 - Tx FIFO Empty 1 - 1 - ≤3 Bytes
B1-B0	RxFIFO Status	These two bits indicate the status of the 11 deep receive FIFO. This status is encoded as follows: B1 - B0 0 - 0 - Rx FIFO Empty 0 - 1 - ≤7 Bytes 1 - 0 - Rx FIFO Overflow 1 - 1 - ≥8 Bytes

Table 6. HDLC Status Register (Address 03_H - Read)

BIT	NAME	DESCRIPTION
B7	EnGA	A '1' will enable the Go-Ahead interrupt signal which is identified by the reception of 01111111_{0B} sequence. A '0' will disable it.
B6	EnEOPD	A '1' will enable the receiver End of Packet Detect interrupt. A '0' will disable it.
B5	EnEOPR	A '1' will enable the receive FIFO End of Packet Read interrupt. A '0' will disable it.
B4	EnFA	A '1' will enable the Frame Abort interrupt. A '0' will disable it.
B3	EnTx3/11	A '1' will enable the Transmit FIFO Low interrupt. A '0' will disable it.
B2	EnTxFun	A '1' will enable the Transmit FIFO Underrun interrupt. A '0' will disable it.
B1	EnRx8/11	A '1' will enable the Receive FIFO 8/11 interrupt. A '0' will disable it.
B0	EnRxFull	A '1' will enable the Receive FIFO Full interrupt. A '0' will disable it.

Table 7. HDLC Interrupt Mask Register (Address 04_H - Write)

BIT	NAME	DESCRIPTION
B7	GA[1]	A '1' indicates that a go-ahead sequence (01111110_B) has been detected on the received HDLC data channel.
B6	EOPD[1]	A '1' indicates that an end of packet has been detected on the HDLC receiver. This can be in the form of a flag, an abort sequence or as an invalid packet.
B5	EOPR[1]	A '1' indicates that the byte just read from RxFIFO was tagged as an end of packet byte.
B4	FA[1]	A '1' indicates that the receiver has detected a frame abort sequence on the received data stream.
B3	Tx3/11[1]	A '1' indicates that the device has only three bytes remaining in the Tx FIFO. This bit has significance only when the Tx FIFO is being depleted, not when it is being loaded.
B2	TxFun[1]	A '1' indicates that the Tx FIFO is empty without being given the 'end of packet' indication. The HDLC will transmit an abort sequence after encountering an underrun condition.
B1	Rx8/11[1]	A '1' indicates that the HDLC controller has accumulated at least 8 bytes in the Rx FIFO.
B0	RxFull[1]	A '1' indicates that the Rx FIFO is full. All new data written to a full receive FIFO will be ignored until the FIFO is read.

Table 8. HDLC Interrupt Status Register (Address 04_H - Read)

Note 1: All interrupts will be reset after a read to the HDLC Interrupt Status Register.

occurring after the start flag and before the end flag of a packet that contains at least 26 bits (not including the frame abort). An interrupt can be generated on reception of the abort sequence using FA bit in the HDLC Interrupt Mask/Vector Registers (refer to Tables 7 and 8).

Interframe Time Fill and Link Channel States

When the HDLC Tranceiver is not sending packets, the transmitter can be in one of two states mentioned below depending on the status of the IFTF bit in the HDLC Control Register.

i) Idle State

The Idle state is defined as 15 or more contiguous ONE's. When the HDLC Protocoller is observing this condition on the receiving channel, the Idle bit in the HDLC Status Register is set HIGH. On the transmit side, the Protocoller ends the transmission of all ones (idle state) when data is loaded into the transmit FIFO.

ii) Interframe Time Fill State

The HDLC Protocoller transmits continuous flags ($7E_{Hex}$) in Interframe Time Fill state and ends this state when data is loaded into the transmit FIFO. The reception of the interframe time fill will have the effect of setting the idle bit in the HDLC Status Register to '0'.

HDLC Transmitter

On power up, the HDLC transmitter is enabled and in the idle state. The transmitter can be disabled through the TxDIS in the HDLC Control Register. To start a packet, the data is written into the 11 byte Transmit FIFO (starting with the address field). All the data must be written to the FIFO in a bytewide manner. When the data is detected in the transmit FIFO, the HDLC protocoller will proceed in one of the following ways:

1) If the transmitter is in idle state, the present byte of ones is completely transmitted before sending the opening flag. The data in the transmit FIFO is then transmitted.

2) If the transmitter is in the interframe time fill state, the flag presently being transmitted is used as the opening flag for the packet stored in the transmit FIFO.

To indicate that the particular byte is the last byte of the packet, the EOP bit in the HDLC Control Register must be set before the last byte is written into the transmit FIFO. After the transmission of the last byte in the packet, the frame check sequence (16 bits) is sent followed by a closing flag. If there is any more data in the transmit FIFO, it is immediately sent after the closing flag. That is, the closing flag of a packet is also used as the opening flag for the next packet. If there is no more data to

be transmitted, the transmitter assumes the selected link channel state. During the transmission of either the data or the frame check sequence, the Protocol Controller checks the transmitted information on a bit by bit basis to insert a ZERO after every sequence of five consecutive ONE's. This is required to eliminate the possibility of imitating the opening or closing flag, the idle code or an abort sequence.

i) Transmit Underrun

A transmit underrun occurs when the last byte loaded into the transmit FIFO was not 'flagged' with the 'end of packet' EOP bit, or the FA bit, and there are no more bytes in the FIFO. In such a situation, the Protocol Controller transmits the abort sequence (eight ones) and moves to the selected link channel state. The transmit underrun is ignored if the packet is less than two bytes long.

Conversely, in the event that the transmit FIFO is full, any further writes will overwrite the last byte in the Transmit FIFO.

ii) Abort Transmission

If it is desired to abort the packet currently being loaded into the transmit FIFO, the next byte written to the FIFO should be 'flagged' to cause this to happen. The FA bit of the HDLC Control Register must be set HIGH, before writing the next byte into the FIFO. When the 'flagged' byte reaches the bottom of the FIFO, a frame abort sequence is sent instead of the byte and the transmitter operation returns to normal. The frame abort sequence is ignored if the packet has less then two bytes.

HDLC Receiver

After a reset on power up, the receive section is enabled. The receive section can be disabled by RxDIS bit in the Control Register. All HDLC interrupts are masked, thus the desired interrupt signal must be unmasked through the HDLC Interrupt Mask Register. All active interrupts are cleared by reading the HDLC Interrupt Status Register. The HDLC controller can also recognize a Go-Ahead sequence. This Go-Ahead signal consists of the binary pattern 011111110 and can be used for higher level protocolling.

i) Normal Packets

After initialization as explained above, the serial data starts to be clocked in and the receiver checks for the idle channel and flags. If an idle channel is detected, the 'Idle' bit in the HDLC Status Register is set HIGH. Once a flag is detected, the receiver synchronizes itself in a bytewide manner to the incoming data stream. The receiver keeps resynchronizing to the flags until an incoming packet appears. The incoming packet is examined on a bit-by-bit basis, inserted zeros are deleted, the FCS is calculated and the data bytes are written into the 11 byte Receive FIFO. However, the FCS and other control characters, i.e., flag and abort are never stored in the Receive FIFO.

All the bytes written to the receive FIFO are flagged with two status bits. The status bits are found in the HDLC status register and indicate whether the byte to be read from the FIFO is the first byte of the packet, the middle of the packet, the last byte of the packet with good FCS or the last byte of the packet with bad FCS.

The incoming data is always written to the FIFO in a bytewide manner. However, in the event of data sent not being a multiple of eight bits, the software associated with the receiver should be able to pick the data bits from the LSB positions of the last byte in the received data written to the FIFO. The protocoller does not provide any indication as to how many bits this might be.

ii) Invalid Packets

If there are less than 24 data bits between the opening and closing flags, the packet is considered invalid and the data never enters the receive FIFO (inserted zeros do not form part of the valid bit count). This is true even with data and the abort sequence, the total of which is less than 24 bits. The data packets that are at least 24 bits but less than 32 bits long are also invalid, but not ignored. They are clocked into the receive FIFO and tagged as having bad FCS.

iii) Frame Abort

When a frame abort is received the appropriate bit in the Interrupt Flag is set. The last byte of the packet that was aborted is written to the FIFO with a status of 'last byte bad FCS' tagged to it.

iv) Idle Channel

While receiving the idle channel, the idle bit in the HDLC status register remains set.

vi) Receive Overflow

Receive overflow occurs when the receive section attempts to load a byte to an already full receive FIFO. All attempts to write to the full FIFO will be ignored until the receive FIFO is read. When

overflow occurs, the rest of the present packet being received is ignored.

Serial Interface

A serial port is required to transfer PCM between the DSP and an external digital transmission device. This serial interface conforms to the ST-BUS architecture defined by Mitel Semiconductor (see MSAN-126). The ST-BUS consists of four signals: an output serial stream (DSTo), an input serial stream DSTi), a clock signal ($\overline{C4i}$), and a framing pulse ($\overline{F0i}$).

The serial streams have a data rate of 2048 kbps, and are Time Division Multiplexed into 32 channels, each with a 64 kbit/s data rate. Individual channel instances are grouped into frames that contain 32 octets of information, each octet belonging to one of the 32 channels. The frame rate is 8 kHz, and each frame has a 125 µs period (see Figure 8).

$\overline{C4i}$ has a frequency that is twice the data rate. DSTi is sampled by the H-Phone at the halfway point in a bit cell (a bit cell is two $\overline{C4i}$ cycles long), and DSTo is output at the start of a bit cell. $\overline{F0i}$ defines frame boundaries. A valid $\overline{F0i}$ pulse is a logic low coinciding with a falling edge of $\overline{C4i}$. The timingfor the ST-BUS is shown in Figure 12.

DSTi And DSTo Channel Assignment

The H-Phone can use the first five timeslots following the frame pulse (F0i). The first channel (channel 0) following the frame pulse may contain HDLC formatted data only. Theses channels may be separately enabled or disabled. Channel 1 is dedicated to control/status information transferred between the H-Phone and the transmission device. This channel is accessible directly from the µP port. Channels 2, 3 and 4 can be assigned to contain PCM for and from the H-Phone.

The ST-BUS output of the H-Phone, DSTo, goes to a high impedance state during the timeslots not used. Having the DSP enabled in more than one channel is not allowed. In this case only the first channel in which it was selected is enabled.

The five serial channels utilized on the ST-BUS are called the D-channel, C-channel, B1-channel, B2-channel, and B3-channel. See Figure 9 for DSTi and DSTo channel assignments. The purpose of having more than one channel selectable on the ST-BUS is because digital transmission devices like the MT8972 and the MT8930 have more than one channel available for PCM or data to be transmitted.

Timeslot assignment for the ST-BUS is controlled through the Timing Control Register (Table 9). All H-Phone channels may be completely disabled,

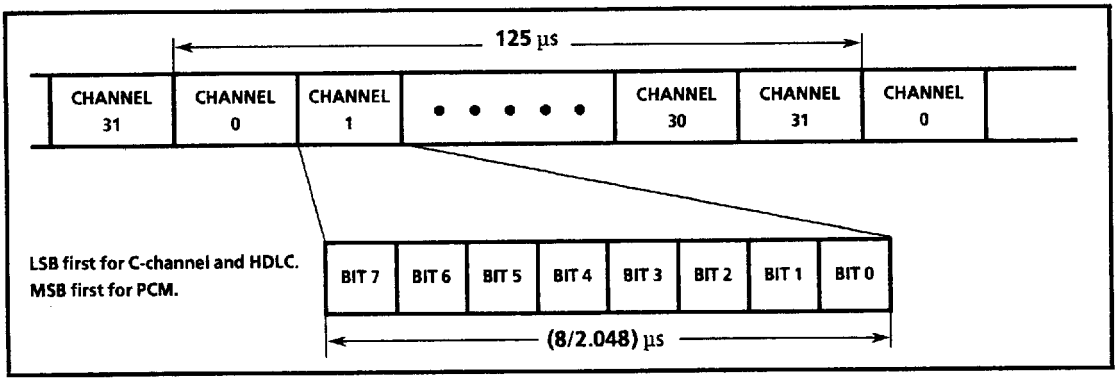

Figure 8 - Format of ST-BUS Stream

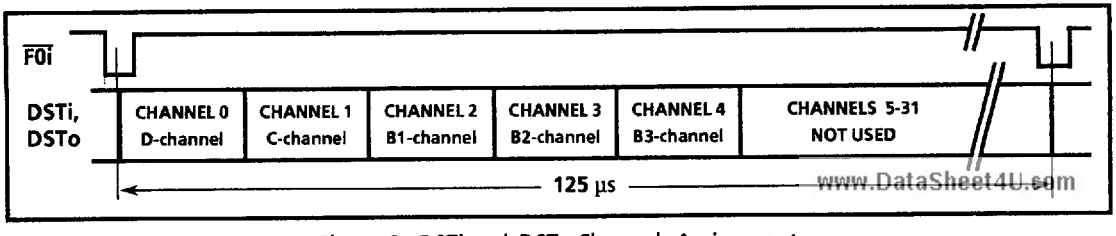

Figure 9 - DSTi and DSTo Channels Assignment

enabling other devices to access the transmission device. During and after power-up reset (PWRST) DSTo is in a high impedance state for all channels until the Timing Control Register is programmed.

Microprocessor Port

The microprocessor port allows microprocessor access to the H-Phone internal control registers, the sense/drive ports, the ST-BUS C-channel and the HDLC transceiver.

The microprocessor (µP) interface is of the type proposed by Motorola in the MOTEL interface description. The data bus and the address bus are multiplexed to reduce pin count.

The timing control pins change automatically to either the "Data Strobe" signal of Motorola style architectures, or to the "Read Strobe/Write Strobe" signals of Intel style architectures. In both configurations, the AS/ALE (Address Strobe, or Address Latch Enable) is a high going pulse. The state of the (DS, $\overline{RD}$) input when AS/ALE is high is used to determine how the timing control pins (DS, $\overline{RD}$ and R/$\overline{W}$,$\overline{WR}$) are used to control µP accesses.

In a Motorola style architecture, the (DS, $\overline{RD}$) input is low on the falling edge of AS. (R/$\overline{W}$, $\overline{WR}$) is in this case considered a R/$\overline{W}$ signal. (DS, $\overline{RD}$) is considered to be a DS signal. See Figure 13.

In an Intel style architecture, (DS, $\overline{RD}$) would be high on the falling edge of ALE. The (R/$\overline{W}$, $\overline{WR}$) signal should be considered a $\overline{WR}$ strobe in an Intel architecture and the (DS, $\overline{RD}$) signal should be considered a $\overline{RD}$ strobe. See Figures 14 and 15.

Reset places the device in the Motorola mode of operation. In Motorola mode, $\overline{CS}$ can be used to qualify data instead of DS if DS is valid. In Intel mode, $\overline{CS}$ can be used to qualify data instead of $\overline{WR}$ or $\overline{RD}$ if either are valid.

H-Phone Internal Register Map

There are thirteen 8-bit control registers through which the H-Phone may be programmed plus one 8-bit register for the HDLC receive and transmit FIFO. Table 10 gives a summary of the H-Phone register map. Note that any register with unused bits will return a '1' when attempting to read these bits.

C-Channel Access

A double-buffered serial-to-parallel conversion for the asynchronous reception of C-channel (Channel 1) octets on DSTi is provided. A double-buffered parallel-to-serial conversion for asynchronous transmission of C-channel octets on DSTo is also

BIT	NAME	DESCRIPTION
7	Channel 1 Select	When '1' Channel 1 carries C-channel information. When '0' Channel 1 is in a high impedance state.
6	Channel 0 ① Select	When '1' Channel 0 carries HDLC data. When '0' Channel 0 is in high impedance state.
5, 4	Channel 4 Select	The state of Channel 4 is as follows: Bit 5 Bit 4 Channel 4 State 0 0 High Impedance 0 1 PCM 1 0 High Impedance 1 1 HDLC Transceiver
3, 2	Channel 3 Select	The state of Channel 3 is as follows: Bit 3 Bit 2 Channel 3 State 0 0 High Impedance 0 1 PCM 1 0 High Impedance 1 1 HDLC Transceiver
1, 0	Channel 2 Select	The state of Channel 2 is as follows: Bit 1 Bit 0 Channel 2 State 0 0 High Impedance 0 1 PCM 1 0 High Impedance 1 1 HDLC Transceiver

Table 9 - Timing Control Register (Address 05_H - Read/Write)

①If HDLC is enabled in any, or all, of channels 2, 3 and 4 then it will be disabled in channel 0 regardless of the state of Bit 6

Address (A7 - A0)	Read	Write	Reference
00_H	C-channel on DSTi (LSB first)	C-channel on DSTo (LSB first)	
01_H	Not used	Not used	
02_H	HDLC Receiver FIFO	HDLC Transmit FIFO	See Text
03_H	HDLC Status	HDLC Control	Table 6 & 5
04_H	HDLC Interrupt Status	HDLC Interrupt Mask	Table 8 & 7
05_H	Timing Control	Timing Control	Table 9
06_H	Not used	Watchdog Timer	See Text
07_H	Not used	Tone Register 1	Table 4
08_H	Not used	Tone Register 2	Table 4
09_H	DSP Control	DSP Control	Table 3
$0A_H$	Transducer Control	Transducer Control	Table 2
$0B_H$	Receive Gain Control	Receive Gain Control	Table 1
$0C_H$	SD Data	SD Data	Table 11
$0D_H$	Not used	SD Data Direction	Table 12
$0E_H$	Not used	Test Register	Table 13
$0F_H$	Not used	Not used	

Table 10 - H-Phone Internal Register Map

provided. The C-channel is enabled by setting Timing Control Register bit 7 to "1".

The C-channel is accessed by the µP at address "00" Hex. A µP read operation reads the C-channel information received on DSTi. A µP write operation writes C-channel information to be output on DSTo. Note that the data is transmitted least significant bit first, and received least significant bit first.

Sense/Drive (SD) Ports

Seven TTL compatible sense/drive ports, SD6 to SD0, are accessible to the external µP. They are intended for keyboard scanning, display driving, etc.

Table 11 maps the bits of the SD Data Register to the SD input/output ports. The state of SD6 to SD0 ports may be sensed by a µP read (whether they are inputs or outputs). If a port is configured as an output, a µP write determines the state of the relevant SD output.

Table 12 maps the SD Data Direction Register bits to the relevant SD port. The contents of this register determines whether an SD port is an input or an output. A '0' configures a port as an input and a '1' configures a port as an output. On power up reset the SD ports are configured as inputs.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
---	SD6	SD5	SD4	SD3	SD2	SD1	SD0

Table 11 - SD Data Register (Address $0C_H$ - Read/Write)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
---	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Table 12 - SD Data Direction Register (Address $0D_H$ - Write)

Watchdog Timer

The watchdog timer and output pin ($\overline{WD}$) may be used as a sanity check for the microcontroller and its operating program. To do this, the $\overline{WD}$ pin is tied to the reset pin of the micro.

$\overline{WD}$ goes low whenever the H-Phone is held in a reset state and will return high immediately after the release of reset along with starting a watchdog timer of period ($T = 2^9$ x cycles of $\overline{F0i}$).

Normally the micro will be instructed to write $XXX01010_B$ to watchdog address 06_H, once within every period, to restart the watchdog timer. If this is done then $\overline{WD}$ will remain high. If the micro fails to restart the timer (by writing address 06_H), then a timeout will occur at the end of 2^9 cycles of $\overline{F0i}$. The micro will be presumed insane (i.e., lost in continuous loop, been hit by static discharge, etc.) and $\overline{WD}$ will then go low for period (T) and proceed to toggle at this rate until address 06_H is again written with the proper data. This results in a reset of the micro back to its start vectors.

The timer is clocked on the falling edge of $\overline{F0i}$ and requires only this input, along with device power, for operation (i.e., the H-Phone does not need to be selected).

BIT	NAME	DESCRIPTION
7		Not Used, set to 0_b.
6,5	Test Enable	To enable any of the test modes, these bits must be set to '01'.
4		Not Used, set to 0_b.
3	PCMLB	When '1', the PCM path from the DSP to the codec is looped back to the DSP, permitting the DSP to be tested by observing DSTo with respect to DSTi. When '0', the PCM path from the codec to the DSP operates normally.
2	DSTLB	When ' 1', DSTo is looped back to DSTi before the DSP. When '0', the DSTo path from the DSP operates normally.
1	DAC	When ' 1', the MIC input is looped back to the M+ pin via the normal A/D and D/A paths, providing a test of the A/D and D/A paths. When '0', this loopback is disabled. This loopback may not be enabled if bit 0 = 1.
0	FILTER	When '1', the Transmit and Receive Filters may be tested separately. The MIC input is connected to the Receive Filter input, and the Receive Filter output is connected to M–. The Transmit Filter input is connected to the MIC input and the Transmit Filter output is connected to M+. This test path may not be enabled if bit 1 = 1. When M+ and M– are used as outputs a buffer amplifier must be provided at the pin.

Table 13 - Test Register (Address $0E_H$ - Write)

Testing

Due to the complexity of the digital and analog circuitry, a test register has been included in the H-Phone chip. When the test modes are being exercised the contents of all the other registers are unaffected.

See Table 13 for the details involving the Test Register. For any of the test modes to be implemented it is necessary to have bit 6 of the Test Register set to '0', and bit 5 of the Test Register set to '1'.

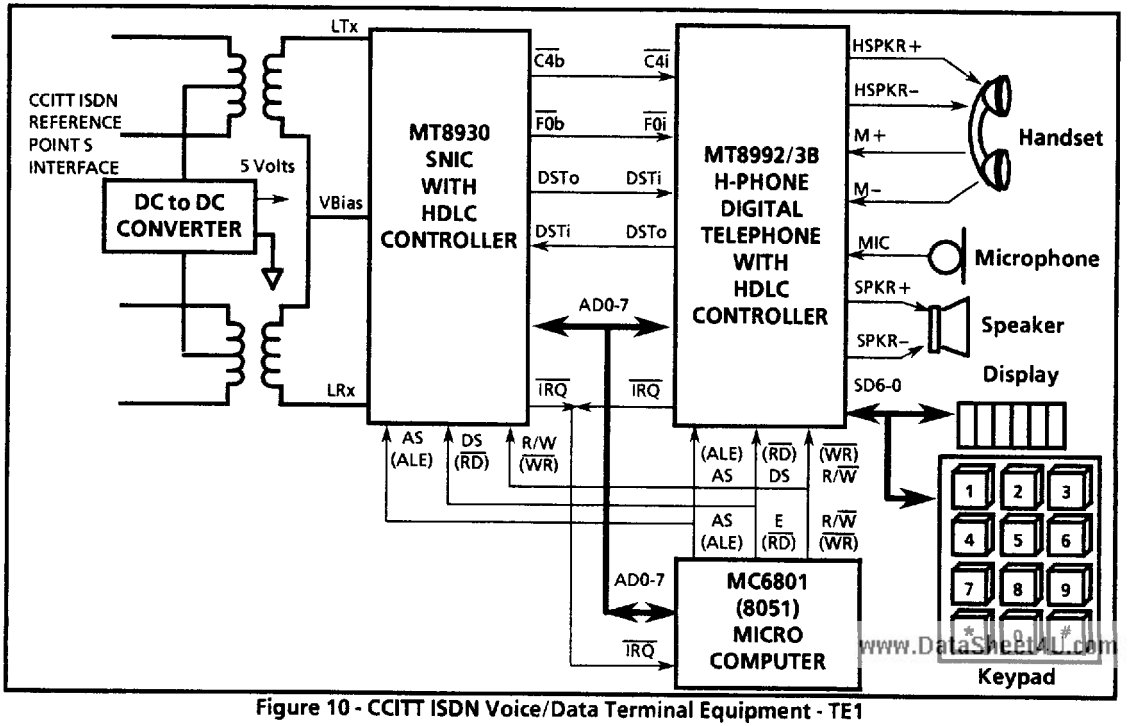

Figure 10 - CCITT ISDN Voice/Data Terminal Equipment - TE1

Applications

The MT8992/3B is part of Mitel's ISDN family of components for use in digital telephone sets. When combined with the MT8930 (Subscriber Network Interface Circuit-SNIC) an ISDN terminal equipment (TE) function may be implemented. See Figure 10.

The H-Phone may also be combined with the MT8972 (Digital Network Interface Circuit - DNIC) to implement voice/data digital telephone sets. See Figure 11. Low power requirements enable the circuit to be line powered without causing excess power drain on the host system.

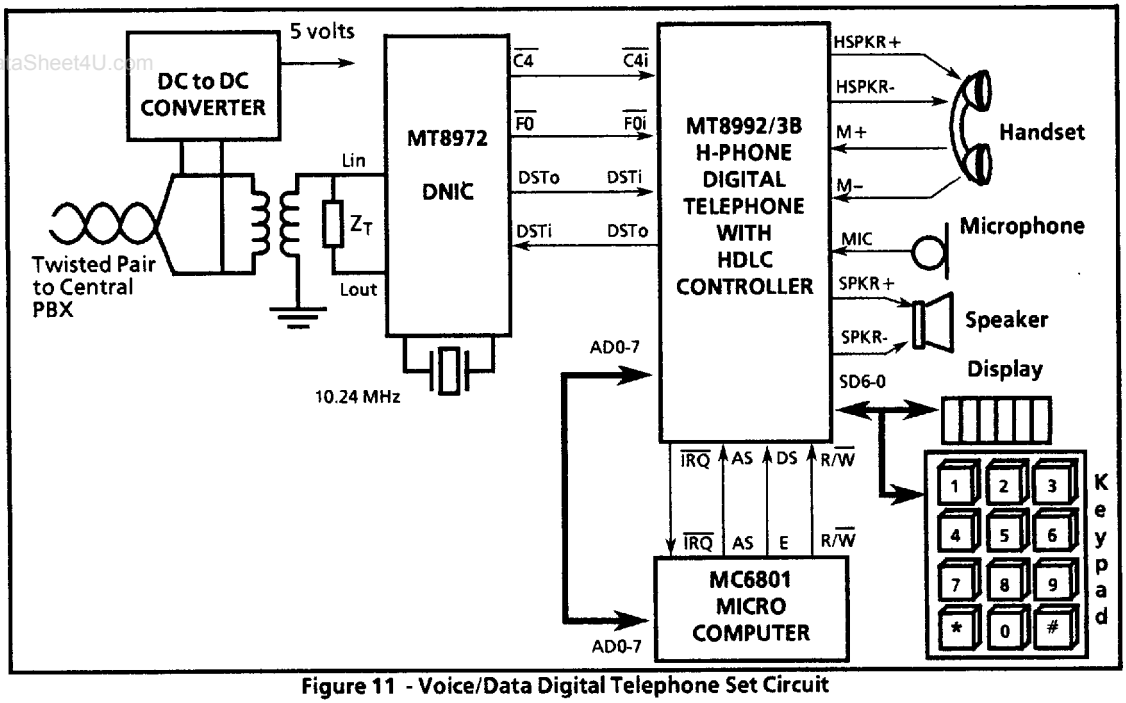

Figure 11 - Voice/Data Digital Telephone Set Circuit

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	$V_{DD}-V_{SS}$	−0.3	7	V
2	Voltage on any I/O pin	V_I/V_O	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	Current on any I/O pin	I_I/I_O		±20	mA
4	Storage Temperature	T_S	−65	+150	°C
5	Power Dissipation (package) Ceramic	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5	5.25	V	
2	Input Voltage (high)	V_{IH}	2.4		V_{DD}	V	Noise margin = 400 mV
3	Input Voltage (low)	V_{IL}	V_{SS}		0.4	V	Noise margin = 400 mV
4	Operating Temperature	T_O	0		+70	°C	
5	Clock Frequency	f_{CLK}		4096		kHz	

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Current (clock disabled) (clock enabled)	I_{DDC1} I_{DDC2}		1 2	3 4	mA mA	Outputs unloaded
2	Supply Current (handset speaker enabled) No Load Load = 150Ω	I_{DDH1} I_{DDH2} I_{DDH3}		4 4 5	8 - 9	mA mA mA	No signal −20 dBm0, 1020 Hz 0 dBm0, 1020 Hz
3	Supply Current (speaker driver enabled) No Load Load = 40Ω	I_{DDS1} I_{DDS2} I_{DDS3}		5 7 45	13 - 70	mA mA mA	No signal −20 dBm0, 1020 Hz 0 dBm0, 1020 Hz
4	Input HIGH Voltage TTL inputs	V_{IH}	2.0			V	
5	Input LOW Voltage TTL inputs	V_{IL}			0.8	V	
6	Input Voltage	V_{Bias}		2.5		V	
7	Input Leakage Current①	I_{IZ}		0.1	10	µA	$V_{IN} = V_{DD}$ to V_{SS}
8	Positive Going Threshold Voltage ($\overline{PWRST}$ only) Negative Going Threshold Voltage ($\overline{PWRST}$ only)	V_{T+} V_{T-}		1.7 1.2			$V_{DD} = 5$ V $V_{DD} = 5$ V
9	Output LOW Voltage TTL O/P	V_{OL}			0.4	V	$I_{OL} = 2.8$ mA
10	Output HIGH Voltage TTL O/P	V_{OH}	2.4			V	$I_{OH} = -7$ mA
11	Output HIGH Current TTL O/P	I_{OH}	-7	−15		mA	$V_{OH} = 2.4$ V
12	Output LOW Current TTL O/P SD0-6	I_{OL}	2.8 2.8	5 5		mA	$V_{OL} = 0.4$ V $V_{OL} = 0.4$ V
13	Output Voltage	V_{Ref}		$V_{DD}/2$-2		V	No load
14	Output Leakage Current①	I_{OZ}		0.01	10	µA	$V_{OUT} = V_{DD}$ and V_{SS}

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
①TTL compatible and SD0-SD6 pins only.

AC Electrical Characteristics†

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input Pin Capacitance	C_I		8		pF	
2	Output Pin Capacitance	C_O		8		pF	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† -ST-BUS Timing (See Figure 12)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	$\overline{C4i}$ Clock Period	t_{C4P}		244		ns	
2	$\overline{C4i}$ Clock High period	t_{C4H}		122		ns	
3	$\overline{C4i}$ Clock Low period	t_{C4L}		122		ns	
4	$\overline{C4i}$ Clock Transition Time	t_T		20		ns	
5	$\overline{F0i}$ Frame Pulse Setup Time	t_{F0iS}			50	ns	
6	$\overline{F0i}$ Frame Pulse Hold Time	t_{F0iH}			50	ns	
7	$\overline{F0i}$ Frame Pulse Width Low	t_{F0iW}		150		ns	
8	DSTo Delay	t_{DSToD}		125	200	ns	$C_L = 50$ pF
9	DSTi Setup Time	t_{DSTiS}			60	ns	
10	DSTi Hold Time	t_{DSTiH}			0	ns	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

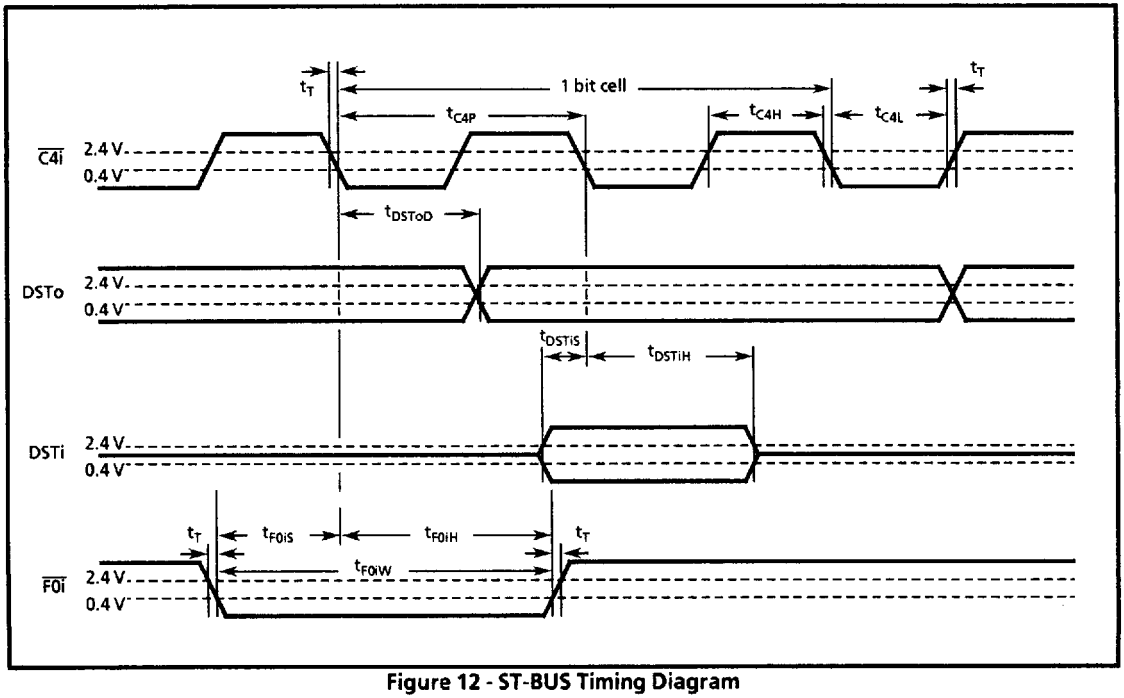

Figure 12 - ST-BUS Timing Diagram

AC Electrical Characteristics - Microprocessor Bus Timing† - (See Figures 13, 14 & 15)

	Characteristics	Sym	Min	Typ‡	Max	Units
1	Cycle Time	t_{CYC}		310		ns
2	Pulse Width, DS Low or $\overline{RD}$, $\overline{WR}$ High	PW_{EL}	240			ns
3	Pulse Width, DS High or $\overline{RD}$, $\overline{WR}$ Low	PW_{EH}	225			ns
4	Input Rise and Fall Time	t_r, t_f			30	ns
5	R/$\overline{W}$ Hold Time	t_{RWH}	10	0		ns
6	R/$\overline{W}$ Setup Time Before DS Rise	t_{RWS}		20		ns
7	Chip Select Setup Time Before DS rise, $\overline{RD}$, $\overline{WR}$ Fall	t_{CS}	50			ns
8	Chip Select Hold Time	t_{CH}	0			ns
9	Read Data Hold Time	t_{DHR}		10		ns
10	Write Data Hold Time	t_{DHW}	15			ns
11	Muxed Address Valid Time to AS, ALE Fall	t_{ASL}	40			ns
12	Muxed Address Hold Time	t_{AHL}	0			ns
13	Delay Time DS or $\overline{RD}$ or $\overline{WR}$ to AS, ALE Rise	t_{ASD}	50	0		ns
14	Pulse Width, AS, ALE High	PW_{ASH}	30	10		ns
15	Delay Time AS, ALE to DS Rise, $\overline{RD}$, $\overline{WR}$ Fall	t_{ASED}	10	0		ns
16	Peripheral Output Data Delay Time from DS or $\overline{RD}$	t_{DDR}		130	220	ns
17	Peripheral Data Setup Time	t_{DSW}	100			ns

† Timing is over recommended temperature range & recommended power supply voltages. All values shown assume a 50 pF load on the data pins. Read means read from the H-Phone and Write means write to the H-Phone.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

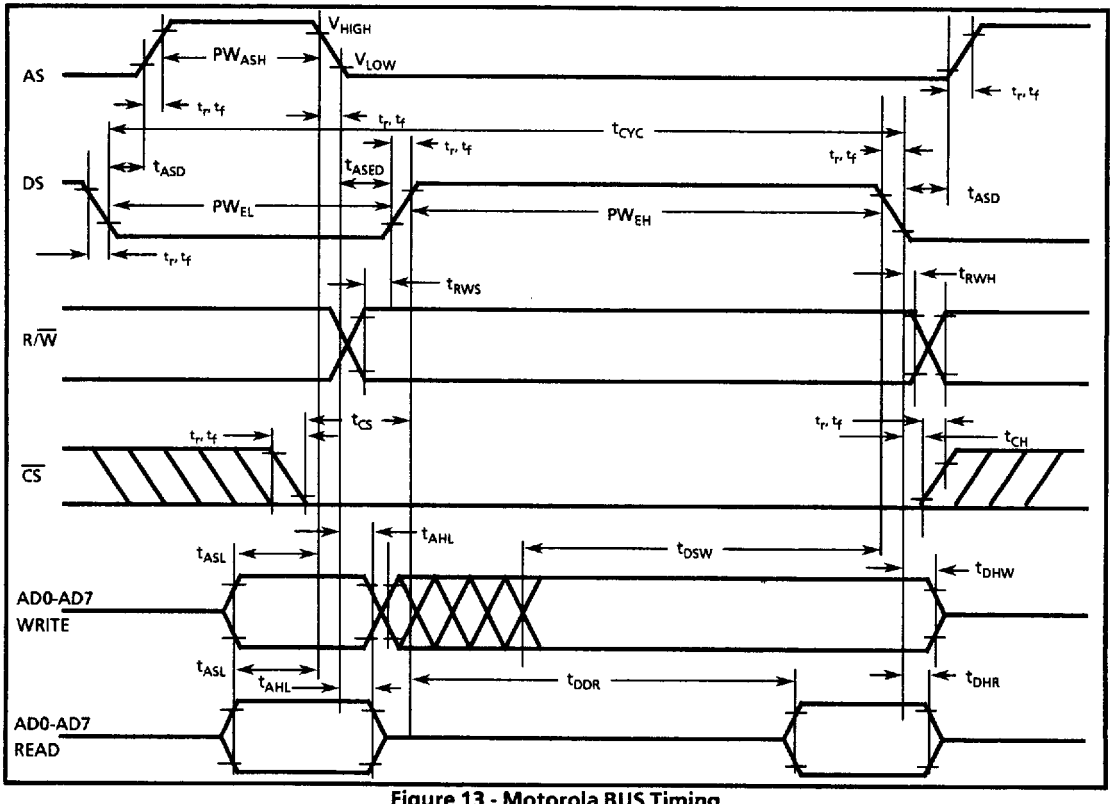

Figure 13 - Motorola BUS Timing

Note: $V_{HIGH} = (V_{DD} - 2.0)$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 5 %

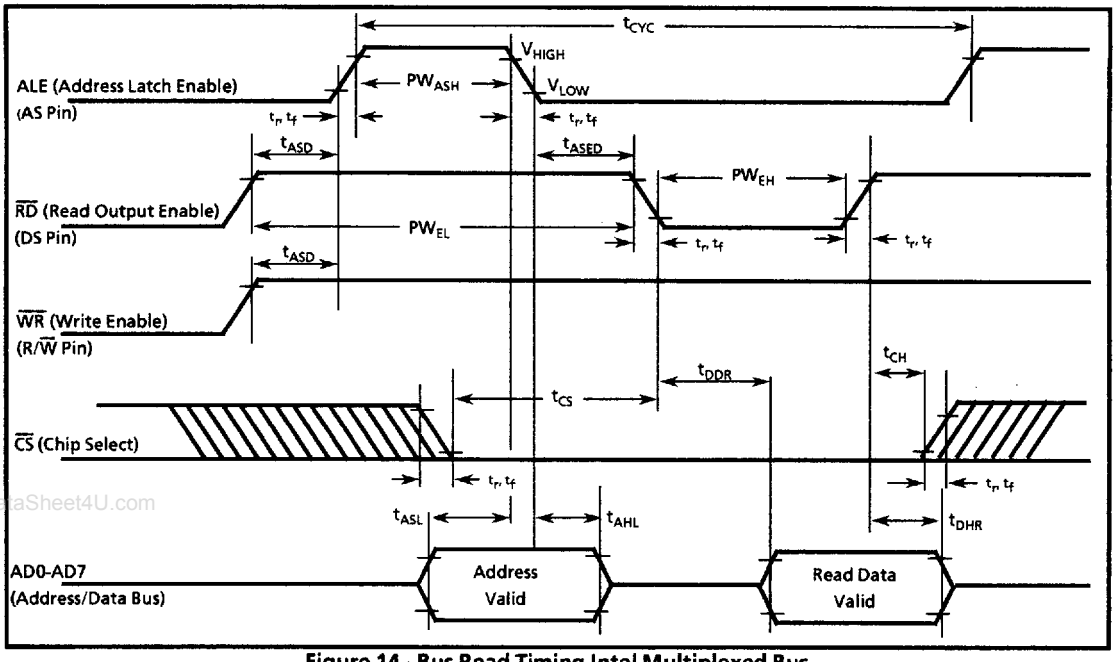

Figure 14 - Bus Read Timing Intel Multiplexed Bus

Note: $V_{HIGH} = (V_{DD}-2.0)$ V , V_{LOW} = 0.8 V, for V_{DD} = 5.0 V ±5 %

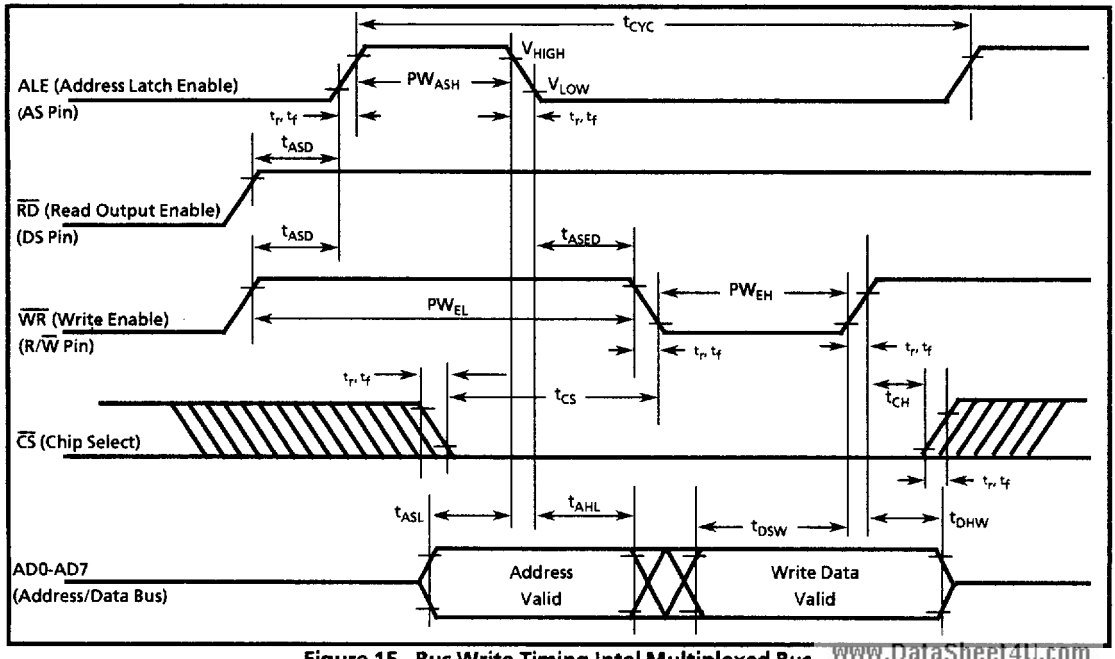

Figure 15 - Bus Write Timing Intel Multiplexed Bus

Note: $V_{HIGH} = (V_{DD}-2.0)$ V , V_{LOW} = 0.8 V, for V_{DD} = 5.0 V ±5 %

AC Electrical Characteristics † - Transmit Path (Microphone Interface, Transmit Filter And A/D)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Analog input to the codec equivalent to overload decision	V_{IN}		3.863 4.000		V_{PP} V_{PP}	μ-Law A-Law
2	Absolute Gain	G_{AX}	7.0	7.5	8.0	dB	at 1020 Hz
3	Gain Tracking using CCITT G.714 method 2②	GT_X	 −0.3 −0.6 −1.6	 ±0.15 ±0.4 ±1.0	 +0.3 +0.6 +1.6	 dB dB dB	Sinusoidal level +3 to −40 dBm0① −40 to−50 dBm0 −50 to −55 dBm0
4	Quantization Distortion using CCITT G.714 method 2②	D_{QX}	 35 29 24	 38.0 31.0 27.0		 dB dB dB	 0 to −30 dBm0 −40 dBm0 −45 dBm0
5	Idle Channel Noise③	N_{CX} N_{PX}		19 −64		dBrnC0 dBm0p	µ-Law A-Law
6	Harmonic Distortion	D_H		-60	−46	dB	Input signal 0 dBm0 at 1020 Hz
7	Envelope Delay 1000-2600 Hz Variation with 600-3000 Hz Frequency 400-3200 Hz	D_{DX}		60 150 250		μs μs μs	Input signal: 400-3200 Hz sinewave at 0 dBm0
8	Gain relative to gain at 1020 Hz <50 Hz 60 Hz 200 Hz 300-2800 Hz 3100-3200 Hz 3300 Hz 3400 Hz 4000 Hz >4600 Hz	G_{RX}	 −1.8 −0.2 −0.25 −0.35 −0.9 	 	 −25 −30 0 +0.2 +0.25 +0.15 −0.1 −14 −32	 dB dB dB dB dB dB dB dB dB	0 dBm0 input signal Transmit Filter response with Highpass Filter disabled (Refer to Table 1). The HP Filter switches the notch at 60 Hz to 120 Hz and adds a high pass function that rolls the filter characteristic off−3 dB at 400 Hz.

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
① 0 dBm0 = 0.948 V_{RMS} for μ-Law and 0.985 V_{RMS} for A-Law (V_{Ref} = 0.5 volt and V_{Bias} = 2.5 volts at respective pins).
② signal fed to MIC input and measurement made after A/D conversion in PCM environment.

AC Electrical Characteristics† - Receive Path (D/A, Receive Filter, Speakerphone Speaker/ Handset Speaker Interface)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Analog output from the codec equivalent to overload decision	V_{OUT}		3.863 4.000		V_{PP} V_{PP}	μ-Law A-Law
2	Absolute gain (Receive Filter and D/A)①	G_{AR}	−0.35		+0.35	dB	at 1020 Hz
3	Deviation of attenuation adjustment (Receive Filter)	D_{AA}	−0.15		+0.15	dB	from nominal
4	Differential handset speaker driver gain μ-Law A-Law	G_{DA}	−14.9 −12.6	−13.9 −11.6	−12.9 −10.6	dB	across 150 Ω load, See Figure 4④
5	Side-tone② μ-Law A-Law	S_T	-16 -22.9	−15 −21.9	-14 -20.9	dB	from M± inputs to 150 Ω load
6	Differential speakerphone speaker driver gain③	G_{SS}	2.8	3.8	4.8	dB	
7	Gain tracking using CCITT G.714 method 2③	GT_R	 −0.3 −0.35	 ±0.15 ±0.15 ±0.5	 +0.3 +0.35	 dB dB dB	Sinusoidal level 0 to −20 dBm0 −20 to−30 dBm0 −40 dBm0
8	Quantization distortion using CCITT G.714 method 2③	D_{QR}	36 30	39.0 38.0 31.0 26.0		dB dB dB dB	0 to −20 dBm0 - 30 dBm0 −40 dBm0 −45 dBm0
9	Idle channel noise	N_{CR} N_{PRS} N_{PRHS}		19 −64 10		dBrnC0 dBm0p dBrnC0	μ-Law SPKR+, SPKR− A-Law SPKR+, SPKR− A-Law and μ-Law across 150 Ω load, See Figure 4④
10	Gain relative to gain at 1020 Hz <200 Hz 200 Hz 300-2800 Hz 3100-3200 Hz 3300 Hz 3400 Hz 4000 Hz >4600 Hz	G_{RR}	 −0.2 −0.2 −0.25 −0.35 −0.8		 +0.2 +0.2 +0.2 +0.25 +0.15 −0.1 −14 −28	 dB dB dB dB dB dB dB dB	Receive Filter response with DIAL disabled (Refer to Table 2). DIAL inserts a first order rolloff at 1 kHz into the receive path.

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
① Note that Rx filter can be adjusted from 0 to −7 dB in 1 dB steps.
② Roll-off 6 dB/octave @ 2.5 kHz.
③ 0 dBm0 input signal, 40 ohm load across SPKR+ and SPKR−.
④ Measurements are made using the test circuit shown in Figure 4.

5

AC Electrical Characteristics† - Receive Path (D/A Receiver Filter, Speakerphone Speaker/Handset Speaker Interface)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
11	Speaker driver distortion 1ST 2ND Total Distortion	D_S		−65 −65 −60	-45 -45	dB dB dB	0 dBm0 input signal, 40Ω/ 150pF load across SPKR+ and SPKR− ① ②
12	PCM input without clipping at the speakerphone μ-Law speaker driver A-Law	C_{PCM}		+1.57 +1.24		dBm0 dBm0	40 ohm load across SPKR+ and SPKR− ① ②
13	Handset driver distortion 1ST 2ND Total Distortion	D_H		-60 -60 -60	−40 −40	dB dB dB	0 dBm0 input signal, 150 Ω load, see Figure 4. ① ② ③
14	Output offset voltage SPKR+, SPKR−, HSPKR+ and HSPKR−	V_{OS}		±25		mV	w.r.t. V_{Bias}
15	SPKR+ and SPKR−peak power		63	94		mW	40 ohm speaker V_{DD}=5V, T=25°C
16	Envelope Delay 1000-2600 Hz Variation with 600-3000 Hz Frequency 400-3200 Hz	D_{DR}		90 170 265		μs μs μs	Input signal: 400-3200 Hz digital sinewave at 0dBm0

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
① 0 dBm0 refers to the input to the drivers from the codec, Rx filters and the PCM at DSTi.
② Distortion may degrade due to clipping at lower V_{DD} voltages or when valid input signal levels have been exceeded.
③ Measurements are made using the test circuit shown in Figure 4.

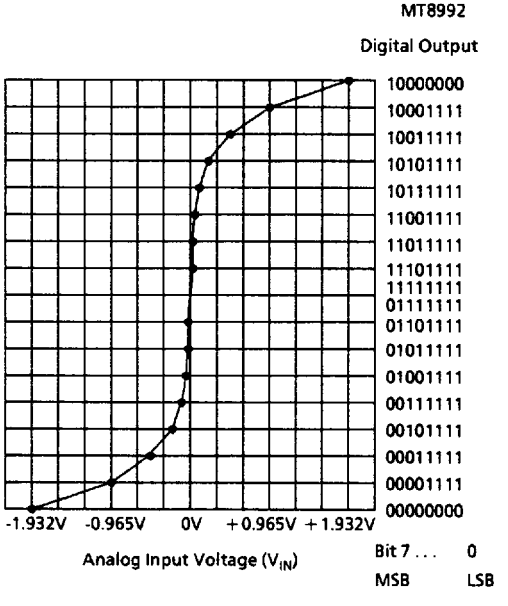

Figure 16 - μ-Law Encoder Transfer Characteristic

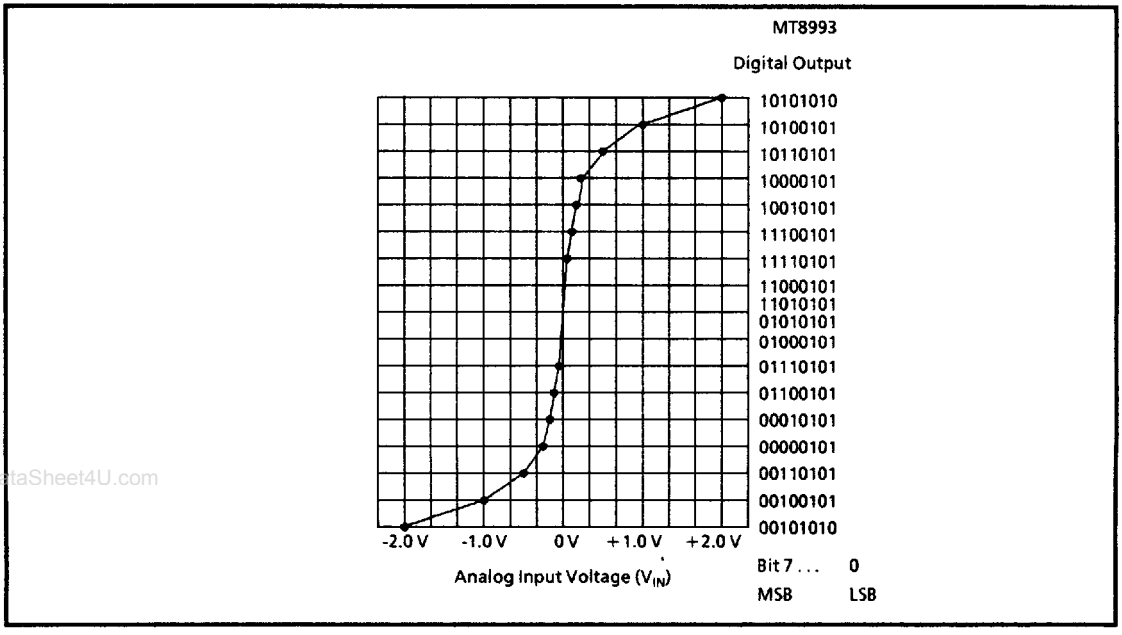

Figure 17 - A-Law Encoder Transfer Characteristic

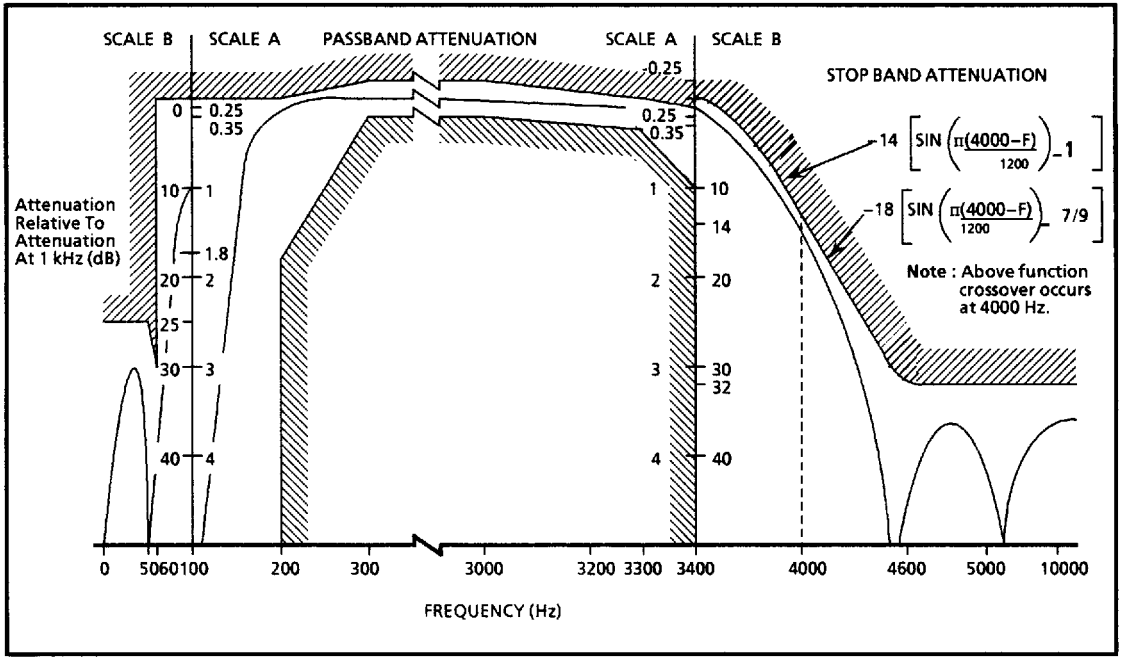

Figure 18 - Attenuation vs Frequency for Transmit Filter

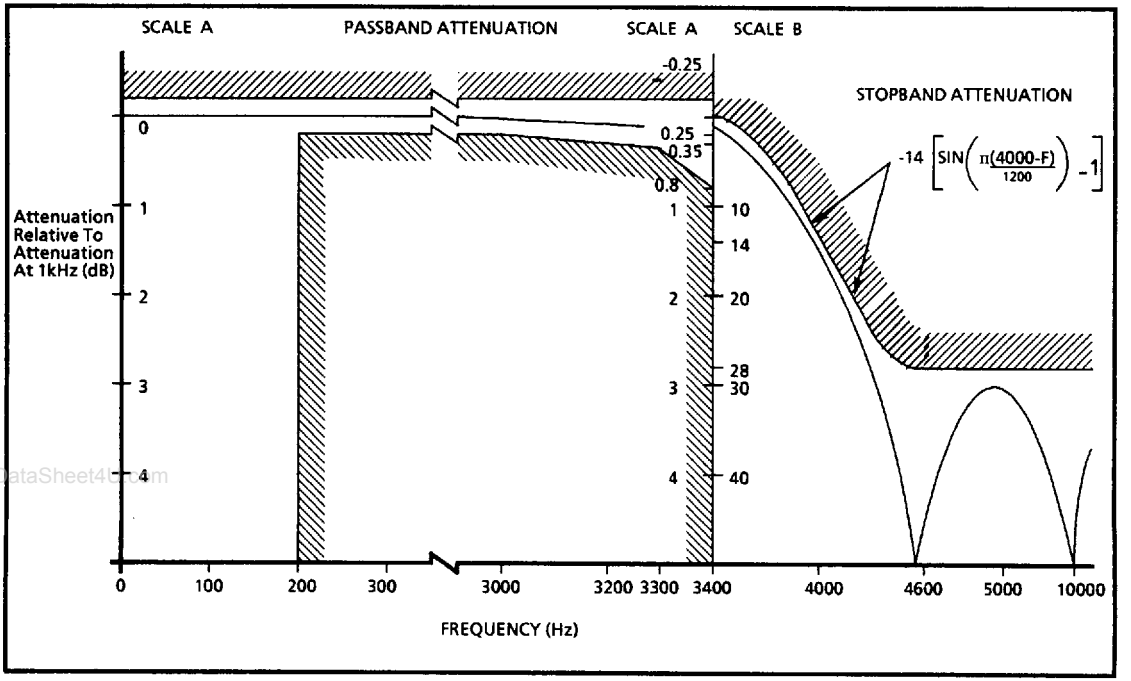

Figure 19 - Attenuation vs Frequency for Receive Filter

Recommended Operating Conditions - Speakerphone†

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Acoustic Separation			40		dB	
2		SPKR+ and SPKR– capacitive load allowed per pin				150	pF	direct speaker connection

† Parameters 1 and 2 are for design aid only and will give optimum results for speakerphone (handsfree) operation.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Recommended Operating Conditions - Handset Microphone

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Sensitivity	S		–40		dBV	Acoustic input of 0 dBPa at 7.6 mm from lip ring at 1000 Hz
2		Output Impedance	Z_{OUT}		1		kΩ	At 1000 Hz
3		Harmonic Distortion	THD		1		%	Between 300 and 3000 Hz with an input level of 0 dBPa
4		External Interface Gain μ-Law ①A-Law	G_{EX}		7.3 16.7		dB dB	

‡ Typical figures are at 25 °C and are for design aid only. Refer to IEEE 269 for artificial mouth calibration procedure.
① Reflects need for higher audio levels typically found in networks for A-Law PCM coding.

Recommended Operating Conditions - Speakerphone Microphone

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Sensitivity	S		-64		dB	(0 dB = 1 V/μbar) input of 1 μbar at 1000 Hz
2	Output Impedance	Z_{OUT}		2.2		kΩ	At 1000 Hz
3	Harmonic Distortion	THD		1		%	Between 300 and 3000 Hz with an input level of 0 dBPa

‡ Typical figures are at 25 °C and are for design aid only.

Recommended Operating Conditions - Handset Speaker

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Efficiency			96.5		dBSPL	Reference frequency 1000 Hz, input signal 81.4 mV_{RMS} (open circuit) and closed loop generator impedance 150Ω
2	Impedance	Z_{HSPK}		150		Ω	Reference1000 Hz
3	Harmonic Distortion	T_{HD}		1		%	Between 300 and 3000 Hz

‡Typical figures are at 25 °C and are for design aid only.

Recommended Operating Conditions - Speakerphone Speaker

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Impedance	Z_{SPK}		40		Ω	At 1000 Hz
2	Harmonic Distortion	T_{HD}		1		%	Between 300 and 3000 Hz

‡Typical figures are at 25 °C and are for design aid only.

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AC Electrical Characteristics - Handset Speaker Driver

	Characteristics		Sym	Min	Typ‡	Max	Units	Test Conditions
1	HSPKR+ and HSPKR− differential gain	μ-Law	G_{DA}	−8.9	−7.9	−6.9	dB	No load
		μ-Law		−14.9	−13.9	−12.9	dB	150 ohm load, See Fig. 4①
		A-Law		−6.6	−5.6	−4.6	dB	No load
		A-Law		−12.6	−11.6	−10.6	dB	150 ohm load, See Fig. 4①
2	Analog voltage across Handset speaker							Receive Gain = 0 dB
		μ-Law		245	275	310	mV_{RMS}	3.17 dBm0 input signal①
		A-Law		331	372	417	mV_{RMS}	3.14 dBm0 input signal①
3	HSPKR+ and HSPKR− drive output							Receive Gain = 0 dB
		μ-Law		402	506	637	μW	3.17 dBm0 input signal①
		A-Law		0.730	0.922	1.159	mW	3.14 dBm0 input signal①
4	Side-tone	μ-Law	S_T		−15		dB	from M± inputs
		A-Law			−21.9		dB	to 150 Ω load

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

① Measurements are made using the test circuit shown in Figure 4, 150 ohm load.

AC Electrical Characteristics - Speakerphone Speaker Driver

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SPKR+ and SPKR– gain			3.8		dB	40 ohm speaker
2	Analog voltage across speakerphone speaker			1.76		V_{RMS}	Receive Filter Gain = 0 dB 40 ohm speaker with 1.57 dBm0 signal (μ-Law)
3	SPKR+ and SPKR– drive output		63	94		mW	Receive Filter Gain = 0 dB 40 ohm speaker with 1.57 dBm0 signal (μ-Law) V_{DD} = 5V, T = 25°C

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Tone Ringer†

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Oscillator Frequency	F_O	15.7		4000	Hz	
2	Frequency Shift Rate	F_S	-	-	-	Hz	10 and 16 Hz only.

† Frequencies are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - Dual Tone Generator†

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Frequency Generated		7.8		1992	Hz	
2	Frequency Resolution		-	-	-	Hz	3.9 Hz Resolution

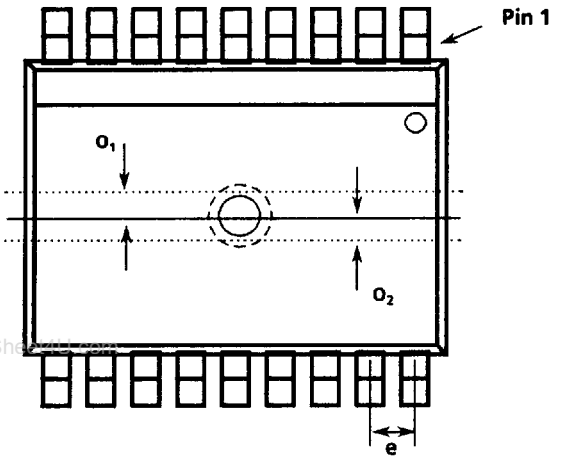
† Frequencies are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

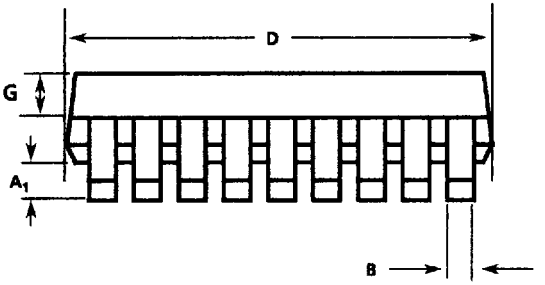
AC Electrical Characteristics - Dual Tone Multi-Frequency Signals Generation†

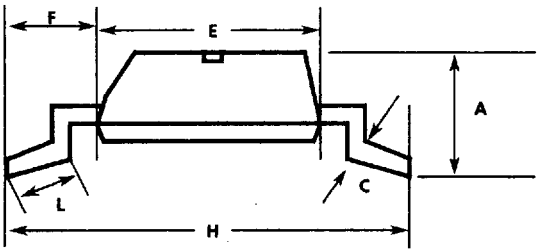
	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Low Frequency 1 Deviation	D_{LF1}		–0.20		%	Nominal = 697 Hz, Actual = 695.3 Hz
2	Low Frequency 2 Deviation	D_{LF2}		+0.40		%	Nominal = 770 Hz, Actual = 773.4 Hz
3	Low Frequency 3 Deviation	D_{LF3}		–0.05		%	Nominal = 852 Hz, Actual = 851.6 Hz
4	Low Frequency 4 Deviation	D_{LF4}		–0.37		%	Nominal = 941 Hz, Actual = 937.5 Hz
5	High Frequency 1 Deviation	D_{HF1}		+0.20		%	Nominal = 1209 Hz, Actual = 1210.9 Hz
6	High Frequency 2 Deviation	D_{HF2}		0.0		%	Nominal = 1336 Hz, Actual = 1335.9 Hz
7	High Frequency 3 Deviation	D_{HF3}		–0.03		%	Nominal = 1477 Hz, Actual = 1476.6 Hz
8	High Frequency 4 Deviation	D_{HF4}		–0.01		%	Nominal = 1633 Hz, Actual = 1632.8 Hz
9	Negative Twist	dBp		2.5		dB	
10	Output Power μ-Law A-Law	P_{OUT}		–4.0 –9.9		dBm0 dBm0	PCM Output Level
11	Distortion	THD		–25		dB	

† Frequencies are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

PACKAGING OUTLINES



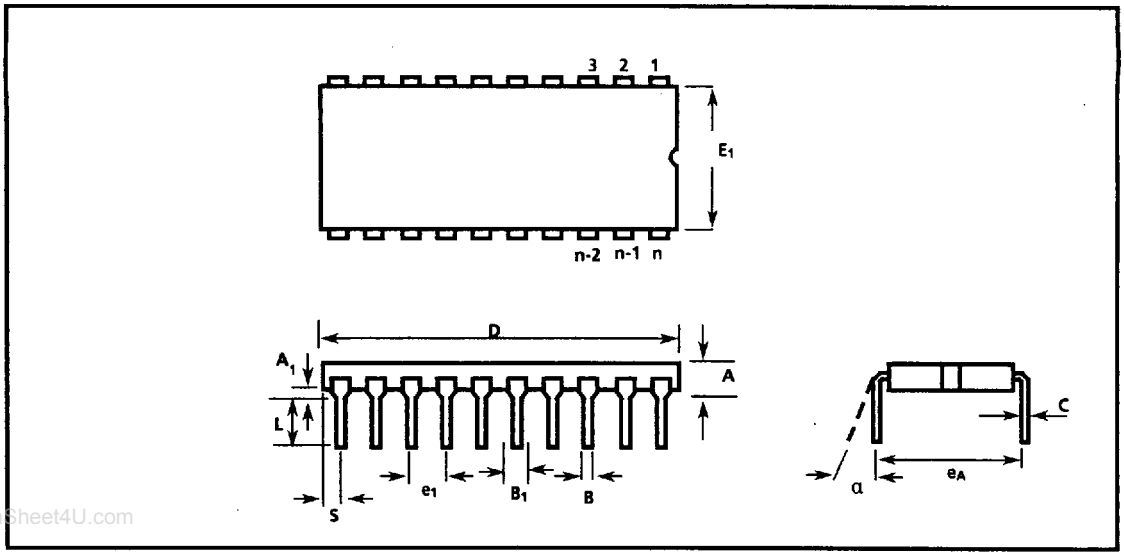




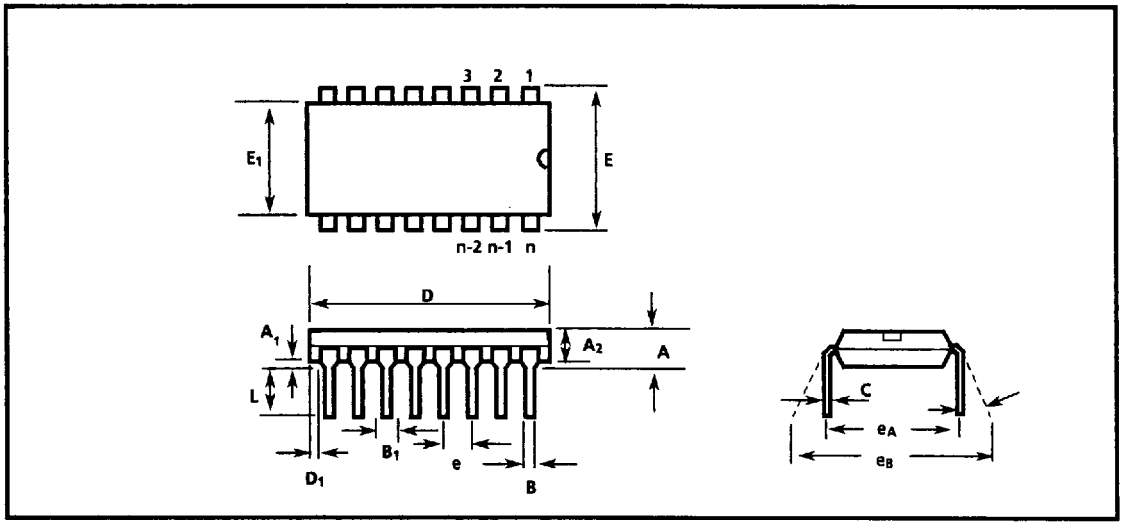
DIM	16-Pin SOIC		18-Pin SOIC		20-Pin SOIC	
	Min	Max	Min	Max	Min	Max
A	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)
A_1	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)
B	0.014 (0.351)	0.019 (0.488)	0.014 (0.351)	0.019 (0.488)	0.014 (0.351)	0.019 (0.488)
C	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)
D	0.398 (10.1)	0.413 (10.5)	0.447 (11.35)	0.469 (11.90)	0.496 (12.60)	0.518 (13.00)
E	0.291 (7.40)	0.305 (7.75)	0.291 (7.40)	0.305 (7.75)	0.291 (7.40)	0.305 (7.75)
e	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
F	0.044 (1.125)	0.064 (1.625)	0.044 (1.125)	0.064 (1.625)	0.044 (1.125)	0.064 (1.625)
G	0.040 (1.016)	0.050 (1.270)	0.040 (1.016)	0.050 (1.270)	0.040 (1.016)	0.050 (1.270)
H	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)
L	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)
O_1	-	0.005 (0.13)	-	0.005 (0.13)	-	0.005 (0.13)
O_2	-	0.005 (0.13)	-	0.005 (0.13)	-	0.005 (0.13)

NOTES:
1) A & B Maximum dimensions include allowable mold flash.
2) O_1 & O_2 are SYMMETRY dimensions.

Lead SOIC Package (S Suffix)



Ceramic Dual-In-Line Packages (CDIP) - C Suffix



Plastic Dual-In-Line Packages (PDIP) - E Suffix

Package Outlines

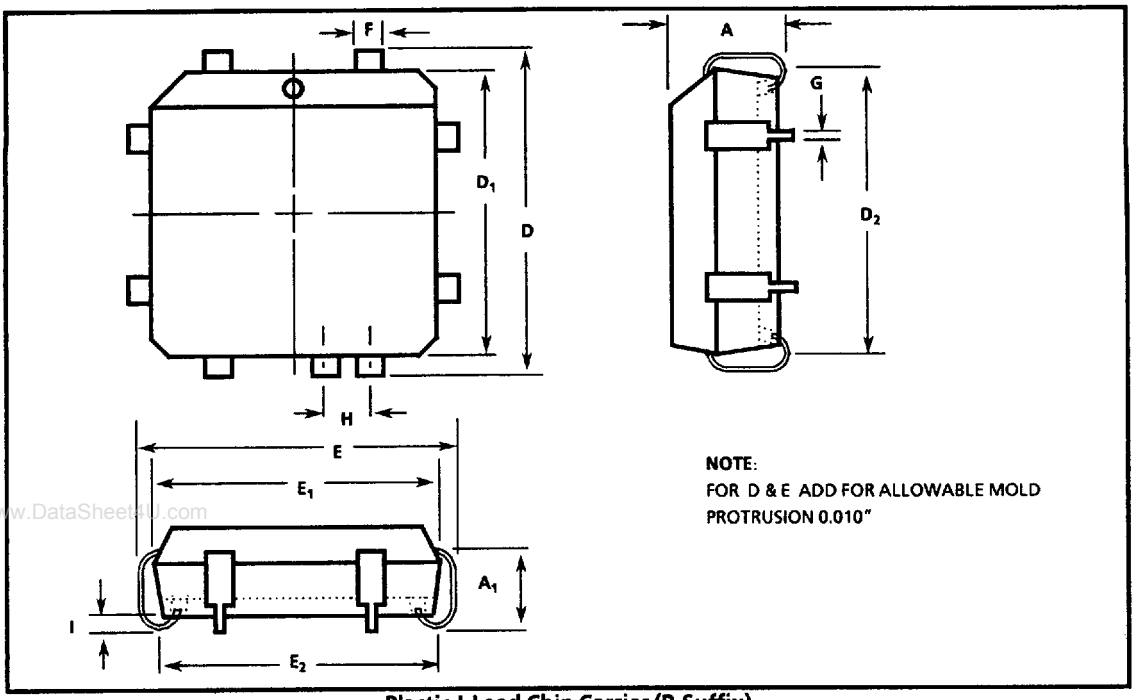
DIM	8-Pin				16-Pin				18-Pin				20-Pin			
	Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)
A_1			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)
A_2	0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)
B_1	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	0.348 (8.84)	0.430 (10.92)	0.380 (9.7)	0.550 (13.9)	0.745 (18.93)	0.840 (21.33)		0.784 (19.9)	0.845 (21.47)	0.925 (23.49)	0.880 (22.36)	0.930 (23.62)	0.925 (23.49)	1.060 (26.9)		0.996 (25.3)
D_1	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)		
E_1	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e_1			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
e_A	0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (2.54 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)	
e_B		0.430 (10.92)				0.430 (10.92)				0.430 (10.92)				0.430 (10.92)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters

DIM	22-Pin				24-Pin				28-Pin				40-Pin			
	Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)	0.090 (2.29)	0.225 (5.71)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)
A_1			0.025 (0.64)	0.055 (1.39)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)
A_2	0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)
B_1	0.045 (1.15)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	1.050 (26.67)	1.120 (28.44)	1.040 (26.42)	1.260 (32.0)	1.150 (29.3)	1.290 (32.7)	1.180 (29.88)	1.291 (32.80)	1.380 (35.1)	1.565 (39.7)	1.380 (35.06)	1.520 (38.61)	1.980 (50.3)	2.095 (53.2)	1.980 (50.30)	2.110 (53.60)
D_1	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.390 (9.91)	0.430 (10.92)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)		
E_1	0.330 (8.39)	0.380 (9.65)	0.350 (8.89)	0.410 (10.41)	0.485 (12.32)	0.580 (14.73)	0.516 (13.11)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.618 (15.70)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e_1			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
e_A	0.400 BSC (10.16 BSC)		0.400 BSC (10 .16 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)	
e_B		0.500 (12.70)				0.700 (17.78)				0.700 (17.78)				0.700 (17.78)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.100 (2.54)				0.800 (2.05)				0.800 (2.05)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters

Package Outlines



Plastic J-Lead Chip Carrier (P-Suffix)

DIM	20-Pin PLCC		28-Pin PLCC		44-Pin PLCC		68-Pin PLCC		84-Pin PLCC	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.200 (5.08)	0.165 (4.20)	0.200 (5.08)
A_1	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.130 (3.30)	0.090 (2.29)	0.130 (3.30)
B			0.020 TP (0.511 TP)							
B_1										
B_2										
D/E	0.385 (9.78)	0.395 (10.03)	0.485 (12.32)	0.495 (12.57)	0.685 (17.40)	0.695 (17.65)	0.985 (25.02)	0.995 (25.27)	0.185 (30.10)	1.195 (30.35)
D_1/E_1	0.350 (8.890)	0.356 (9.042)	0.450 (11.430)	0.456 (11.582)	0.650 (16.510)	0.656 (16.662)	0.950 (24.130)	0.958 (24.333)	1.150 (29.210)	1.158 (29.413)
D_2/E_2	0.290 (7.37)	0.330 (8.38)	0.390 (9.91)	0.430 (10.92)	0.590 (14.99)	0.630 (16.00)	0.890 (22.61)	0.930 (23.62)	1.090 (27.69)	1.130 (28.70)
D_4/E_4										
e			0.050 BSC (1.27 BSC)							
F	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)
G	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)
H	0.050 BSC (1.27 BSC)				0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
h										
h_1										
I	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	
L										
L_1										
R_1										

NOTE: ( ) Millimeters