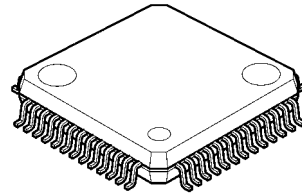


Multi Input Wide Band Video Interface with I²C Control

■ GENERAL DESCRIPTION

NJW1328 is a multi input wide band video interface IC with I²C control. Also the **NJW1328** includes 7-input 2 channel video switch for CVBS, isolation amplifier for CVBS, 3-input 1 channel video switch for Component Video Signal, 2 channel 75-ohm driver for CVBS and 1 channel 75-ohm driver for Component Video Signal. **NJW1328** is suitable for video equipment that has multi input and multi output.

■ PACKAGE OUTLINE

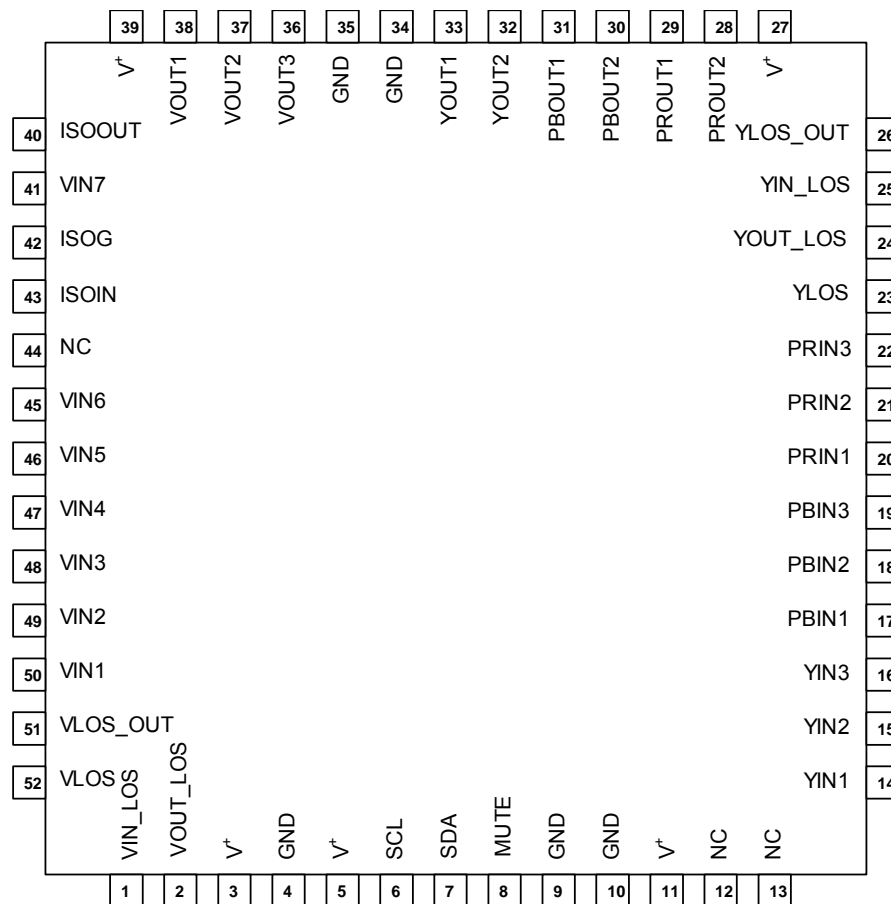


NJW1328FH2

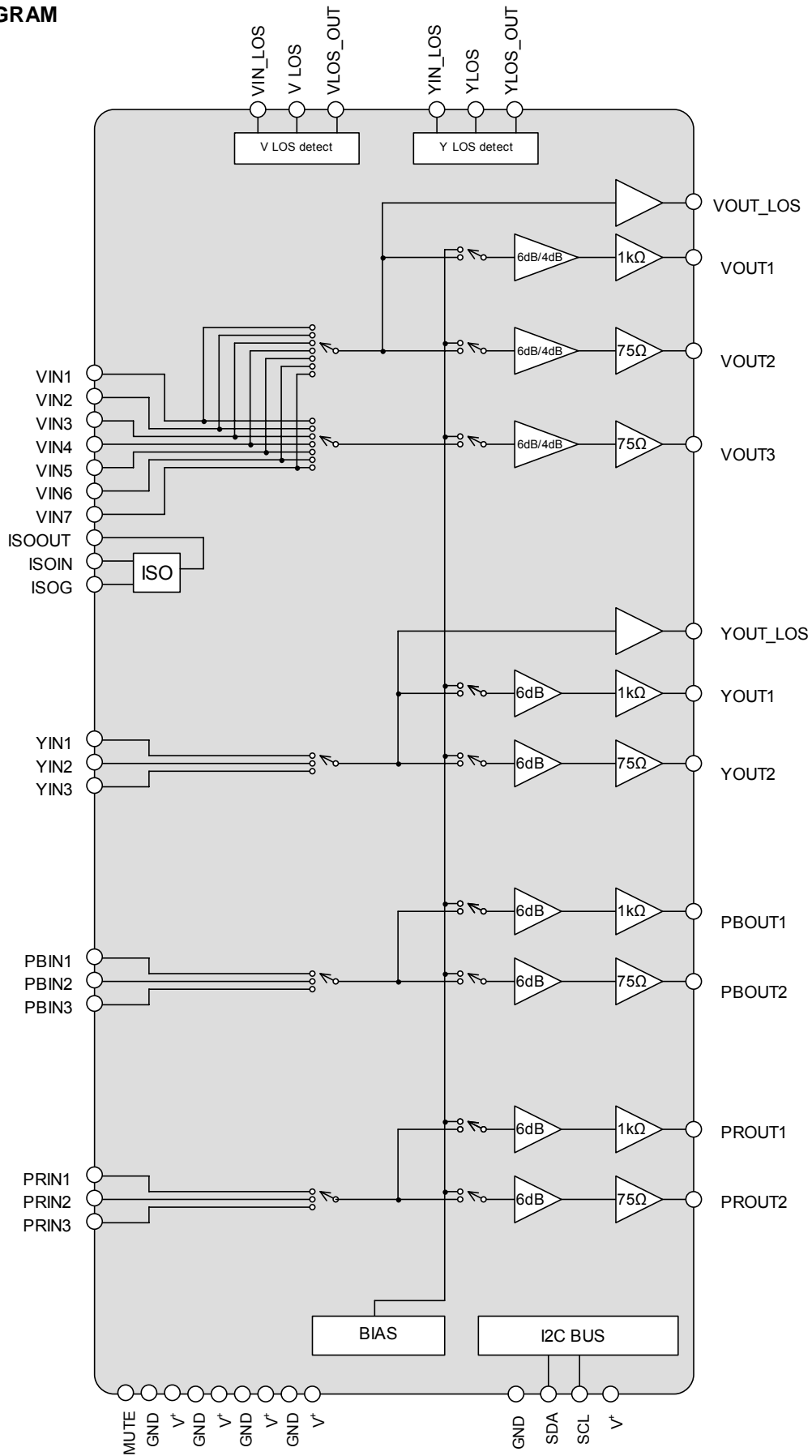
■ FEATURES

- Operating Voltage Single Supply 4.5 to 5.5V
- 7-input 2 channel video switch for CVBS
- 3-input 1 channel video switch for Component Video Signal
- Ground ISO (Isolation) amplifier for CVBS
- 2 channel 75-ohm driver for CVBS
- 1 channel buffer for CVBS
- 1 channel 75-ohm driver for Component Video Signal
- 1 channel buffer for Component Video Signal
- 1 channel LOS (Loss Of Signal) detector for each CVBS and Component Video Signal
- I²C BUS control
- LQFP52-H2

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	7.0	V
Power Dissipation	P _D	1900 ^{NOTE)}	mW
Operating Temperature Range	Topr	-20 to +75	°C
Storage Temperature Range	Tstr	-40 to +150	°C

(Note) At on a board of EIA/JDAC specification. (114.3 x 76.2 x 1.6mm Two layers,FR-4)

■ RECOMMEND OPERATING VOLTAGE

(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	Vopr	V ⁺ - GND	4.5	5.0	5.5	V

■ ELECTRICAL CHARACTERISTICS

● Power Supply Characteristics

(TEST CONDITION: Ta=25°C, V⁺= 5.0V all controls unless otherwise specified)

● DC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I _{CC}	V ⁺ , No Signal	-	65	100	mA
Operating Current at power save mode	I _{save}	V ⁺ , Power Save Mode	-	1.0	3.0	mA

● AC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Output Voltage	V _{OM}	Input sine signal voltage (100kHz), THD=1%	2.4	-	-	Vp-p
Voltage Gain 1	Gv1	Input sine signal (100kHz, 1.0Vp-p),4dB mode	3.5	4.0	4.5	dB
Voltage Gain 2	Gv2	Input sine signal (100kHz, 1.0Vp-p),6dB mode	5.5	6.0	6.5	dB
Voltage Gain 3	Gv3	Input sine signal (100kHz, 1.0Vp-p) for ISO output terminal	-0.5	0.0	0.5	dB
Frequency Characteristic 1	Gf1	Input sine signal (12MHz/100kHz, 1.0Vp-p) 6dB mode for V input terminal	-3.0	0.0	-	dB
Frequency Characteristic 2	Gf2	Input sine signal (6MHz/100kHz, 1.0Vp-p) 6dB mode for ISO input terminal	-3.0	0.0	-	dB
Frequency Characteristic 3	Gf3	Input sine signal (100MHz/100kHz, 1.0Vp-p) 6dB mode for Y/PB/PR input terminal	-	-3.0	-	dB
Frequency Characteristic 4	Gf4	Input sine signal (150MHz/100kHz, 100mVp-p) 6dB mode for Y/PB/PR input terminal	-	-3.0	-	dB
Cross Talk between Input terminals	CT	Input sine signal (3.58MHz, 1.0Vp-p)	-	-60	-50	dB
Differential Gain	DG	Input Video signal (1.0Vp-p, 10step)	-	0.5	-	%
Differential Phase	DP	Input Video signal (1.0Vp-p, 10step)	-	0.5	-	deg
Signal Detective Voltage	Vdet	Input Square pulse (16kHz, 4.7μs)	-	200	-	mVp-p
Common Mode Rejection Ratio	CMRR	Input sine signal (20kHz, 1.0Vp-p)	-	-55	-	dB
Output/output voltage difference on mute mode	dVDo	On mute mode	-0.4	-	0.4	V
S/N ratio	SNv	Input White Video signal (1.0Vp-p, 100%) for V/Y/PB/PR input terminal	-	75	-	dB

NJW1328

● AC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Switch Change Over Voltage (H level)	VthH		2.0	-	V ⁺	V
Switch Change Over Voltage (L level)	VthL		0	-	1.0	V
Maximum inflow current on Switch ON	IthH	V=5.0V	-	-	120	uA
Maximum inflow current on Switch OFF	IthL	V=0.3V	-	-	8	uA

■ MUTE CONTROL

NJW1328 performs Mute for all output voltages simultaneously with MUTE terminal.

MUTE TERMINAL VOLTAGE	OPERATION
<VthL	MUTE ON
>VthH	MUTE OFF

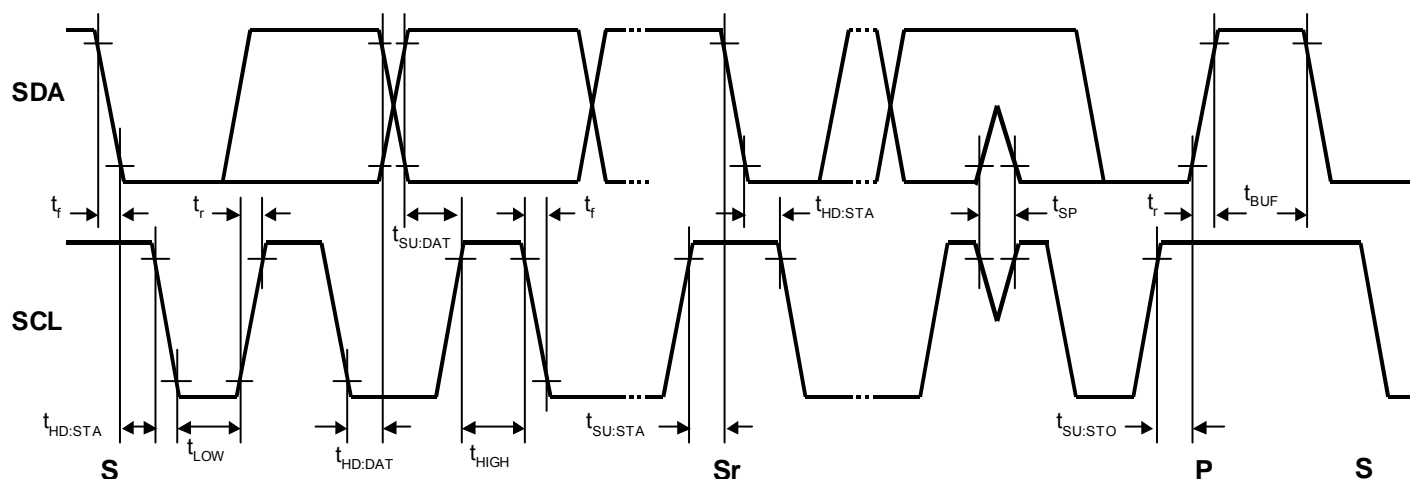
■ SIGNAL DETECTION

NJW1328 detects a signal that is larger than Signal Detective Voltage (SDV).

INPUT SIGNAL VOLTAGE	LOS_OUT	CONDITION
Vdet > V _{IN}	H	Signal is smaller than SDV
Vdet < V _{IN}	L	Signal is larger than SDV

NOTE) If you input a signal except for video signal with sync, there is the case that output of LOS_OUT terminal is not stable.

■ TIMING on the I²C BUS (SDA, SCL)



■ CHARACTERISTICS OF I/O STAGES FOR I²C BUS (SDA, SCL)

I²C BUS Load Conditions

STANDARD MODE: Pull up resistance 4kΩ (Connected to V⁺), Load capacitance 200pF (Connected to GND)

HIGH-SPEED MODE: Pull up resistance 4kΩ (Connected to V⁺), Load capacitance 50pF (Connected to GND)

PARAMETER	SYMBOL	STANDARD MODE			HIGH-SPEED MODE			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V _{IL}	0.0	-	0.3V ⁺	0.0	-	0.3V ⁺	V
High Level Input Voltage	V _{IH}	0.7V ⁺	-	5.5	0.7V ⁺	-	5.5	V
Low Level Output Voltage (3mA at SDA pin)	V _{OL}	0	-		0	-	0.4	V
Input current each I/O pin with an input voltage between 0.1V _{cc} and 0.9V _{cc}	I _i	-10	-	10	-10	-	10	μA

■ CHARACTERISTICS OF BUS LINES (SDA, SCL) FOR I²C BUS DEVICES

PARAMETER	SYMBOL	STANDARD MODE			HIGH-SPEED MODE			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
SCL clock frequency	f_{SCL}	-	-	100	-	-	400	kHz
HOLD time	$t_{HD:STA}$	4.0	-	-	0.6	-	-	μ s
Low period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	μ s
High period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	μ s
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	-	0.6	-	-	μ s
Data Hold Time ^(NOTE)	$t_{HD:DAT}$	0	-	-	0	-	-	μ s
Data set-up Time	$t_{SU:DAT}$	250	-	-	100	-	-	ns
Rise time of both SDA and SCL signals	t_r	-	-	1000	-	-	300	ns
Fall time of both SDA and SCL signals	t_f	-	-	300	-	-	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	-	0.6	-	-	μ s
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	μ s
Capacitive load for each bus line	C_b	-	-	400	-	-	400	pF
Noise margin at the Low level	V_{nL}	0.5	-	-	0.5	-	-	V
Noise margin at the High level	V_{nH}	1	-	-	1	-	-	V

C_b ; total capacitance of one bus line in pF

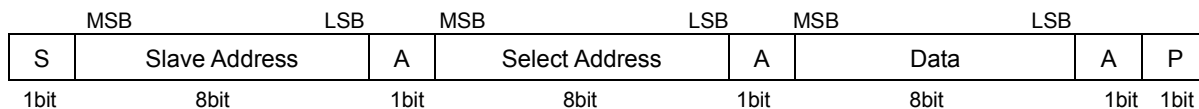
NOTE) Data hold time: $t_{HD:DAT}$

Please hold the Data Hold Time ($t_{HD:DAT}$) to 300ns or more to avoid status of unstable at SCL falling edge.

■ DEFINITION OF I²C REGISTER

You can send and transmit address by I²C REGISTER with SDA input and SCL input.

• I²C BUS FORMAT



S: Starting term

A: Acknowledge bit

P: Ending term

• SLAVE ADDRESS

Slave Address								Hex
MSB				LSB				-
1	0	0	1	0	1	1	0	96(h)

NJW1328 is not suitable for read mode.

• CONTROL REGISTER TABLE

The auto increment function cycles the select address as follows.

00H → 01H → 00H

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	VOUT1,2 Select			VOUT3 Select			VOUT1,2 Gain	VOUT3 Gain
01H	VOUT1 Mute	VOUT2 Mute	VOUT3 Mute	YOUT/PBOUT/PROUT Select		YOUT1/PBOUT1/PROUT1 Mute	YOUT2/PBOUT2/PROUT2 Mute	Power Save

■ CONTROL REGISTER INITIAL VALUE

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	0

■ INSTRUCTION CODE

a)

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	VOUT1,2 Select			VOUT3 Select			VOUT1,2 Gain	VOUT3 Gain

•VOUT1,2 SIGNAL SELECT TABLE

VOUT1,2 Select			VOUT1,2
D7	D6	D5	
0	0	0	VIN1*
0	0	1	VIN2
0	1	0	VIN3
0	1	1	VIN4
1	0	0	VIN5
1	0	1	VIN6
1	1	0	VIN7

*Default Value

•VOUT3 SIGNAL SELECT TABLE

VOUT3 Select			VOUT3
D4	D3	D2	
0	0	0	VIN1*
0	0	1	VIN2
0	1	0	VIN3
0	1	1	VIN4
1	0	0	VIN5
1	0	1	VIN6
1	1	0	VIN7

*Default Value

•VOUT1,2 GAIN SELECT TABLE

VOUT Gain	Gain
D1	
0	4dB*
1	6dB

*Default Value

•VOUT3 GAIN SELECT TABLE

VOUT Gain	Gain
D0	
0	4dB*
1	6dB

*Default Value

■ INSTRUCTION CODE

b)

No.	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
01H	VOUT1 Mute	VOUT2 Mute	VOUT3 Mute	YOUT/PBOUT/ PROUT Select		YOUT1/ PBOUT1/ PROUT1 Mute	YOUT2/ PBOUT2/ PROUT2 Mute	Power Save

•VOUT1 SIGNAL Mute/Through SELECT TABLE

VOUT1 Mute	VOUT1
D7	
0	Mute*
1	Through

*Default Value

•VOUT2 SIGNAL Mute/Through SELECT TABLE

VOUT2 Mute	VOUT2
D6	
0	Mute*
1	Through

*Default Value

•VOUT3 SIGNAL Mute/Through SELECT TABLE

VOUT3 Mute	VOUT3
D5	
0	Mute*
1	Through

*Default Value

•YOUT/PBOUT/PROUT SIGNAL SELECT TABLE

YOUT/PBOUT/ PROUT Select		YOUT	PBOUT	PROUT
D4	D3			
0	0	YIN1*	PBIN1*	PRIN1*
0	1	YIN2	PBIN2	PRIN2
1	0	YIN3	PBIN3	PRIN3

*Default Value

•YOUT1/PBOUT1/PROUT1 SIGNAL Mute/Through SELECT TABLE

YOUT1/PBOUT1/ PROUT1 Mute	YOUT1/PBOUT1/ PROUT1
D2	
0	Mute*
1	Through

*Default Value

•YOUT2/PBOUT2/PROUT2 SIGNAL Mute/Through SELECT TABLE

YOUT2/PBOUT2/ PROUT2 Mute	YOUT2/PBOUT2/ PROUT2
D1	
0	Mute*
1	Through

*Default Value

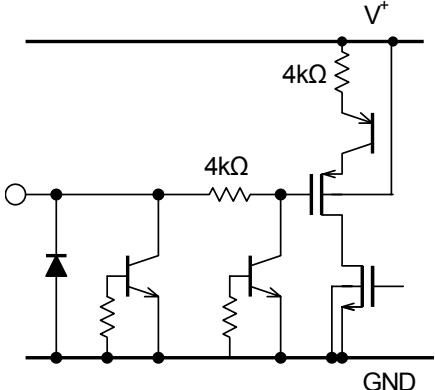
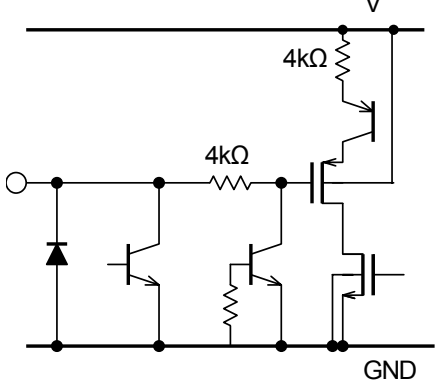
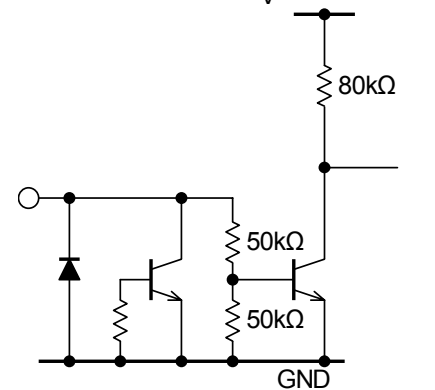
•POWER SAVE SELECT TABLE

Power Save	Power Save
D0	
0	Power Save Mode*
1	Normal Mode

*Default Value

■ TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
1 25	VIN_LOS YIN_LOS	V Input for LOS Y Input for LOS		3.1V
2 24	VOUT_LOS YOUT_LOS	V output for LOS Y output for LOS		1.9V
3 5 11 27 39	V ⁺ 1 V ⁺ 2 V ⁺ 3 V ⁺ 4 V ⁺ 5	Supply		5V
4 9 10 34 35	GND	Ground		0V

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
6	SCL	I ² C Clock Input	 <p>The diagram shows the internal circuitry of the SCL pin. It includes a pull-up resistor of 4kΩ connected to V⁺. The input signal is connected to a network of transistors and resistors. A 4kΩ resistor is connected between the input and the base of a transistor. The circuit also features a diode connected to ground, another transistor, and a resistor connected to the base of a second transistor. The output of this second transistor is connected to the base of a third transistor, which is also connected to V⁺ through a 4kΩ resistor. The emitter of this third transistor is connected to GND.</p>	-
7	SDA	I ² C Data Input	 <p>The diagram shows the internal circuitry of the SDA pin. It includes a pull-up resistor of 4kΩ connected to V⁺. The input signal is connected to a network of transistors and resistors. A 4kΩ resistor is connected between the input and the base of a transistor. The circuit also features a diode connected to ground, another transistor, and a resistor connected to the base of a second transistor. The output of this second transistor is connected to the base of a third transistor, which is also connected to V⁺ through a 4kΩ resistor. The emitter of this third transistor is connected to GND.</p>	-
8	MUTE	Mute	 <p>The diagram shows the internal circuitry of the MUTE pin. It includes a pull-up resistor of 80kΩ connected to V⁺. The input signal is connected to a network of transistors and resistors. A 50kΩ resistor is connected between the input and the base of a transistor. The circuit also features a diode connected to ground, another transistor, and a resistor connected to the base of a second transistor. The output of this second transistor is connected to the base of a third transistor, which is also connected to V⁺ through a 50kΩ resistor. The emitter of this third transistor is connected to GND.</p>	-

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
50 49 48 47 46 45 41 14 15 16	VIN1 VIN2 VIN3 VIN4 VIN5 VIN6 VIN7 YIN1 YIN2 YIN3	V Input Y Input		1.9V
17 18 19 20 21 22	PBIN1 PBIN2 PBIN3 PRIN1 PRIN2 PRIN3	Pb Input Pr Input		2.5V
52 23	VLOS YLOS	V LOS Detect Filter Y LOS Detect Filter		-

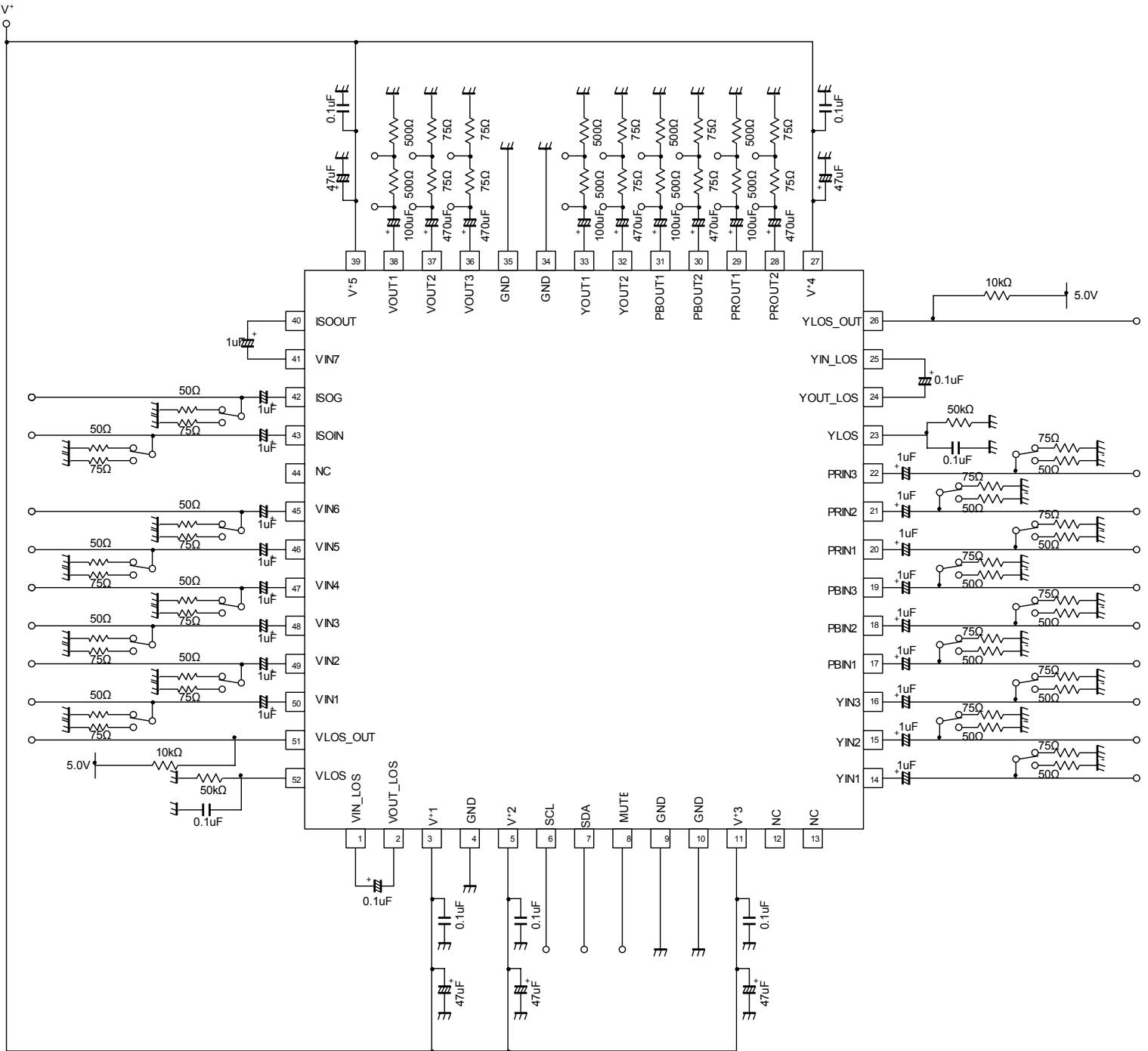
No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
51 26	VLOS_OUT YLOS_OUT	VLOS Output YLOS Output		-
30 28	PBOUT2 PROUT2	Pb Output Pr Output For 75Ω Drive		2.5V
33 31 29	YOUT1 PBOUT1 PROUT1	Y Output Pb Output Pr Output With load resistance 1kΩ		1.3V 2.5V 2.5V

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
32	YOUT2	Y Output For 75Ω Drive		1.3V
37 36	VOUT2 VOUT3	V Output For 75Ω Drive		1.3V
38	VOUT1	V Output With load resistance 1kΩ		1.3V

No.	SYMBOL	FUNCTION	EQUIVALENT CIRCUIT	VOLATGE
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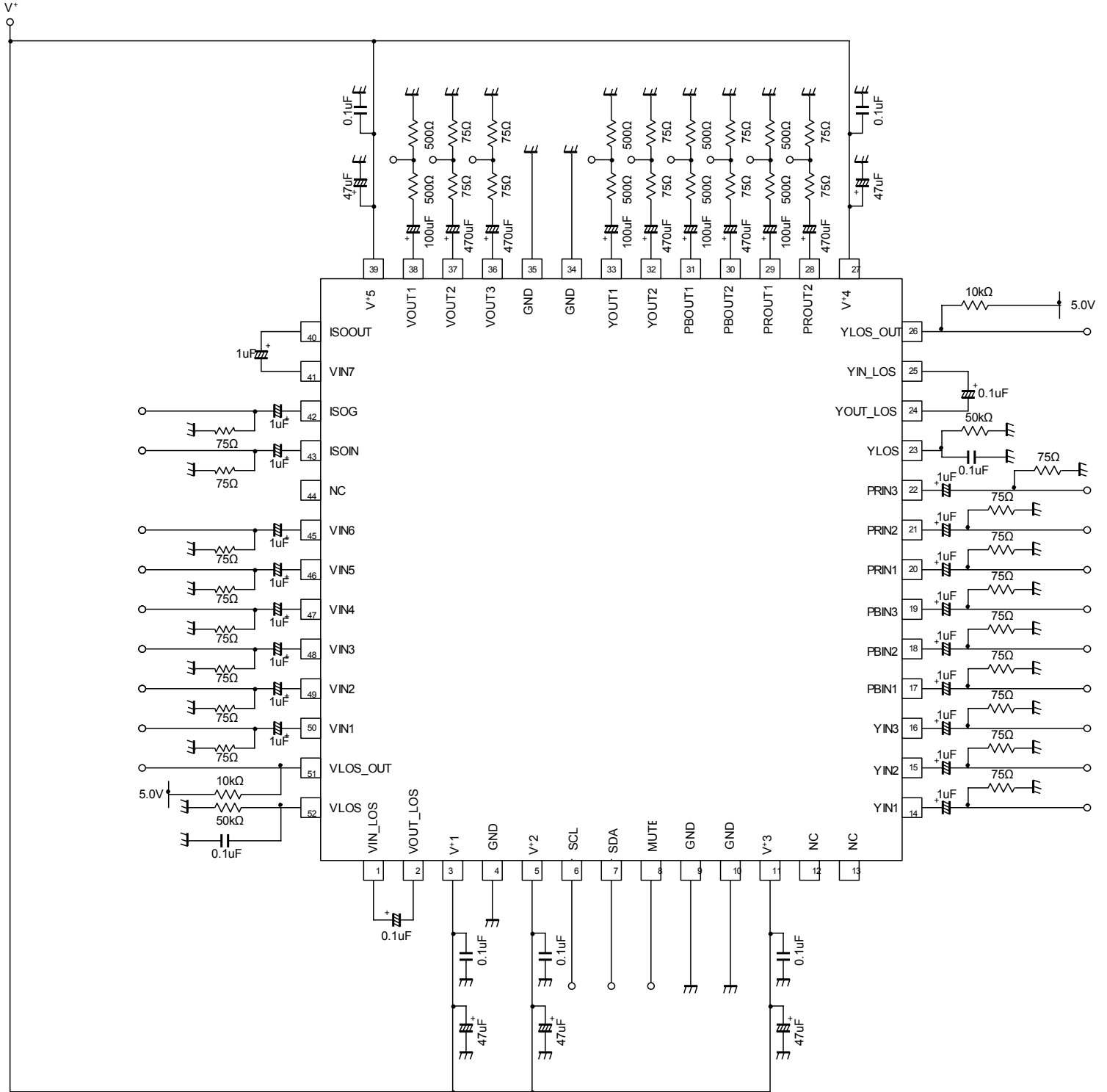
40	ISOOUT	Isolation Output		2.9V
43 42	ISOIN ISOG	Isolation Input Isolation Ground Input		2.9V

TEST CIRCUIT



NJW1328

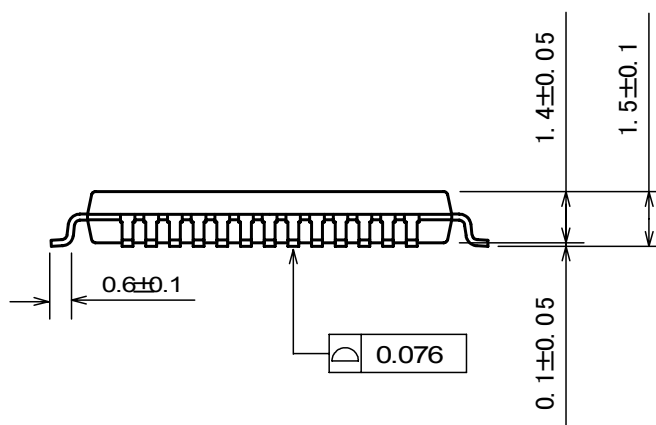
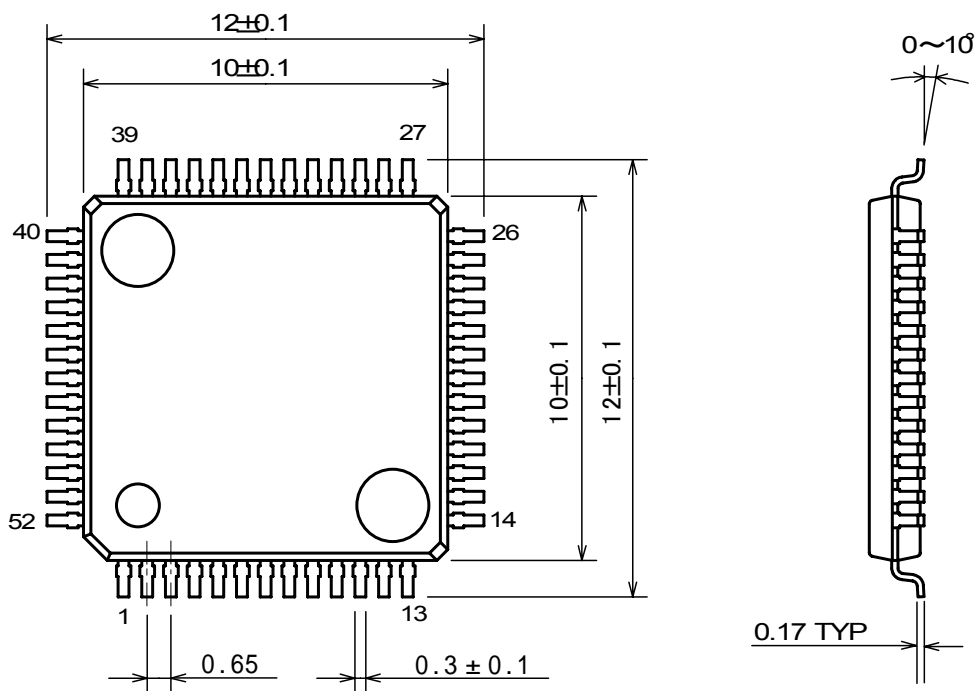
APPLICATION CIRCUIT



EXTERNAL DIMENSIONS

LQFP52-H2

Unit : mm



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