SSI 35P550
4-Channel Magnetic Tape Read Device

July, 1990

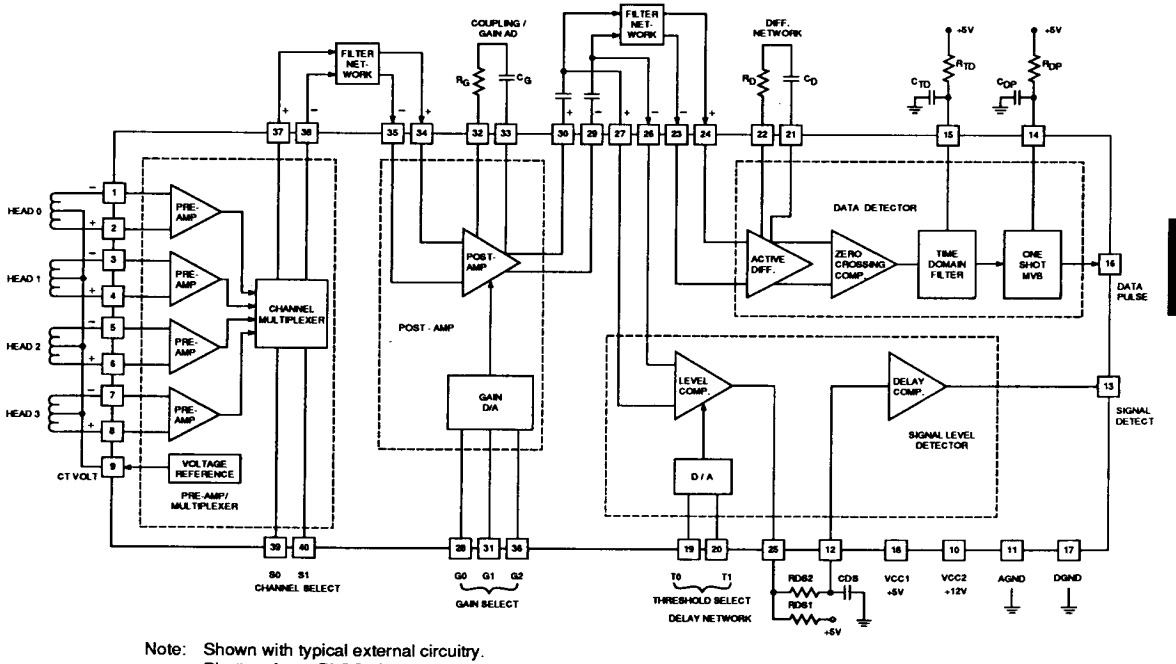
DESCRIPTION

Silicon Systems' SSI 35P550 combines magnetic tape head read signal amplification and processing onto a single integrated circuit. The device accepts up to 4 center-tapped magnetic read heads connected directly to the head inputs; head center tap voltage is provided by an on-chip reference. The device architecture permits system design flexibility by providing the external connections between the Preamplifier/Multiplexer, Postamplifier, Signal Level Detector, and Data Detector; this allows the implementation of many suitable filtering combinations. Low noise amplifiers are used throughout the device. The SSI 35P550 operates on +5 and +12 Volt supplies and has TTL compatible control signals.

FEATURES

- **4-Channel Multiplexer with differential-input Preamplifiers**
- **Postamplifier has component-adjustable and programmable gain**
- **On-chip Signal Level Detector with programmable threshold and adjustable delay**
- **Data Detection Circuit includes spurious signal rejection (adjustable time domain filter) and provides an adjustable uniform Data Pulse output**
- **Available in 40-pin DIP or 44-pin PLCC plastic packages**

BLOCK DIAGRAM



Note: Shown with typical external circuitry.
Pin #s refer to PLCC pinout.

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

4-CHANNEL PREAMPLIFIER AND MULTIPLEXER

The device contains four low level differential-input Preamplifiers. The differential output of a single Preamplifier is selectively connected to the Preamplifier output terminals by means of two logical CHANNEL SELECT signals, S0 and S1. The selected Preamplifier number is the binary value of the logical SELECT signals for active high voltage levels.

The Preamplifier inputs are intended for connection to center-tapped magnetic read heads. An appropriate Preamplifier input bias voltage level is obtained by connecting the head center taps to the circuit C.T. VOLT terminal.

The C.T. VOLT terminal is the output of a voltage reference which has a value to center the Preamplifier inputs within their operating range.

POSTAMPLIFIER

The Postamplifier is a differential-input, differential-output circuit which has two means of gain adjustment. A continuously-variable gain adjustment is obtained by use of an external resistor or potentiometer. Discrete values of gain setting are additionally obtained by applying combinations of logical signal levels to the three GAIN SELECT terminals, G0, G1, and G2.

The Postamplifier receives the output signals of the Preamplifier after frequency selection by an external filter network. The input characteristics of the Postamplifier are such that the inputs may have DC coupling to the Preamplifier output, or may be AC coupled with proper bias of 3V nom.

A suitable coupling capacitor must be connected between the GAIN1, GAIN2 terminals independent of the use of a gain setting resistor.

SIGNAL LEVEL DETECT CIRCUITS

The Signal Level Detect circuits consist of detector circuits which compare the amplitude of the signal envelope of the Postamplifier output with a selectable threshold and provide a logical output level which indicates the presence of Postamplifier signal greater than the threshold. AC coupling is required between the Postamplifier output and the Signal Level Detect circuits input. The Signal Level Detect input has internal bias connections so that no external bias network is required.

The threshold to which the Postamplifier signals are compared is selected by means of two THRESHOLD SELECT logical inputs T0 and T1. The result of the comparison is delayed from appearing at the circuit SIGNAL DETECT output terminal by means of a delay circuit which is adjustable by means of external components. The delay associated with signal detection is set by combinations of capacitor CDS and resistor RDS1. The delay associated with signal loss is set by combinations of CDS and resistors RDS1 plus RDS2.

DATA DETECTION CIRCUITS

The Data Detection circuits are AC coupled to the Postamplifier outputs through an (optional) external filter network and provide logical output pulse signals in response to positive and negative input signal amplitude peaks. This function is performed by differentiating input signals to obtain zero-crossing voltages at points of inflection and detecting these crossings to provide output signals.

To enhance the signal peak detection, spurious inflection points which occur in pairs between true signal peaks are suppressed by means of the Time Domain Filter. The filter inhibits the propagation of detected zero-crossings if they are not sufficiently separated in time. This time period is set by external capacitor CTD and resistor RTD.

Uniform DATA PULSE output signals are provided by the One-Shot Multivibrator which is triggered by outputs of the Time Domain Filter. The time duration of the DATA PULSE signals is set by external capacitor CDP and RDP.

DC paths through the external filter network to the Signal Level Detect circuits inputs are required to properly bias the Data Detection circuits. The resistance of each path is not critical and may be as large as 10 kΩ.

PIN DESCRIPTION

NAME	40-PIN	44-PIN	DESCRIPTION
IN0 -	1	1	Channel 0 (-) input
IN0 +	2	2	Channel 0 (+) input
IN1 -	3	3	Channel 1 (-) input
IN1 +	4	4	Channel 1 (+) input
IN2 -	5	5	Channel 2 (-) input
N/C		6	No internal connection
IN2 +	6	7	Channel 2 (+) input
IN3 -	7	8	Channel 3 (-) input
IN3 +	8	9	(+) input
CT VOLT	9	10	Center tap voltage
VCC2	10	11	+ 12 Volt supply connection
AGND	11	12	Analog signal ground
DEL IN	12	13	Input to delay comparator
SIGNAL DETECT	13	14	Output of delay comparator
DPN	14	15	External RC for output pulse width
TDF	15	16	External RC for time-domain delay
N/C		17	No internal connection
DATA PULSE	16	18	Output of time-domain filter
DGND	17	19	Ground
VCC1	18	20	+5 Volt supply
T0	19	21	Threshold select signal (1 of 2)
T1	20	22	Threshold select signal (1 of 2)
CAP1	21	23	External differentiating capacitor connection
CAP2	22	24	
DIF -	23	25	Inputs to active differentiator
DIF +	24	26	
LEV OUT	25	27	Output to level detector
N/C		28	No internal connection
LEV -	26	29	Inputs to level detector
LEV +	27	30	
G0	28	31	Postamp gain select (1 of 3)

PIN DESCRIPTION (Continued)

NAME	40-PIN	44-PIN	DESCRIPTION
PSTOUT -	29	32	Outputs of Postamplifier
PSTOUT +	30	33	
G1	31	34	Postamp gain select (1 of 3)
GAIN 1	32	35	External Postamplifier gain adjusting RC terminals
GAIN 2	33	36	
PSTIN +	34	37	Inputs to Postamplifier
PSTIN -	35	38	
N/C		39	No internal connection
G2	36	40	Postamp gain select (1 of 3)
PREOUT +	37	41	(+) Output of Preamplifier
PREOUT -	38	42	(-) Output of Preamplifier
S0	39	43	Input channel select (1 of 2)
S1	40	44	Input channel select (1 of 2)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature	0 to 130	°C
Supply Voltage, VCC1	-0.5 to +6.0	VDC
Supply Voltage, VCC2	-0.5 to +14.0	VDC
Voltage Applied to Logic Inputs	-0.5 to VCC1 +0.5	VDC
Voltage Applied to OFF Logic Outputs	-0.5 to VCC1 +0.5	VDC
Current Into ON Logic Outputs	5.0	mA
Lead Temperature (soldering, 10 sec)	+260	°C

DC CHARACTERISTICS
(Unless otherwise specified, VCC1 = 4.75V to 5.25V, VCC2 = 11.4V to 12.6V, Ta = 0 to 70 °C.)

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Input Current Logical Inputs HIGH	Vih = VCC1			100	µA
Input Current Logical Inputs LOW	Vil = 0V			-400	µA
Output Voltage Delay Comparator OFF	Ioh = -400 µA	2.4			V
Output Voltage Delay Comparator ON	Iol = 2.0 mA			0.5	V
Data Pulse Inactive Level Output Voltage	Ioh = -400 µA	2.4			V
Data Pulse Active Level Output Voltage	Iol = 2.0 mA			0.5	V
VCC1 Power Supply Current	No Head Inputs			30	mA
VCC2 Power Supply Current	No Head Inputs			62	mA
NOTE: Characteristic applies to Inputs S0, S1, G0, G1, G2, T0, T1					

PREAMPLIFIER AND MULTIPLEXER CHARACTERISTICS
Output Load = 2 kΩ line-line, Channel Select Signals (S0,S1): VON = 2V Min., VOFF = 0.8V Max.

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain	Vin = 4 mVpp @ 100 kHz ref. to CT VOLT	80		120	V/V
Gain Flatness	Vin = 4 mVpp DC to 0.5 MHz ref. to CT VOLT	±0.5			dB
Bandwidth, -1 dB	Vin = 4 mVpp	1.5			MHz
Bandwidth, -3 dB	Vin = 4 mVpp	3.0			MHz
Differential Input Impedance	Vin = 4 mVpp @ 100 kHz ref to CT VOLT	10			kΩ
Common-Mode Rejection Ratio	Vin = 300 mVpp @ 500 kHz Inputs shorted to CT VOLT	50			dB
Power Supply Rejection Ratio	Δ VCC = 300 mVpp @ 500 kHz Inputs shorted to CT VOLT	50			dB
Channel Isolation	Unselected Vin = 100 mVpp @ 2 MHz. Selected Channel inputs connected to CT VOLT	60			dB

PREAMPLIFIER AND MULTIPLEXER CHARACTERISTICS (Continued)

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Total Harmonic Distortion	Vin = 0.5 to 6.0 mV pp @ 500 kHz			2	%
Equivalent Input Noise	Power BW = 10 kHz to 1MHz Inputs shorted to CT VOLT			10	µVrms
Small Signal Single-Ended Output Res.	Io = 1 mApp @ 100 kHz			35	Ω
Maximum Diff. Output Voltage	Freq = 100 kHz THD < 5%	3			Vpp
Output Offset Voltage	Inputs shorted to CT VOLT Volt Load = Open Circuit			±1.0	V
Common-Mode Output Voltage	Inputs shorted to CT VOLT Volt Load = Open Circuit	2.68		3.5	V
Center Tap Voltage, CT VOLT			3.0		V

DATA DETECTION CIRCUIT CHARACTERISTICS
Vin = 1.0Vpp diff. square wave, Tr, Tf < 20 ns, dc-coupled (for biasing).
RD = 2.5 kΩ; CD = 0.1 µF; RTD = 7.8 kΩ; CTD = 200 pF; RDP = 3.9 kΩ;
CDP = 100 pF. Data Pulse load = 2.5 kΩ to VCC1 plus 20 pF or less to PWR GND.

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Differentiator Maximum Differential Input Voltage	Vin = 100 kHz sine wave, dc-coupled. < 5% THD in voltage across CD. CD = 620 pF RD = 0	5.0			Vpp
Differentiator Input Impedance	Vin = 4Vpp diff., 100 kHz sine wave. CD = 620 pF RD = 0	10			kΩ
Differentiator Threshold Differential Input Voltage	Vin = 100 kHz square wave, Tr, Tf , 0.4 µs, no overshoot. Data Pulse from each Vin transition.			300	mVpp
Data Pulse Width Accuracy	TDP = .59 RDP X CDP, RDP = .85 TDP 3.9 kΩ to10 kΩ, CDP = 75 pF to 300 pF. Width measured at 1.5V amplitude	.85TDP		1.15TDP	sec

DATA DETECTION CIRCUIT CHARACTERISTICS

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Time Domain Filter Delay Accuracy	TTD = 0.59 RTD X CTD + 50 ns, RTD = 3.9 kΩ to 10 kΩ, CTD =100 pF to 750 pF Delay measured from 50% input amplitude to 1.5V Data Pulse amplitude	.85TTD		1.15TTD	sec
Data Pulse Width Drift from + 25 °C value	Width measure from 1.5V amplitude			±5.0	%
Time Domain Filter Delay Drift from +25 °C value	Delay measured from 50% Input amplitude to 1.5V Data Pulse amplitude			±5.0	%
Note: Differentiating network impedance should be chosen such that 1 mA peak current flows at maximum signal level and frequency.					

SIGNAL LEVEL DETECT CIRCUITS CHARACTERISTICS

Level Comparator Inputs connected in parallel with Differentiator Inputs. Vin (Level Comp) = 100 kHz sine wave, ac-coupled. RDS1 = 5 kΩ; RDS2, CDS = open

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Level Comparator Input Thresholds, Single-Ended, Each Input	T0 VT0 = 0.8V VT1 = 0.8V Vo pulse value < 0.5V at MAX LIMIT, >VCC1 - 0.5V at MIN LIMIT	30		70	mV pk
	T1 VT0 = 2.0V VT1 = 0.8V Vo pulse Value <0.5V at MAX LIMIT, >VCC1 - 0.5V at MIN LIMIT	97		153	mV pk
	T2 VT0 = 0.8V VT1 = 2.0V Vo pulse value <0.5V at MAX LIMIT, >VCC1 - 0.5V at MIN LIMIT	138		202	mV pk
	T3 VT0 = 2.0V VT1 = 2.0V Vo pulse value <0.5V at MAX LIMIT, >VCC1 - 0.5V at MIN LIMIT	210		290	mV pk
Level Comparator Diff. Input Resistance	Vin = 5 Vpp @ 100 kHz	5			kΩ
Level Comparator Off Output Leakage	Vo = VCC1			25	µA

9

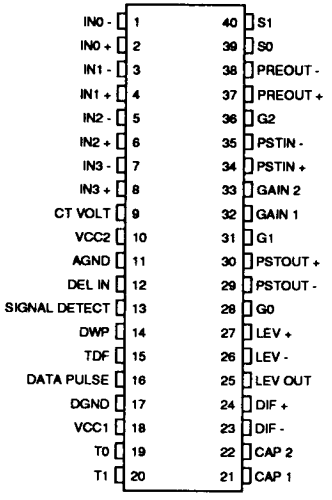
SIGNAL LEVEL DETECT CIRCUITS CHARACTERISTICS (Continued)

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Level Comparator ON Output Voltage	VT0 = 0.8V VT1 = 0.8V Vin = ±140 mV diff. dc Io = 2.0 mA			0.25	V
Delay Comparator Upper Threshold Voltage	Vo > 2.4V	.65VCC1		.75VCC1	V
Delay Comparator Lower Threshold Voltage	Vo < 0.5V	.25VCC1		.35VCC1	V
Delay Comparator Input Current	0V < Vin < VCC1			25	µA

POSTAMPLIFIER CHARACTERISTICS
Output Load = 2.5 kΩ + 0.1 µF line-line, Vin = 100 mVpp, 100 kHz sine wave, dc-coupled (to provide proper biasing). CG = 0.1 µF, RG = 0.

CHARACTERISTICS	CONDITIONS	MIN	MAX	UNITS
Differential Voltage Gain	A0 VG0 = 0.8V VG1 = 0.8V VG2 = 0.8V A1 VG0 = 2.0V VG1 = 0.8V VG2 = 0.8V A2 VG0 = 0.8V VG1 = 2.0V VG2 = 0.8V A3 VG0 = 2.0V VG1 = 2.0V VG2 = 0.8V A4 VG0 = 0.8V VG1 = 0.8V VG2 = 2.0V A5 VG0 = 2.0V VG1 = 0.8V VG2 = 2.0V A6 VG0 = 0.8V VG1 = 2.0V VG2 = 2.0V A7 VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V ARG VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V when RG = 2.5 kΩ	A7 - 14.75 A7 - 12.75 A7 - 10.75 A7 - 8.75 A7 - 6.75 A7 - 4.75 A7 - 2.75 32 A7 - 7.5	A7 - 13.25 A7 - 11.25 A7 - 9.25 A7 - 7.25 A7 - 5.25 A7 - 3.25 A7 - 1.25 36 A7 - 4.5	dB dB dB dB dB dB dB dB dB
Differential Input Impedance	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V	10		kΩ
Bandwidth, 1dB	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V	1.5		MHz
Bandwidth, 3dB	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V	3.0		MHz
Maximum Diff. Output Voltage	VG0 = 0.8V VG1 - 0.8V VG2 = 0.8V VIN = 100 kHz sine wave THD < 5%	5		Vpp
Small Signal Single-Ended Output Res	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V VIN = 0V Io = 1 mApp, 100 kHz		35	Ω
Input Bias Offset Voltage Range	VG0 = 0.8V VG1 = 0.8V VG2 = 0.8V THD < 2.0%		±1.0	V
Input Bias Common-Mode Voltage Range	VG0 = 0.8V VG1 = 0.8V VG2 = 0.8V THD < 2.0%	2.68	3.5	V

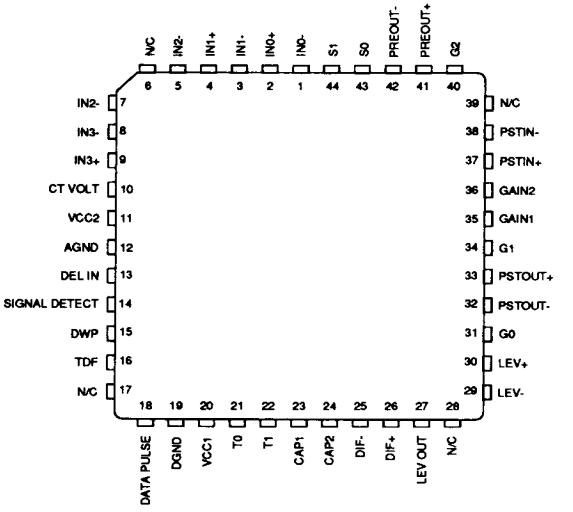
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



40-Pin DIP

THERMAL CHARACTERISTICS: θja

40-pin PDIP	45°C/W
44-pin PLCC	60°C/W



44-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 35P550		
44-Pin PLCC	SSI 35P550-CH	35P550-CH
40-Pin DIP	SSI 35P550-CP	35P550-CP

9

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