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TDA8777

Triple 10-bit video DAC, up to 330 MHz sample frequency

Rev. 03 — 15 August 2005 Preliminary data sheet

1. General description

The TDA8777 consists of three separate 10-bit video Digital-to-Analog Converters (DACs) with complementary outputs. They convert the digital input signals into analog current outputs at a maximum conversion rate of 330 MHz.

The DACs are based on current source architecture.

A sync pulse can be added to the green signal (sync-on-green) to allow devices driven by the video DAC to be synchronized.

The TDA8777 has a Power-down mode to reduce power consumption during inactive periods.

The TDA8777 is fabricated in a CMOS process that ensures high functionality with low power dissipation.

2. Features

- Triple 10-bit DAC
- Sampling frequency up to 330 MHz
- Internal voltage reference (1.21 V)
- Complementary outputs
- Direct drive of double terminated 75 Ω load into standard level
- TTL compatible input
- Sync and blank control inputs
- Analog output current source
- Power-down mode
- 3.3 V power supply
- LQFP48 package

3. Applications

- PC video cards
- High resolution image processing
- Digital video systems
- General purpose high-speed digital-to-analog conversion

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4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
I_{DDA}	analog supply current		-	90	-	mA
INL	integral non-linearity		−2	-	+2	LSB
DNL	differential non-linearity		−1	-	+1	LSB
f_{CLK}	clock frequency					
	TDA8777HL/14/C1		-	-	140	MHz
	TDA8777HL/24/C1		-	-	240	MHz
	TDA8777HL/33/C1		-	-	330	MHz
P_{tot}	total power dissipation		-	297	-	mW
I_{pd}	current in Power-down mode		-	20	-	mA

5. Ordering information

Table 2: Ordering information

Type number	Package			Sampling frequency
	Name	Description	Version	
TDA8777HL/14/C1	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2	140 MHz
TDA8777HL/24/C1				240 MHz
TDA8777HL/33/C1				330 MHz

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6. Block diagram

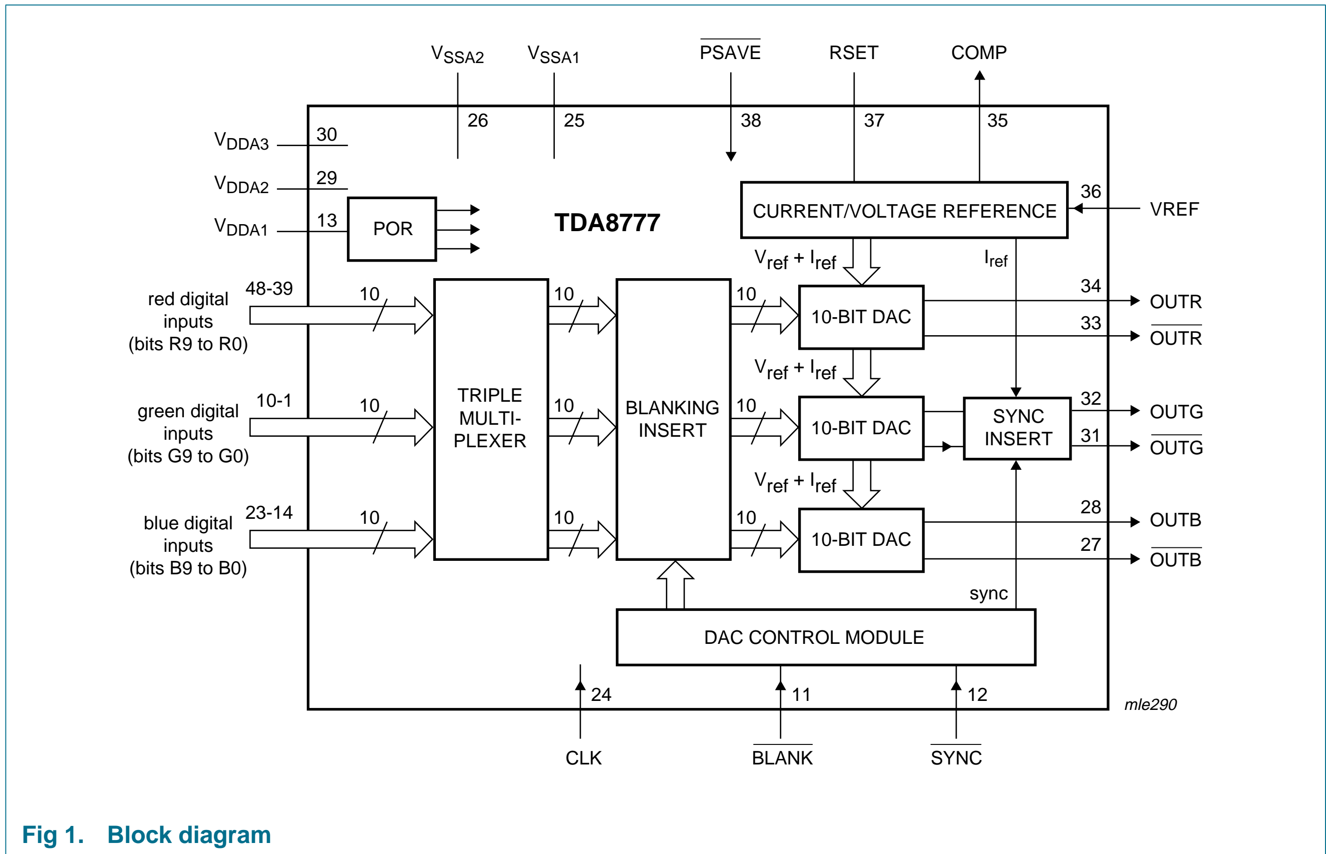

Fig 1. Block diagram

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7. Pinning information

7.1 Pinning

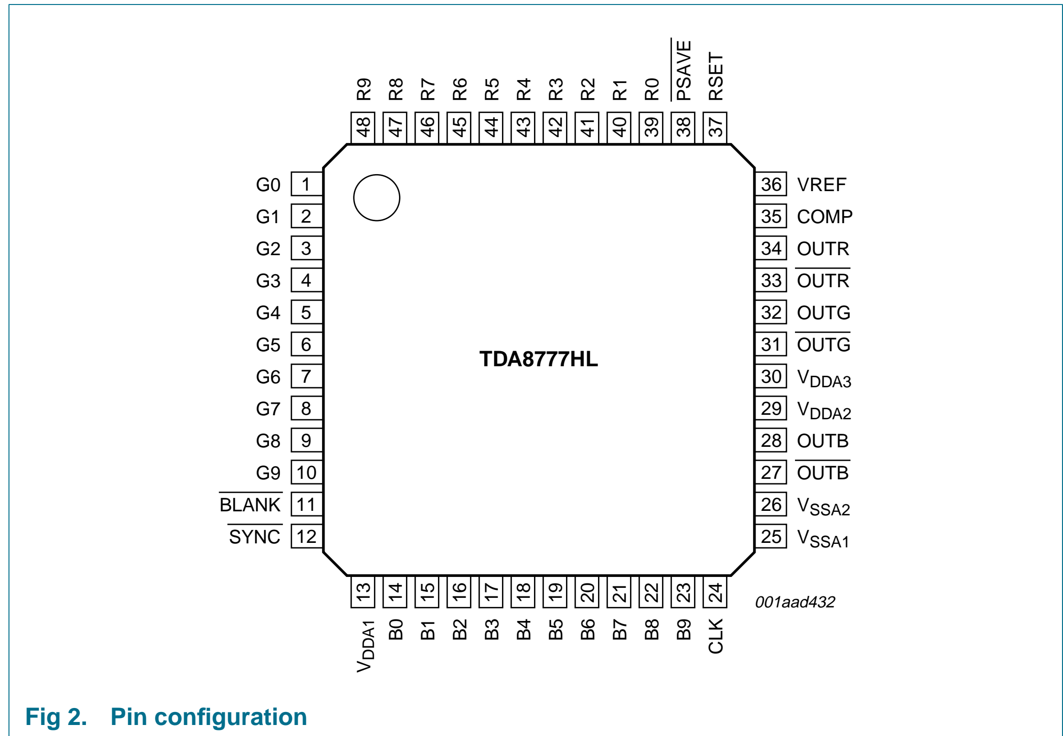

Fig 2. Pin configuration

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
G0	1	green digital input data; bit 0 (LSB)
G1	2	green digital input data; bit 1
G2	3	green digital input data; bit 2
G3	4	green digital input data; bit 3
G4	5	green digital input data; bit 4
G5	6	green digital input data; bit 5
G6	7	green digital input data; bit 6
G7	8	green digital input data; bit 7
G8	9	green digital input data; bit 8
G9	10	green digital input data; bit 9 (MSB)
$\overline{\text{BLANK}}$	11	composite blank control input (active LOW)
$\overline{\text{SYNC}}$	12	composite sync control input; for green channel only (active LOW)
V_{DDA1}	13	analog supply voltage 1
B0	14	blue digital input data; bit 0 (LSB)
B1	15	blue digital input data; bit 1
B2	16	blue digital input data; bit 2

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Table 3: Pin description *…continued*

Symbol	Pin	Description
B3	17	blue digital input data; bit 3
B4	18	blue digital input data; bit 4
B5	19	blue digital input data; bit 5
B6	20	blue digital input data; bit 6
B7	21	blue digital input data; bit 7
B8	22	blue digital input data; bit 8
B9	23	blue digital input data; bit 9 (MSB)
CLK	24	clock input
V_{SSA1}	25	analog supply ground 1
V_{SSA2}	26	analog supply ground 2
$\overline{OUTB}$	27	complementary blue current analog output
OUTB	28	blue current analog output
V_{DDA2}	29	analog supply voltage 2
V_{DDA3}	30	analog supply voltage 3
$\overline{OUTG}$	31	complementary green current analog output
OUTG	32	green current analog output
$\overline{OUTR}$	33	complementary red current analog output
OUTR	34	red current analog output
COMP	35	compliance voltage output
VREF	36	voltage reference input
RSET	37	full-scale current control resistor pin
$\overline{PSAVE}$	38	power-save control input (active LOW)
R0	39	red digital input data; bit 0 (LSB)
R1	40	red digital input data; bit 1
R2	41	red digital input data; bit 2
R3	42	red digital input data; bit 3
R4	43	red digital input data; bit 4
R5	44	red digital input data; bit 5
R6	45	red digital input data; bit 6
R7	46	red digital input data; bit 7
R8	47	red digital input data; bit 8
R9	48	red digital input data; bit 9 (MSB)

8. Functional description

This triple 10-bit video DAC is designed to convert digital input signals into analog output currents. All inputs (clock, data, blank and sync) must be TLL levels.

8.1 Voltage reference

The voltage reference input to pin VREF should be 1.21 V. For correct operation, a 100 nF capacitor should be connected between pin VREF and pin V_{DDA}.

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An external reference resistor must be connected between pin RSET and analog ground. This resistor sets the reference current which determines the analog output level, and is specified to be 560 Ω. This value allows a 1 V (p-p) output (video plus sync) into a 37.5 Ω load, such as a double-terminated 75 Ω coaxial cable.

8.2 Blanking and sync pulse insertion

The video signal (see Figure 3) is comprised of the following three parts:

- The video information: defined by the 10 bits used to drive the DAC; nominal signal amplitude = 700 mV (p-p)
- The sync pulse: a horizontal synchronization (hsync) pulse indicates the end of a video line and the start of the next video line; sync nominal amplitude = 300 mV; sync is added to the video signal output via the $\overline{\text{SYNC}}$ input (active LOW)
- The blanking period: allows interface-free detection of both sync and video, blanking is allocated either side of the sync pulse; the blank level is equal to the video black level; blanking is added to the video signal output via the $\overline{\text{BLANK}}$ input (active LOW).

The values of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ are latched on the rising edge of the clock signal. When no sync and no blank are applied, the DAC can be used continuously. This is the so-called generic mode.

Because the signal delay in the DAC is 1.5 times the clock period, the sync and blank are also delayed by 1.5 times the clock period.

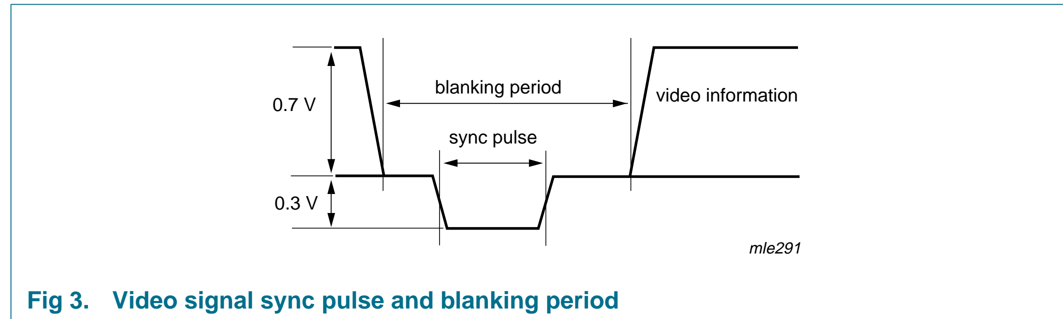

Fig 3. Video signal sync pulse and blanking period

9. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage	referred to V_{SSA1}	–0.5	+6.5	V
V_n	voltage on digital input pins	referred to V_{SSA2}	–0.5	+5.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		–40	+125	°C

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10. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air for SOT313-2	88	K/W

11. Characteristics

Table 6: Characteristics

Typical values measured at V_{DDA} = 3.3 V; R_{RSET} = 560 Ω; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
I_{DDA}	analog supply current		-	90	-	mA
P_{tot}	total power dissipation		-	297	-	mW
I_{pd}	current in Power-down mode		-	20	-	mA
Inputs						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
I_{IL}	LOW-level input current		-	-	80	µA
I_{IH}	HIGH-level input current		-	-	120	µA
C_{IN}	input capacitance		-	<tbd>	-	pF
Band gap reference						
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
I_{DDA}	analog supply current		-	2.7	-	mA
V_{VREF}	reference voltage input		-	1.21	-	V
R_{RSET}	resistor for reference current		-	560	-	Ω
Digital-to-analog converter						
RES_{DAC}	DAC resolution		-	-	10	bits
$\Delta I_{o(DAC)}$	DAC to DAC output current matching		-	-	4	%
INL	integral non-linearity		−2	-	+2	LSB
DNL	differential non-linearity		−1	-	+1	LSB
DAC_{CT}	DAC to DAC crosstalk		-	<tbd>	-	dB
THD	total harmonic distortion	f_{CLK} = 140 MHz				
		f_{OUT} = 1 MHz	-	60	-	dB
		f_{OUT} = 2.2 MHz	-	60	-	dB
		f_{OUT} = 4.7 MHz	-	60	-	dB
		f_{OUT} = 12 MHz	-	59	-	dB
		f_{OUT} = 22 MHz	-	58	-	dB
		f_{OUT} = 39 MHz	-	57	-	dB

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Table 6: Characteristics *...continued*

Typical values measured at V_{DDA} = 3.3 V; R_{RSET} = 560 Ω; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	f_{CLK} = 240 MHz				
		f_{OUT} = 1 MHz	-	60	-	dB
		f_{OUT} = 2.2 MHz	-	60	-	dB
		f_{OUT} = 4.7 MHz	-	60	-	dB
		f_{OUT} = 12 MHz	-	60	-	dB
		f_{OUT} = 22 MHz	-	54	-	dB
		f_{OUT} = 39 MHz	-	51	-	dB
		f_{CLK} = 330 MHz				
		f_{OUT} = 1 MHz	-	60	-	dB
		f_{OUT} = 2.2 MHz	-	60	-	dB
		f_{OUT} = 4.7 MHz	-	60	-	dB
		f_{OUT} = 12 MHz	-	60	-	dB
		f_{OUT} = 22 MHz	-	52	-	dB
		f_{OUT} = 39 MHz	-	43	-	dB
SFDR	spurious-free dynamic range to Nyquist limit	f_{CLK} = 140 MHz				
		f_{OUT} = 1 MHz	-	62	-	dB
		f_{OUT} = 2.2 MHz	-	62	-	dB
		f_{OUT} = 4.7 MHz	-	63	-	dB
		f_{OUT} = 12 MHz	-	63	-	dB
		f_{OUT} = 22 MHz	-	61	-	dB
		f_{OUT} = 39 MHz	-	61	-	dB
		f_{CLK} = 240 MHz				
		f_{OUT} = 1 MHz	-	61	-	dB
		f_{OUT} = 2.2 MHz	-	61	-	dB
		f_{OUT} = 4.7 MHz	-	63	-	dB
		f_{OUT} = 12 MHz	-	56	-	dB
		f_{OUT} = 22 MHz	-	58	-	dB
		f_{OUT} = 39 MHz	-	52	-	dB
		f_{CLK} = 330 MHz				
		f_{OUT} = 1 MHz	-	59	-	dB
		f_{OUT} = 2.2 MHz	-	59	-	dB
		f_{OUT} = 4.7 MHz	-	54	-	dB
		f_{OUT} = 12 MHz	-	53	-	dB
		f_{OUT} = 22 MHz	-	54	-	dB
		f_{OUT} = 39 MHz	-	47	-	dB
Outputs						
$V_{O(compl)}$	output voltage compliance		0	-	1.4	V
Z_{OUT}	output impedance		-	<tbd>	-	kΩ
C_{OUT}	output capacitance		-	<tbd>	-	pF

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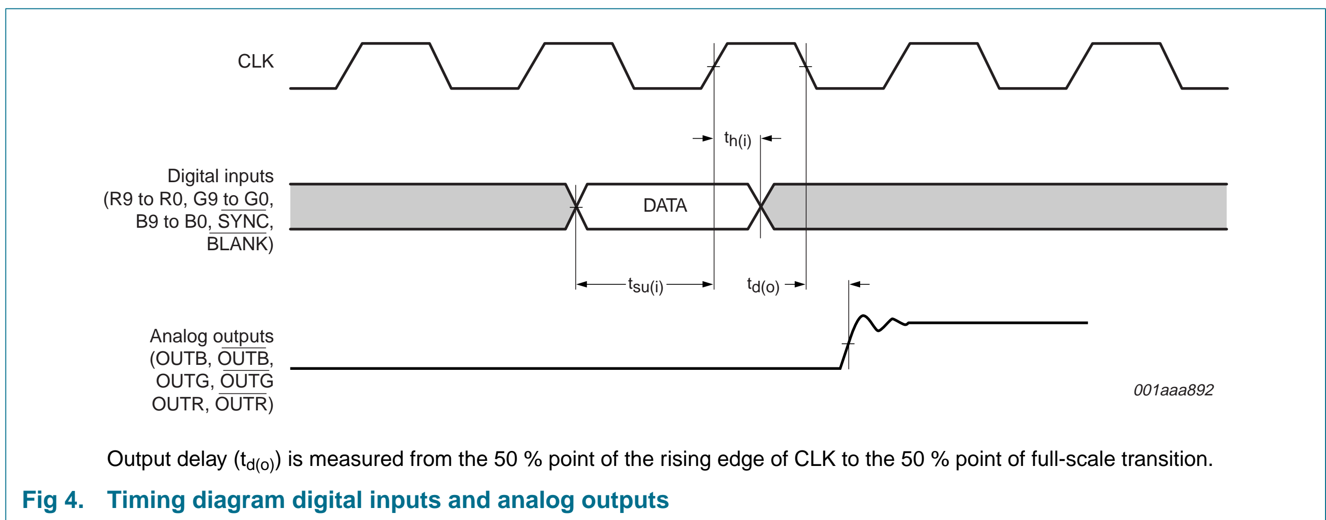
Table 6: Characteristics *...continued*

Typical values measured at V_{DDA} = 3.3 V; R_{RSET} = 560 Ω; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing						
f_{CLK}	clock frequency					
	TDA8777HL/14/C1		-	-	140	MHz
	TDA8777HL/24/C1		-	-	240	MHz
	TDA8777HL/33/C1		-	-	330	MHz
$t_{d(p)}$	pipeline delay	in clock cycles	2.5	2.5	2.5	
$t_{su(i)}$	input setup time	see Figure 4	0.15	-	-	ns
$t_{h(i)}$	input hold time	see Figure 4	0	-	-	ns
$t_{d(o)}$	output delay time	see Figure 4	-	3.75	-	ns



Output delay ($t_{d(o)}$) is measured from the 50 % point of the rising edge of CLK to the 50 % point of full-scale transition.

Fig 4. Timing diagram digital inputs and analog outputs

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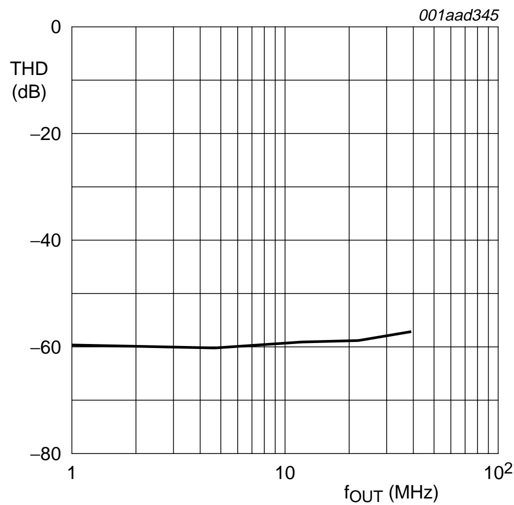
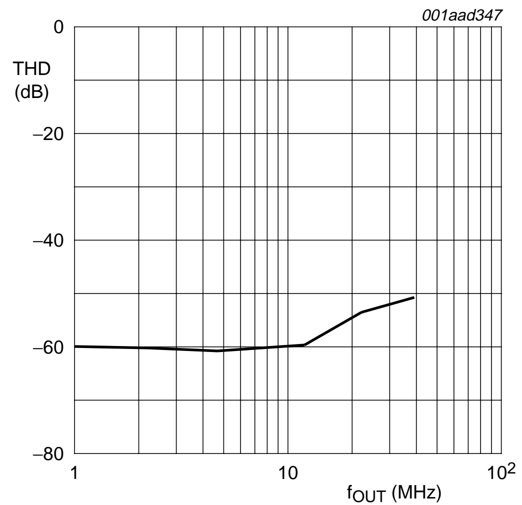
12. Application information



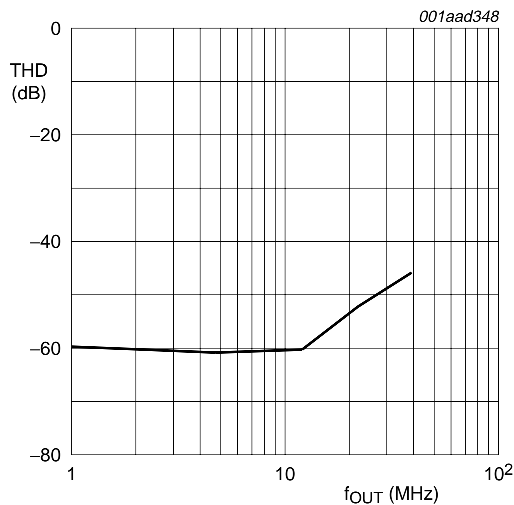
Sampling frequency = 140 MHz.

Fig 5. THD as a function of f_{OUT}, typical values



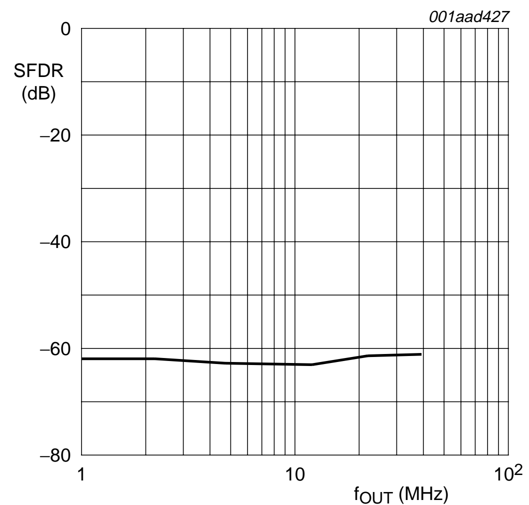
Sampling frequency = 240 MHz.

Fig 6. THD as a function of f_{OUT}, typical values



Sampling frequency = 330 MHz.

Fig 7. THD as a function of f_{OUT}, typical values



Sampling frequency = 140 MHz.

Fig 8. SFDR as a function of f_{OUT}, typical values

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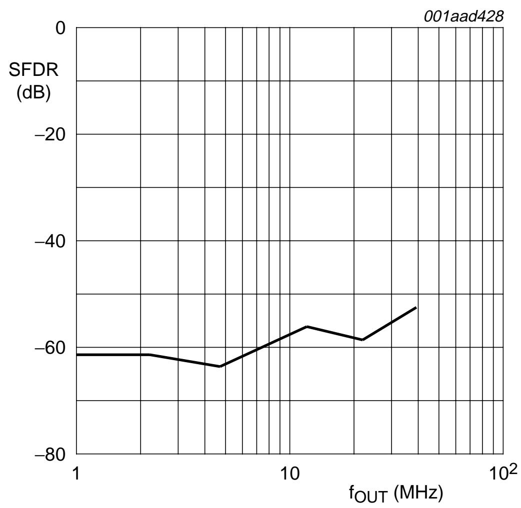
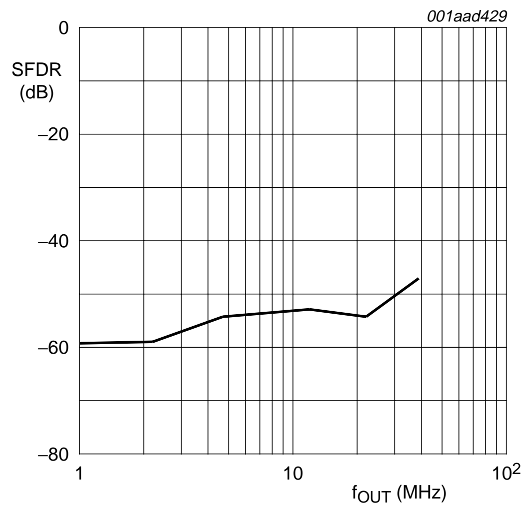


Sampling frequency = 240 MHz

Fig 9. SFDR as a function of f_{OUT}, typical values.



Sampling frequency = 330 MHz.

Fig 10. SFDR as a function of f_{OUT}, typical values

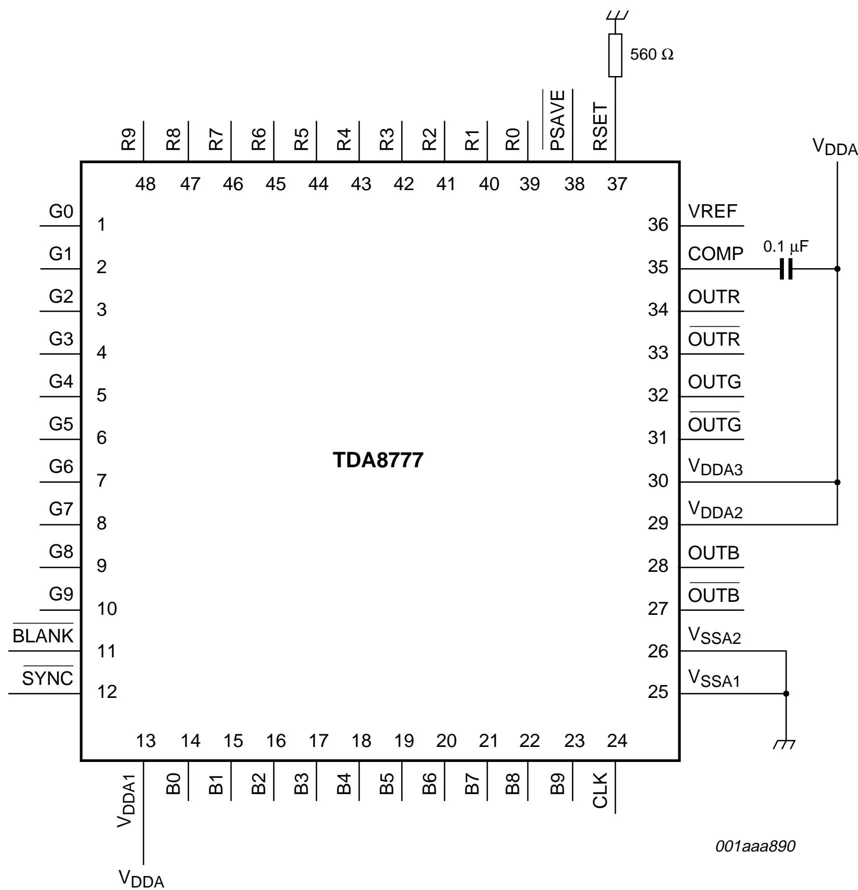


Fig 11. Application diagram

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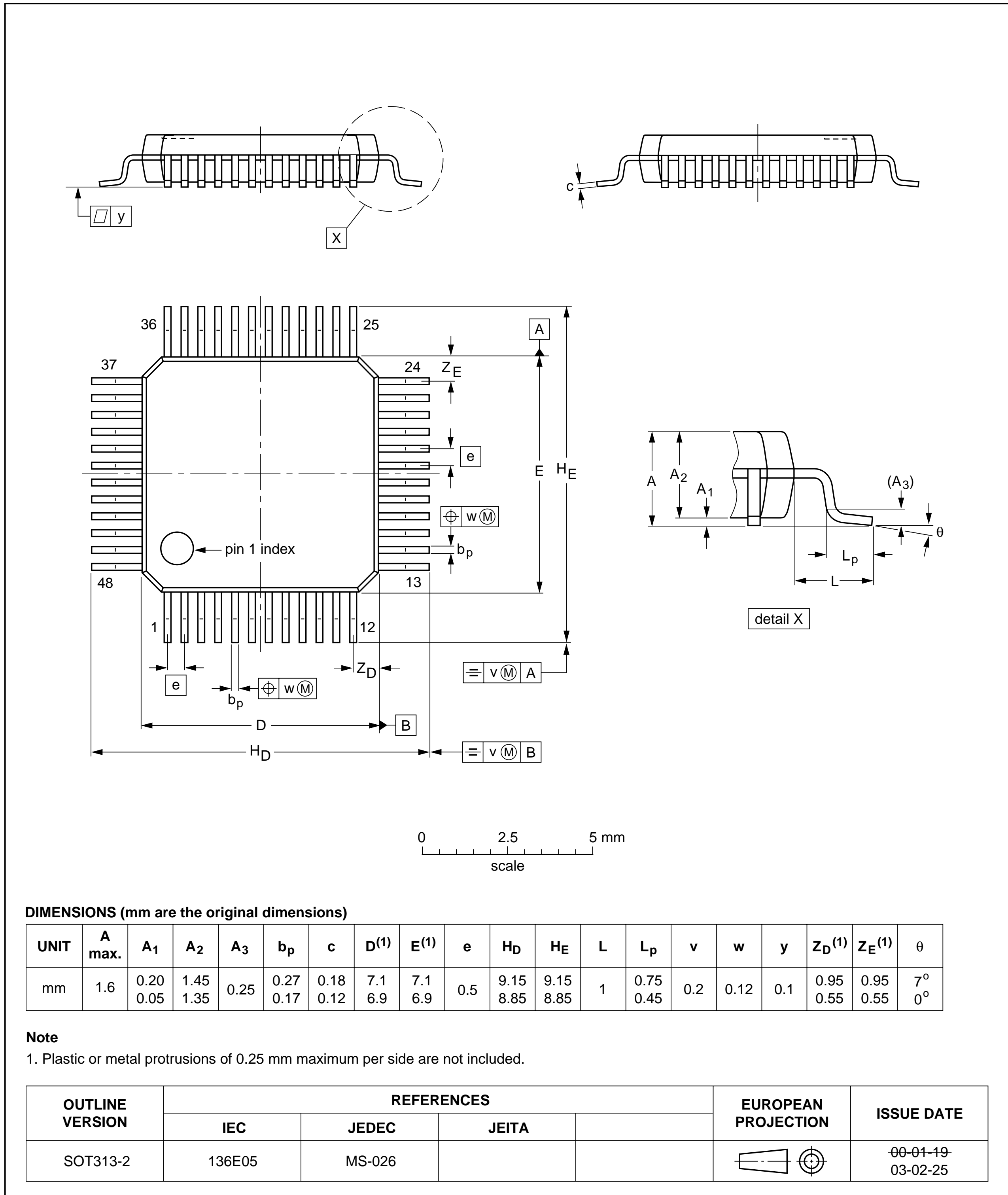
13. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 12. Package outline SOT313-2 (LQFP48)

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14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

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– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 7: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

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[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

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15. Revision history

Table 8: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TDA8777_3	20050815	Preliminary data sheet	-	-	TDA8777_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Status changed to Preliminary data sheet. • Characteristics table revised, SPDR and THD data added, see Table 6. • Figure 4 corrected. • Figure 5 through to Figure 10 added.				
TDA8777_2	20040517	Objective specification	-	-	TDA8777_1
TDA8777_1	20040108	Objective specification	-	-	-

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16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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