# DATA SHEET



# MOS INTEGRATED CIRCUIT $\mu$ PD160903

# 384/402-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

#### **DESCRIPTION**

The  $\mu$  PD160903 is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 262,144 colors by output of 64 values  $\gamma$ -corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as Vss<sub>2</sub> + 0.1 V to Vdd - 0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a clock frequency of 45 MHz when driving at 2.7 V.

#### **FEATURES**

- · CMOS level input
- 384/402 outputs
- . Input of 6 bits (gray-scale data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Logic power supply voltage (VDD1): 2.7 to 3.6 V
- Driver power supply voltage ( $V_{DD2}$ ): 5.5 V  $\pm$  0.275 V
- High-speed data transfer: fclk = 45 MHz (internal data transfer speed when operating at VDD1 = 2.7 V)
- Output dynamic range: Vss2 + 0.1 V to Vdd2 0.1 V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Display data inversion function (POL21, POL22)
- Single-side mounting is possible (incorporation of slim TCP)

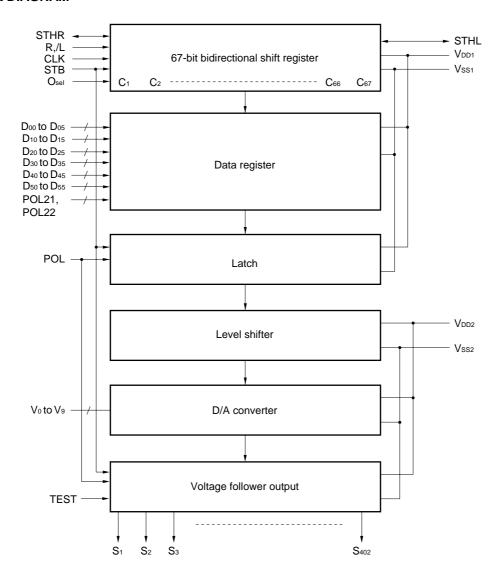
#### **ORDERING INFORMATION**

Part Number	Package	
μ PD160903N-xxx	TCP (TAB package)	

**Remark** The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

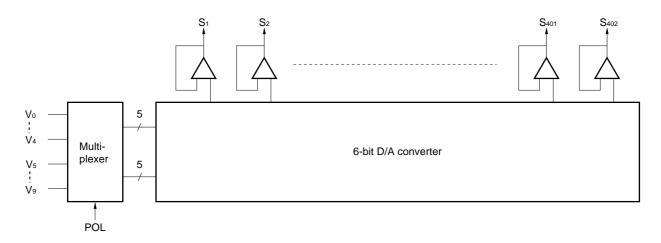
The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version. Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

# 1. BLOCK DIAGRAM

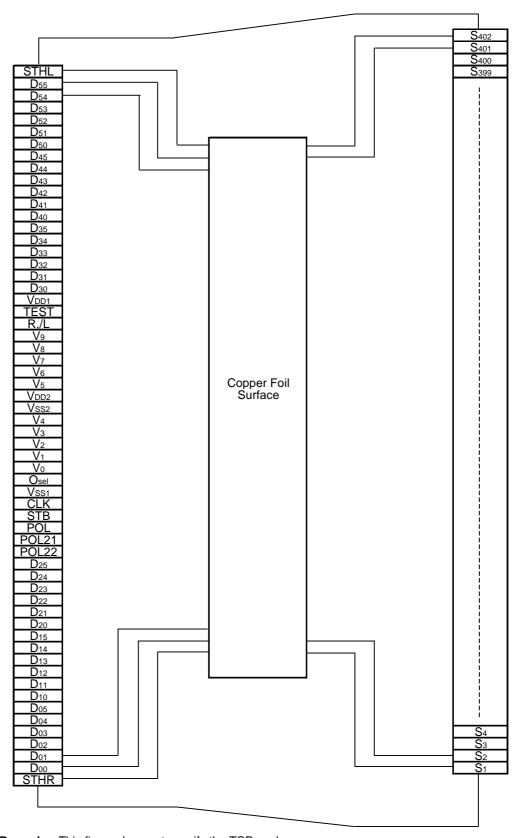


Remark /xxx indicates active low signal.

# 2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



# 3. PIN CONFIGURATION (µPD160903N-xxx) (Copper Foil Surface, Face-up)



 $\label{eq:Remark} \textbf{Remark} \quad \text{This figure does not specify the TCP package}.$ 



# 4. PIN FUNCTIONS

Din Cumbal	Din Nama	I/O	(1/2)
Pin Symbol	Pin Name		Description The D/A converted 64 grove code english veltage is surface.
S <sub>1</sub> to S <sub>402</sub>	Driver output	0	The D/A converted 64-gray-scale analog voltage is output.
Osel	Selection number of	I	Osel:= H or open: 384 outputs (Output pinsS <sub>193</sub> through S <sub>210</sub> are invalid)
	outputs switching		Osel: = L: 402 outputs
D 4- D	D'anlas data		Pulled up internally in the LSI.
D <sub>00</sub> to D <sub>05</sub>	Display data	I	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6
D <sub>10</sub> to D <sub>15</sub>			dots (2 pixels).
D <sub>20</sub> to D <sub>25</sub>			Dxo: LSB, Dxs: MSB
D <sub>30</sub> to D <sub>35</sub>			
D40 to D45			
D <sub>50</sub> to D <sub>55</sub>			
R,/L	Shift direction control	I	Refers to the shift direction control. The shift directions of the shift registers are as follows.
			R,/L = H (right shift): STHR (input), $S_1 \rightarrow S_{402}$ , STHL (output)
			R,/L = L (left shift) : STHL (input), $S_{402} \rightarrow S_1$ , STHR (output)
STHR	Right shift start pulse	I/O	These refer to the start pulse I/O pins when driver ICs are connected in cascade.
			Fetching of display data starts when H is read at the rising edge of CLK.
			R,/L = H (right shift): STHR input, STHL output
STHL	Loft chift atort pulso	I/O	R,/L = L (left shift): STHL input, STHR output
SITL	Left shift start pulse	1/0	A high level should be input as the pulse of one cycle of the clock signal.
			If the start pulse input is more than 2CLK, the first 1CLK of the high-level input is
			valid.
CLK	Shift clock	I	Refers to the shift register's shift clock input. The display data is incorporated into
			the data register at the rising edge. At the rising edge of the 67th clock (64th clock
			in 384 outputs mode) after the start pulse input, the start pulse output reaches the
			high level, thus becoming the start pulse of the next-level driver. If 69th clock (66th
			clock in 384 mode) pulses are input after input of the start pulse, input of display
			data is halted automatically. The contents of the shift register are cleared at the
			STB's rising edge.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge.
			And, at the falling edge, the gray scale voltage is supplied to the driver after 4CLK.
			It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity	I	POL = L: The $S_{2n-1}$ output uses $V_0$ to $V_4$ as the reference supply. The $S_{2n}$ output
			uses V <sub>5</sub> to V <sub>9</sub> as the reference supply.
			POL = H: The $S_{2n-1}$ output uses $V_5$ to $V_9$ as the reference supply. The $S_{2n}$ output
			uses V <sub>0</sub> to V <sub>4</sub> as the reference supply.
			S <sub>2n-1</sub> indicates the odd output: and S <sub>2n</sub> indicates the even output. Input of the POL
			signal is allowed the setup time (tpol-stb) with respect to STB's rising edge.
POL21,	Data inversion	I	Data inversion can invert when display data is loaded.
POL22			POL21: Invert/not invert of display data D <sub>00</sub> to D <sub>05</sub> , D <sub>10</sub> to D <sub>15</sub> , D <sub>20</sub> to D <sub>25</sub> .
			POL22: Invert/not invert of display data D <sub>30</sub> to D <sub>35</sub> , D <sub>40</sub> to D <sub>45</sub> , D <sub>50</sub> to D <sub>55</sub> .
			POL21, POL22 = H: Display data is inverted.
			POL21, POL22 = L: Display data is not inverted.
TEST	Test	I	Normally, TEST = H or open.
			This pin is pulled up to the VDD1 power supply inside the IC
Vo to V9	$\gamma$ -corrected power	-	Input the $\gamma$ -corrected power supplies from outside by using operational amplifier.
	supplies		Make sure to maintain the following relationships. During the gray scale voltage
			output, be sure to keep the gray scale level power supply at a constant level.
			$V_{DD2} - 0.1 \text{ V} \ge V_0 > V_1 > V_2 > V_3 > V_4 > 0.5 \text{ V}_{DD2} > V_5 > V_6 > V_7 > V_8 > V_9 \ge V_{SS2} + 0.1 \text{ V}_{SS2} + 0.1  V$

(2/2)

Pin Symbol	Pin Name	I/O	Description
V <sub>DD1</sub>	Logic power supply	-	2.7 to 3.6 V
V <sub>DD2</sub>	Driver power supply	_	5.5 V ± 0.275 V
Vss1	Logic ground	_	Grounding
Vss2	Driver ground	=	Grounding

- Cautions 1. The power start sequence must be V<sub>DD1</sub>, logic input, and V<sub>DD2</sub> & V<sub>0</sub> to V<sub>9</sub> in that order. Reverse this sequence to shut.
  - 2. To stabilize the supply voltage, please be sure to insert a 0.1  $\mu$ F bypass capacitor between V<sub>DD1</sub>-V<sub>SS1</sub> and V<sub>DD2</sub>-V<sub>SS2</sub>. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01  $\mu$ F is also recommended between the  $\gamma$ -corrected power supply terminals (V<sub>0</sub>, V<sub>1</sub>, V<sub>2</sub>,....., V<sub>9</sub>) and V<sub>SS2</sub>.

5

#### 5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The  $\mu$  PD160903 incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode voltage. The D/A converter consists of ladder resistors and switches.

The ladder resistors (r0 to r62) are designed so that the ratio of LCD panel  $\gamma$ -compensated voltages to V<sub>0</sub>' to V<sub>63</sub>' and V<sub>0</sub>" to V<sub>63</sub>" is almost equivalent. For the 2 sets of five  $\gamma$ -compensated power supplies, V<sub>0</sub> to V<sub>4</sub> and V<sub>5</sub> to V<sub>9</sub>, respectively, input gray scale voltages of the same polarity with respect to the common voltage.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages  $V_{DD2}$  and  $V_{SS2}$ , common electrode potential  $V_{COM}$ , and  $\gamma$ -corrected voltages  $V_0$  to  $V_9$  and the input data. Be sure to maintain the voltage relationships as follows:

$$V_{DD2} - 0.1 \ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > 0.5 \ V_{DD2} > V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1 \ V_{SS2} + 0.1 \ V_{SS2} + 0.1 \ V_{SS2} + 0.1 \ V_{SS3} + 0.$$

Figures 5–2 and 5–3 indicates the relationship between the input data and output voltage and the resistance values of the resistor strings.

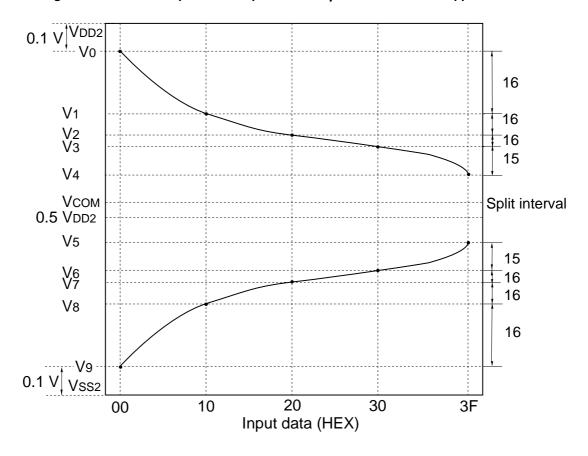


Figure 5–1. Relationship between Input Data and  $\gamma$ -corrected Power Supplies

Resitance ratio

800

750

700

650

600

550 550

500

500 400

400

350

350

350

300

300

300

250 250

250

200

200

200

150

150 150

150

100

100

100

100

100

100

100

100

100 100

100

100

100

100

100

100

100

100

100

100

100

100

100

100

100

100

150

150

150

200

200

250

250

300

500

800

rn

r0

r1

r2

r3

r4

r5

r6

r7

r8

r10

r11

r12

r13

r14

r15

r16

r17

r18

r19

r20

r21

r22

r23

r24

r25

r26 r27

r28

r29

r30

r31

r32

r33

r34

r35

r36

r37

r39

r40

r41

r42

r43

r44

r45

r46

r47

r48 r49

r50

r51

r52

r53

r54

r55

r56

r57

r58

r59

r60

r61

r62

Figure 5–2. Relationship between Input Data and Output Voltage  $V_{DD2}-0.1\ V\geq V_0>V_1>V_2>V_3>V_4>0.5\ V_{DD2},\ POL21,\ POL22=L$ 

r0 r1 V2 r2 r3 r14 r15 r16 r17 r47 r49 r60 r61 V<sub>62</sub>' r62

Data	DX5	DX4	DX3	DX2	DX1	DX0		Output vol	tage	
00H	0	0	0	0	0	0	V0'	V0	9-	
01H	0	0	0	0	0	1	V1'	V1+(V0-V1)×	7250 /	8050
02H	0	0	0	0	1	0		V1+(V0-V1)×	6500 /	8050
03H	0	0	0	0	1	1		V1+(V0-V1)×	5800 /	8050
04H	0	0	0	1	0	0		V1+(V0-V1)×	5150 /	8050
05H	0	0	0	1	0	1		V1+(V0-V1)×	4550 /	8050
06H	0	0	0	1	1	0		V1+(V0-V1)×	4000 /	8050
07H	0	0	0	1	1	1		V1+(V0-V1)×	3450 /	8050
08H	0	0	1	0	0	0		V1+(V0-V1)×	2950 /	8050
09H	0	0	1	0	0	1		V1+(V0-V1)×	2450 /	8050
0AH	0	0	1	0	1	0		V1+(V0-V1)×	2050 /	8050
0BH	0	0	1	0	1	1	_	V1+(V0-V1)×	1650 /	8050
0CH	0	0	1	1	0	0	_	V1+(V0-V1)×	1300 /	8050
0DH	0	0	1	1	0	1	_	V1+(V0-V1)×	950 /	8050
0EH			1	1	1	0		, ,	600 /	
	0	0				1		V1+(V0-V1)×		8050
0FH	0	0	1	1	1			V1+(V0-V1)×	300 /	8050
10H	0	1	0	0	0	0		V1	0.450 /	0750
11H	0	1	0	0	0	1		V2+(V1-V2)×	2450 /	2750
12H	0	1	0	0	1	0		V2+(V1-V2)×	2200 /	2750
13H	0	1	0	0	1	1		V2+(V1-V2)×	1950 /	2750
14H	0	1	0	1	0	0		V2+(V1-V2)×	1700 /	2750
15H	0	1	0	1	0	1		V2+(V1-V2)×	1500 /	2750
16H	0	1	0	1	1	0		V2+(V1-V2)×	1300 /	2750
17H	0	1	0	1	1	1		V2+(V1-V2)×	1100 /	2750
18H	0	1	1	0	0	0		V2+(V1-V2)×	950 /	2750
19H	0	1	1	0	0	1		V2+(V1-V2)×	800 /	2750
1AH	0	1	1	0	1	0	V26'	V2+(V1-V2)×	650 /	2750
1BH	0	1	1	0	1	1	V27'	V2+(V1-V2)×	500 /	2750
1CH	0	1	1	1	0	0	V28'	V2+(V1-V2)×	400 /	2750
1DH	0	1	1	1	0	1	V29'	V2+(V1-V2)×	300 /	2750
1EH	0	1	1	1	1	0	V30'	V2+(V1-V2)×	200 /	2750
1FH	0	1	1	1	1	1	V31'	V2+(V1-V2)×	100 /	2750
20H	1	0	0	0	0	0	V32'	V2		
21H	1	0	0	0	0	1	V33'	V3+(V2-V3)×	1500 /	1600
22H	1	0	0	0	1	0	V34'	V3+(V2-V3)×	1400 /	1600
23H	1	0	0	0	1	1	V35'	V3+(V2-V3)×	1300 /	1600
24H	1	0	0	1	0	0	V36'	V3+(V2-V3)×	1200 /	1600
25H	1	0	0	1	0	1		V3+(V2-V3)×	1100 /	1600
26H	1	0	0	1	1	0		V3+(V2-V3)×	1000 /	1600
27H	1	0	0	1	1	1		V3+(V2-V3)×	900 /	1600
28H	1	0	1	0	0	0		V3+(V2-V3)×	800 /	1600
29H	1	0	1	0	0	1		V3+(V2-V3)×	700 /	1600
2AH	1	0	1	0	1	0		V3+(V2-V3)×	600 /	1600
2BH	1	0	1	0	1	1	_	V3+(V2-V3)×	500 /	1600
2CH	1	0	1	1	0	0		V3+(V2-V3)×	400 /	1600
2DH	1	0	1	1	0	1	_	V3+(V2-V3)×	300 /	1600
	1	0	1	1	1	0				
2EH 2FH	1		1	1	1	1		V3+(V2-V3)×	200 /	1600
		0						V3+(V2-V3)×	100 /	1600
30H	1	1	0	0	0	0		V3	2250 /	2450
31H	1	1	0	0	0	1		V4+(V3-V4)×	3350 /	3450
32H	1	1	0	0	1	0	-	V4+(V3-V4)×	3250 /	3450
33H	1	1	0	0	1	1		V4+(V3-V4)×	3150 /	3450
34H	1	1	0	1	0	0		V4+(V3-V4)×	3050 /	3450
35H	1	1	0	1	0	1		V4+(V3-V4)×	2950 /	3450
36H	1	1	0	1	1	0		V4+(V3-V4)×	2800 /	3450
37H	1	1	0	1	1	1		V4+(V3-V4)×	2650 /	3450
38H	1	1	1	0	0	0		V4+(V3-V4)×	2500 /	3450
39H	1	1	1	0	0	1	V57'	V4+(V3-V4)×	2300 /	3450
3AH	1	1	1	0	1	0	V58'	V4+(V3-V4)×	2100 /	3450
	1	1	1	0	1	1	V59'	V4+(V3-V4)×	1850 /	3450
3BH		4	1	1	0	0	_	V4+(V3-V4)×	1600 /	3450
3BH 3CH	1	1								
	1	1	1	1	0	1	V61'	V4+(V3-V4)×	1300 /	3450
3CH					0	1		V4+(V3-V4)× V4+(V3-V4)×	1300 / 800 /	3450 3450

Caution There is no connection between V4 and V5 terminal in the chip.

7

μPD160903

Figure 5–3. Relationship between Input Data and Output Voltage  $0.5~V_{DD2}>V_5>V_6>V_7>V_8>V_9\geq V_{SS2}+0.1~V,~POL21,~POL22=L$ 

			Data	DX5	DX4	DX3	DX2	DX1	DX0	1	Output voltage	rn	Resistance ratio
V <sub>5</sub> -		V <sub>63</sub> "	00H	0	0	0	0	0	0	V0"	V9	r0	800
r62	$\Box$		01H	0	0	0	0	0	1	V1"	V9+(V8-V9)× 800 / 8050	r1	750
	Т_	—► V <sub>62</sub> "	02H	0	0	0	0	1	0	V2"	V9+(V8-V9)× 1550 / 8050	r2	700
r61	ф	- V 02	03H	0	0	0	0	1	1	V3"	V9+(V8-V9)× 2250 / 8050	r3	650
101	Y		04H	0	0	0	1	0	0	V4"	V9+(V8-V9)× 2900 / 8050	r4	600
	4	V <sub>61</sub> "	05H	0	0	0	1	0	1	V5"	V9+(V8-V9)× 3500 / 8050	r5	550
r60	Ļ		06H	0	0	0	1	1	0	V6"	V9+(V8-V9)× 4050 / 8050	r6	550
	4	V <sub>60</sub> "	07H	0	0	0	1	1	1	V7"	V9+(V8-V9)× 4600 / 8050	r7	500
r59	Ļ		08H	0	0	1	0	0	0	V8"	V9+(V8-V9)× 5100 / 8050	r8	500
	1		09H	0	0	1	0	0	1	V9"	V9+(V8-V9)× 5600 / 8050	r9	400
			0AH	0	0	1	0	1	0	V10"	V9+(V8-V9)× 6000 / 8050	r10	400
	i i		0BH	0	0	1	0	1	1	V11"	V9+(V8-V9)× 6400 / 8050	r11	350
			0CH	0	0	1	1	0	0	V12"	V9+(V8-V9)× 6750 / 8050	r12	350
	<u> </u>		0DH	0	0	1	1	0	1	V13"	V9+(V8-V9)× 7100 / 8050	r13	350
r49	Ш		0EH	0	0	1	1	1	0	V14"	V9+(V8-V9)× 7450 / 8050	r14	300
	上	V <sub>49</sub> "	0FH	0	0	1	1	1	1	V15"	V9+(V8-V9)× 7750 8050	r15	300
r48	Ш		10H	0	1	0	0	0	0	V16"	V8	r16	300
V <sub>6</sub> —		V <sub>48</sub> "	11H	0	1	0	0	0	1	V17"	V8+(V7-V8)× 300 / 2750	r17	250
r47	Ц		12H	0	1	0	0	1	0	V18"	V8+(V7-V8)× 550 / 2750	r18	250
	Д.	V47"	13H	0	1	0	0	1	1	V19"	V8+(V7-V8)× 800 / 2750	r19	250
r46	Ш		14H	0	1	0	1	0	0	V20"	V8+(V7-V8)× 1050 / 2750	r20	200
	1		15H	0	1	0	1	0	1	V21"	V8+(V7-V8)× 1250 / 2750	r21	200
			16H	0	1	0	1	1	0	V22"	V8+(V7-V8)× 1450 / 2750	r22	200
			17H	0	1	0	1	1	1	V23"	V8+(V7-V8)× 1650 / 2750	r23	150
			18H	0	1	1	0	0	0	V24"	V8+(V7-V8)× 1800 / 2750	r24	150
	i		19H	0	1	1	0	0	1	V25"	V8+(V7-V8)× 1950 / 2750	r25	150
			1AH	0	1	1	0	1	0	V26"	V8+(V7-V8)× 2100 / 2750	r26	150
	i		1BH	0	1	1	0	1	1	V27"	V8+(V7-V8)× 2250 / 2750	r27	100
			1CH	0	1	1	1	0	0	V28"	V8+(V7-V8)× 2350 / 2750	r28	100
			1DH	0	1	1	1	0	1	V29"	V8+(V7-V8)× 2450 / 2750	r29	100
			1EH	0	1	1	1	1	0	V30"	V8+(V7-V8)× 2550 / 2750	r30	100
	- 1		1FH	0	1	1	1	1	1	V31"	V8+(V7-V8)× 2650 2750	r31	100
	į		20H	1	0	0	0	0	0	V32"	V7	r32	100
	- 1		21H	1	0	0	0	0	1	V33"	V7+(V6-V7)× 100 / 1600	r33	100
	i		22H	1	0	0	0	1	0	V34"	V7+(V6-V7)× 200 / 1600	r34	100
	- 1		23H	1	0	0	0	1	1	V35"	V7+(V6-V7)× 300 / 1600	r35	100
			24H	1	0	0	1	0	0	V36"	V7+(V6-V7)× 400 / 1600	r36	100
	1		25H	1	0	0	1	0	1	V37"	V7+(V6-V7)× 500 / 1600	r37	100
r17	ė.		26H	1	0	0	1	1	0	V38"	V7+(V6-V7)× 600 / 1600	r38	100
	ᆛ	<b>→</b> V <sub>17</sub> ''	27H	1	0	0	1	1	1	V39"	V7+(V6-V7)× 700 / 1600	r39	100
r16	$\vdash$	- V17	28H	1	0	1	0	0	0	V40"	V7+(V6-V7)× 800 / 1600	r40	100
V <sub>8</sub> —	ᆛ	- V16"	29H	1	0	1	0	0	1	V41"	V7+(V6-V7)× 900 / 1600	r41	100
vs r15	ф	- 10	2AH	1	0	1	0	1	0	V42"	V7+(V6-V7)× 1000 / 1600	r42	100
113	닏	→ V <sub>15</sub> ''	2BH	1	0	1	0	1	1	V43"	V7+(V6-V7)× 1100 / 1600	r43	100
r14	$\vdash$		2CH	1	0	1	1	0	0	V44"	V7+(V6-V7)× 1200 / 1600	r44	100
114	Ÿ		2DH	1	0	1	1	0	1	V45"	V7+(V6-V7)× 1300 / 1600	r45	100
			2EH	1	0	1	1	1	0	V46"	V7+(V6-V7)× 1400 / 1600	r46	100
	- 1		2FH	1	0	1	1	1	1	V47"	V7+(V6-V7)× 1500 / 1600	r47	100
			30H 31H	1	1	0	0	0	0 1	V48" V49"	V6 V6+(V5-V6)× 100 / 3450	r48 r49	100 100
	- 1		31H 32H	1	1	0	0	1	0	V49"		r50	
	i		32H 33H	1	1	0	0	1	1	V50" V51"	V6+(V5-V6)× 200 / 3450 V6+(V5-V6)× 300 / 3450	r51	100 100
	- }		34H	1	1	0	1	0	0	V51"		r52	100
-0	$\dot{\Box}$		35H	1	1	0	1	0	1	V52 V53"	V6+(V5-V6)× 400 / 3450 V6+(V5-V6)× 500 / 3450	r53	150
r2	Y		36H	1	1	0	1	1	0	V53 V54"	V6+(V5-V6)× 500 / 3450	r54	150
	4	<b>→</b> V <sub>2</sub> ''	37H	1	1	0	1	1	1	V54 V55"	V6+(V5-V6)× 800 / 3450	r55	150
r1	Ļ		38H	1	1	1	0	0	0	V56"	V6+(V5-V6)× 950 / 3450	r56	200
	Щ	<b>→</b> V <sub>1</sub> ''	39H	1	1	1	0	0	1	V57"	V6+(V5-V6)× 1150 / 3450	r57	200
r0	Ļ		3AH	1	1	1	0	1	0	V58"	V6+(V5-V6)× 1350 / 3450	r58	250
V <sub>9</sub> —		<b>→</b> V <sub>0</sub> ''	3BH	1	1	1	0	1	1	V59"	V6+(V5-V6)× 1600 / 3450	r59	250
			3CH	1	1	1	1	0	0	V60"	V6+(V5-V6)× 1850 / 3450	r60	300
			3DH	1	1	1	1	0	1	V61"	V6+(V5-V6)× 2150 / 3450	r61	500
			3EH	1	1	1	1	1	0	V62"	V6+(V5-V6)× 2650 / 3450	r62	800
			3FH	1	1	1	1	1	1	V63"	V5		
						· · · · ·	<u> </u>	<u> </u>	· · · ·				

Caution There is no connection between  $V_4$  and  $V_5$  terminal in the chip.



## 6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x 2 RGBs (6 dots) Input width : 36 bits (2-pixel data)

# (1) $R_{1}/L = H$ (Right shift)

Output	S <sub>1</sub>	S <sub>2</sub>	S₃	S <sub>4</sub>	 S <sub>401</sub>	S <sub>402</sub>
Data	Doo to Do5	D <sub>10</sub> to D <sub>15</sub>	D <sub>20</sub> to D <sub>25</sub>	D <sub>30</sub> to D <sub>35</sub>	 D40 to D45	D <sub>50</sub> to D <sub>55</sub>

# (2) R,/L = L (Left shift)

Output	S <sub>1</sub>	S <sub>2</sub>	S3	S4	 S <sub>401</sub>	S <sub>402</sub>
Data	Doo to Do5	D <sub>10</sub> to D <sub>15</sub>	D <sub>20</sub> to D <sub>25</sub>	D <sub>30</sub> to D <sub>35</sub>	 D <sub>40</sub> to D <sub>45</sub>	D50 to D55

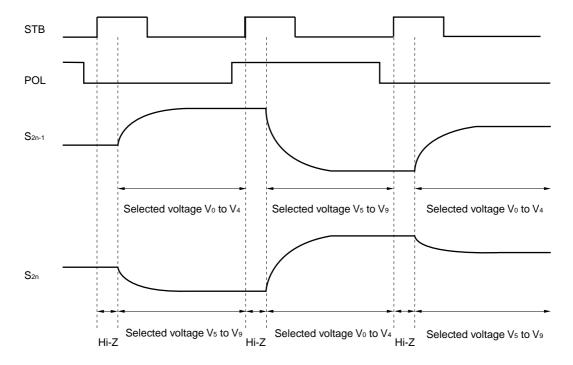
POL	S <sub>2n-1</sub> Note	Note S <sub>2n</sub>
L	Vo to V4	V <sub>5</sub> to V <sub>9</sub>
Н	V <sub>5</sub> to V <sub>9</sub>	Vo to V4

Note  $S_{2n-1}$  (Odd output),  $S_{2n}$  (Even output),  $n = 1, 2, \dots 201$ 

# 7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The gray-scale voltage is output 4 clocks after the start of D/A conversion in the LSI, in synchronization with the rising edge of STB.

During this 4-clock period, Hi-Z is output.



9

## 8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (TA = 25°C, Vss1 = Vss2 = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V <sub>DD1</sub>	-0.5 to +4.0	V
Driver Part Supply Voltage	V <sub>DD2</sub>	−0.5 to +10.0	V
Logic Part Input Voltage	VI1	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver Part Input Voltage	V <sub>I2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Logic Part Output Voltage	V <sub>01</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver Part Output Voltage	V <sub>O2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Operating Ambient Temperature	TA	−20 to +75	°C
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range ( $T_A = -20 \text{ to } +75^{\circ}\text{C}$ ,  $V_{SS1} = V_{SS2} = 0 \text{ V}$ )

		· ·	-			
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V <sub>DD1</sub>		2.7	3.3	3.6	V
Driver Part Supply Voltage	V <sub>DD2</sub>		5.225	5.5	5.775	V
High-Level Input Voltage	ViH		0.7 V <sub>DD1</sub>		V <sub>DD1</sub>	V
Low-Level Input Voltage	VIL		0		0.3 V <sub>DD1</sub>	V
$\gamma$ -Corrected Voltage	V <sub>0</sub> to V <sub>4</sub>		0.5 V <sub>DD2</sub>		V <sub>DD2</sub> -0.1	V
	V <sub>5</sub> to V <sub>9</sub>		0.1		0.5 V <sub>DD2</sub>	V
Driver Part Output Voltage	Vo		0.1		V <sub>DD2</sub> -0.1	V
Clock Frequency	fclk				45	MHz

Electrical Characteristics (T <sub>A</sub>	20 to ±75°C Vpp₁ -	- 27 to 36 V Vnn2 -	55 V + 0 275 V Vee	1 – Vee2 – 0 V)

Parameter	Symbol	Cor	ndition	MIN.	TYP.	MAX.	Unit
Input Leak Current	lıL				±1.0	μΑ	
High-Level Output Voltage	Vон	STHR (STHL), Ion =	0 mA	V <sub>DD1</sub> - 0.1			V
Low-Level Output Voltage	VoL	STHR (STHL), IoL =	0 mA			0.1	V
$\gamma$ -Corrected Resistance	Rγ	V <sub>DD2</sub> = 5.5 V	6.0	12.0	18.0	kΩ	
		$V_0$ to $V_4 = V_5$ to $V_9 =$	2.0 V				
Driver Output Current	Іvон	$V_{DD2} = 5.5 \text{ V}, V_{X} = 5.0 \text{ V}, V_{OUT} = 4.5 \text{ V}$ Note1			-150	-70	μΑ
	Ivol	$V_{DD2} = 5.5 \text{ V}, \text{ Vx} = 0.$	70	250		μΑ	
Output Voltage Deviation	ΔVο	T <sub>A</sub> = 25°C, V <sub>SS2</sub> + 1.0	0 V to V <sub>DD2</sub> – 1.0 V		±5	±20	mV
Output Swing Difference	$\Delta V_{P-P1}$	V <sub>DD1</sub> = 3.3 V	Vout = 1.2 to 4.3 V		±3	±15	mV
Deviation	ΔV <sub>P-P2</sub>	V <sub>DD2</sub> = 5.5 V	Vout = 0.8 to 4.7 V		±7	±20	mV
	ΔV <sub>P-P3</sub>	T <sub>A</sub> = 25°C	Vout = 0.1 to 5.4 V		±15	±30	mV
Logic Part Dynamic Current	I <sub>DD1</sub>	V <sub>DD1</sub>			1.0	6.0	mA
Consumption Note2,3,4							
Driver Part Dynamic Current Consumption Note2,4	I <sub>DD2</sub>	V <sub>DD2</sub> , with no load			3.7	7.0	mA

Notes 1. Vx refers to the output voltage of analog output pins  $S_1$  to  $S_{402}$ .

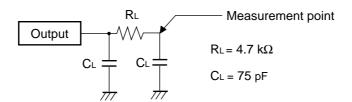
Vout refers to the voltage applied to analog output pins S1 to S402.

- **2.**  $f_{STB} = 48 \text{ kHz}$ .  $f_{CLK} = 32.5 \text{ MHz}$
- **3.** The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
- **4.** Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).

Switching Characteristics (TA = -20 to +75°C, VDD1 = 2.7 to 3.6 V, VDD2 = 5.5 V  $\pm$  0.275 V, Vss1 = Vss2 = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	<b>t</b> PLH1	C <sub>L</sub> = 15 pF		9	18	ns
Driver Output Delay Time	t <sub>PLH2</sub> Note	$C_L = 150 \text{ pF}, R_L = 4.7 \text{ k}\Omega$		3.8	5.0	μs
	t <sub>PLH3</sub> Note			5.4	8.5	μs
	t <sub>PHL2</sub> Note			3.3	5.0	μs
	t <sub>PHL3</sub> Note			4.4	8.5	μs
Input Capacitance	C <sub>I1</sub>	Logic input other than STHR (STHL) is		5	10	pF
		T <sub>A</sub> = 25°C				
C <sub>12</sub> STHR (STHL),T <sub>A</sub> = 25°C		STHR (STHL),TA = 25°C		8	15	pF

Note tplh2 and tphl2 are the time until the voltage reached its target voltage  $\pm 10\%$  from the falling edge of STB. tplh2 and tphl2 are the time until the voltage reached its target voltage  $\pm 20$  mV from the falling edge of STB.



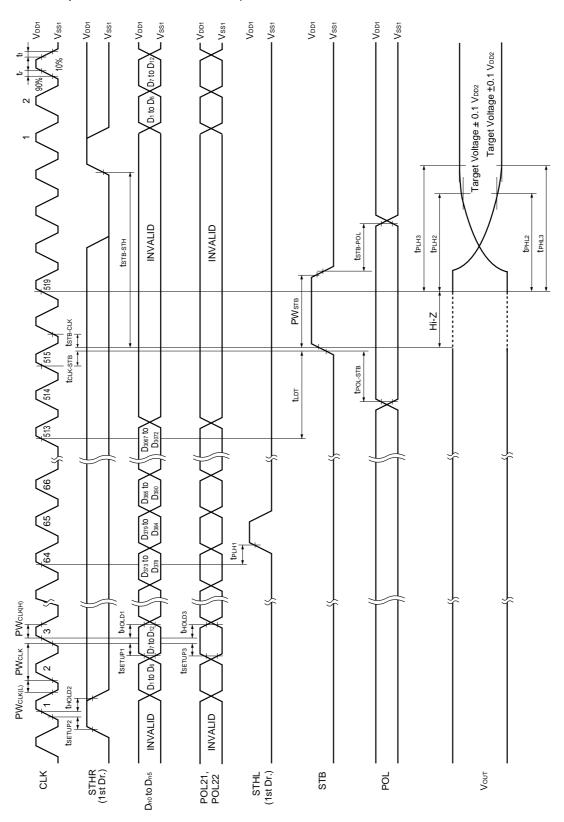
Timing Requirements (TA = -20 to +75°C, VDD1 = 2.7 to 3.6 V, Vss1 = 0 V, tr = tr = 5.0 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PWclk		22			ns
Clock Pulse High Period	PW <sub>CLK(H)</sub>		4			ns
Clock Pulse Low Period	PW <sub>CLK(L)</sub>		4			ns
Data Setup Time	tsetup1		4			ns
Data Hold Time	tHOLD1		2			ns
Start Pulse Setup Time	tsetup2		4			ns
Start Pulse Hold Time	tHOLD2		2			ns
POL21/22 Setup Time	tsetup3		2			ns
POL21/22 Hold Time	thold3		3			ns
STB Pulse Width	PWstB		4			CLK
Last Data Timing	<b>t</b> ldt		2			CLK
CLK-STB Time	tclk-stb	$CLK \uparrow \to STB \uparrow$	4			ns
STB-CLK Time	tsтв-clк	$STB \uparrow \to CLK \uparrow$	4			ns
Time Between STB and Start Pulse	<b>t</b> sтв-sтн	STB $\uparrow \rightarrow$ STHR(STHL) $\uparrow$	2			CLK
POL-STB Time	tpol-stb	POL $\uparrow$ or $\downarrow \rightarrow$ STB $\uparrow$	6			ns
STB-POL Time	tstb-pol	$STB \downarrow \to POL \downarrow or \uparrow$	6			ns

**Remark** Unless otherwise specified, the input level is defined to be  $V_{IH} = 0.7 \text{ V}_{DD1}$ ,  $V_{IL} = 0.3 \text{ V}_{DD1}$ .

# **★** Switching Characteristic Waveform(R,/L= H)

Unless otherwise specified, the input level is defined to be  $V_{IH} = 0.7 \text{ V}_{DD1}$ ,  $V_{IL} = 0.3 \text{ V}_{DD1}$  (the clock and display data numbers are examples when the resolution is XGA).



## 9. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the  $\mu$ PD160903.

For more details, refer to the Semiconductor Device Mounting Technology Manual (C10535E).

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

 $\mu$ PD160903N-xxx : TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100g
		(per solder)
	ACF	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm <sup>2</sup> : time 3 to 5 sec.
	(Adhesive	Real bonding 165 to 180°C: pressure 25 to 45 kg/cm <sup>2</sup> : time 30 to 40 sec.
	Conductive Film)	(When using the anisotropy conductive film SUMIZAC1003 of Sumitomo
		Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

#### NOTES FOR CMOS DEVICES

#### 1 PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

# ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

## 3 STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Data Sheet S14578EJ1V1DS 15

NEC  $\mu$ PD160903

#### **Reference Documents**

NEC Semiconductor Device Reliability/Quality Control System (C10983E)
Quality Grades to NEC's Semiconductor Devices (C11531E)

- The information in this document is current as of June, 2001. The information is subject to change
  without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data
  books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products
  and/or types are available in every country. Please check with an NEC sales representative for
  availability and additional information.
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of
  third parties by or arising from the use of NEC semiconductor products listed in this document or any other
  liability arising from the use of such products. No license, express, implied or otherwise, is granted under any
  patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative
  purposes in semiconductor product operation and application examples. The incorporation of these
  circuits, software and information in the design of customer's equipment shall be done under the full
  responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third
  parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers
  agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize
  risks of damage to property or injury (including death) to persons arising from defects in NEC
  semiconductor products, customers must incorporate sufficient safety measures in their design, such as
  redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  - "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.
  - "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.

(Note)

- (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.
- (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4