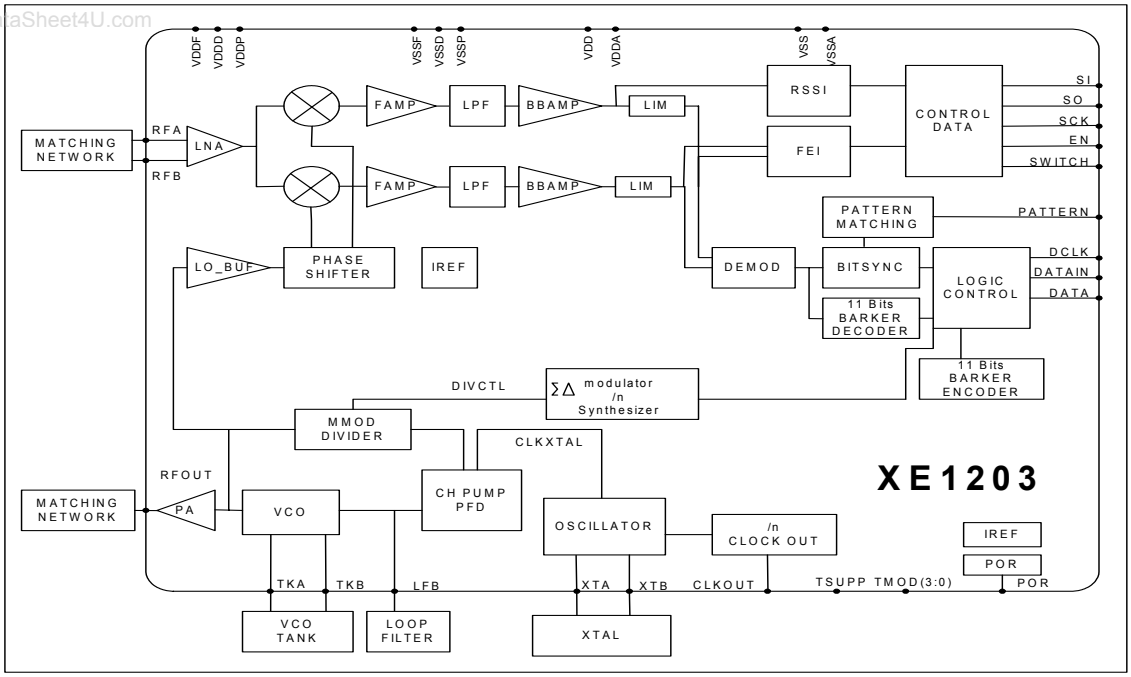


XE1203

433MHz / 868MHz / 915MHz

Low-power, integrated UHF transceiver

GENERAL DESCRIPTION

The XE1203 is a single chip transceiver operating in the 868 and 915MHz license-free ISM (Industry Scientific and Medical) frequency bands. Its highly integrated architecture allows for minimum external components while maintaining design flexibility. All major RF communication parameters are programmable and most of them can be dynamically set. The XE1203 offers the unique advantage of high data rate communication at rates up to 152.3kbit/s, without the need to modify the number or parameters of the external components. The XE1203 is optimized for low power consumption while offering high RF output power and exceptional receiver sensitivity. The device is suitable for circuit applications which have to satisfy either the European (ETSI-300-220) or the North American (FCC part 15) regulatory standards.

APPLICATIONS

- Automated Meter Reading (AMR)
- Home Automation and Access Control
- High-Quality Speech, Music and Data over RF
- Applications requiring Konnex-compatibility

KEY PRODUCT FEATURES

- RF output power: up to +15dBm on a 50 Ω load (typical)
- High reception sensitivity: down to –113 dBm (typical)
- Low power consumption:
  R_X = 14mA; T_X = 62 mA @15dBm (typical)
- Supply voltage down to 2.4V
- Data rate from 1.2 to 152.3kbps, NRZ coding
- Konnex-compatible operation mode
- 11-bit Barker encoder/decoder
- On-chip frequency synthesizer with steps of 500Hz
- Continuous phase 2-level FSK modulation
- Received data pattern recognition (for wake-up)
- Bit-Synchronizer for incoming data/clock synchronization and recovery
- RSSI (Received Signal Strength Indicator)
- FEI (Frequency Error Indicator)

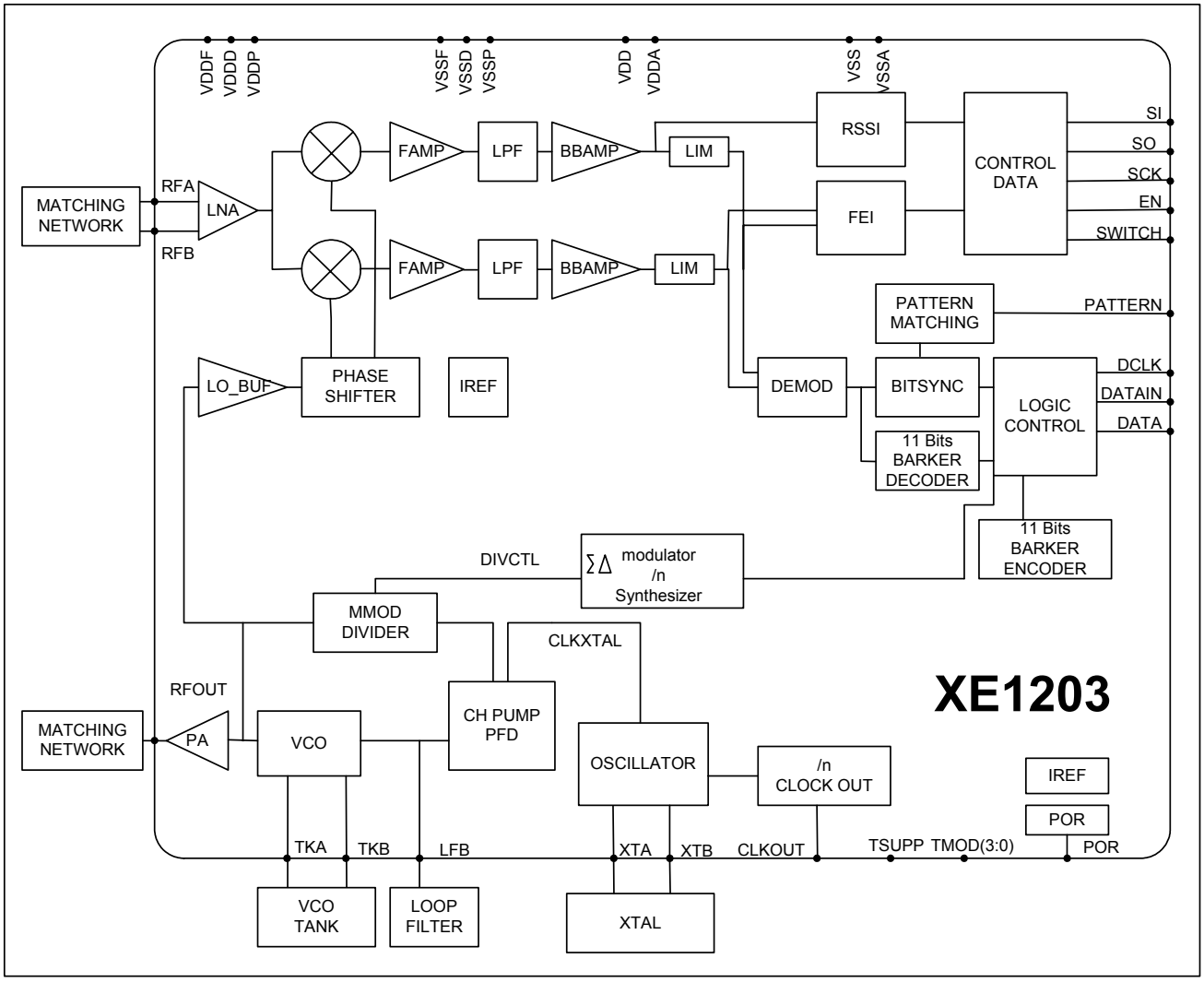
ORDERING INFORMATION

Part number	Temperature range	Package
XE1203I063	-40°C to +85°	VQFN48

Table of Contents

The XE1203 is a single-chip integrated circuit solution intended for use as a low cost FSK transceiver to establish a frequency-agile, half-duplex, bi-directional RF link, with NRZ (non-return to zero) data coding. Barker encoder/decoder hardware can be activated to modulate/demodulate the transmitted signal to reduce the effects of fixed-frequency in-band interference. The device is available in a VQFN48 package and is designed to provide a fully functional multi-channel FSK transceiver. It is intended for applications in the 868MHz European band and the North American 902-928MHz ISM band. The single chip transceiver operates down to 2.4 V and provides low power consumption solutions for battery-operated and power sensitive applications. The XE1203 is capable of operating data rates as high as 152.3 kbit/s. This makes it ideally suited for applications where high data rates are required.

1 FUNCTIONAL BLOCK DIAGRAM



2 PIN DESCRIPTION

PIN	NAME	I/O	Description
36	VDD	IN	VDD for low frequency digital blocks
18	VDDD	IN	VDD for high frequency digital blocks
29	VDDA	IN	VDD for low frequency analog blocks
12	VDDF	IN	VDD for high frequency analog blocks
10	VDDP	IN	VDD for the power amplifier
42	VSS	IN	VSS for low frequency digital blocks
19	VSSD	IN	VSS for high frequency digital blocks
27,25	VSSA	IN	VSS for low frequency analog blocks
4,16,13	VSSF	IN	VSS for high frequency analog blocks
7,8	VSSP	IN	VSS for the power amplifier
5	RFA	IN	RF input
6	RFB	IN	RF input
9	RFOUT	OUT	RF output
14	TKA	IN/OUT	VCO tank
15	TKB	IN/OUT	VCO tank
17	LFB	IN/OUT	Loop filter of the PLL
26	XTA	IN/OUT	Quartz and input of external clock
28	XTB	IN/OUT	Quartz
1,2,3,22,30,31,47,48			Not connected
39	SI	IN	Data input of the 3-wires interface
35	EN	IN	3-wire interface communication enable signal
38	SO	OUT	Data output of the 3-wires interface
40	SCK	IN	Input clock of the 3-wires interface
37	SWITCH	IN/OUT	Receiver or Transmitter mode selection
43	DCLK	OUT	Transmitter or Receiver clock
45	DATAIN	IN	Transmitter input data
44	DATA	IN/OUT	Transmitter input data or Receiver output data
41	CLKOUT	Out	Output clock at quartz frequency divided by 4, 8, 16 or 32
46	PATTERN	Out	Output of the pattern recognition block
11,20,21,23,24,32, 33, 34	Test pins	IN	Connected to ground

3 ELECTRICAL CHARACTERISTICS

3.1 ABSOLUTE MAXIMUM OPERATING RANGES

Stresses above those values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Description	Min.	Max.	Unit
VDDmr	Supply voltage	-0.5	3.9	V
Tmr	Storage temperature	-55	125	°C

The device is ESD sensitive and should be handled with precaution.

3.2 SPECIFICATIONS

3.2.1 Operating Range

Symbol	Description	Min.	Max.	Unit
VDDop	Supply voltage	2.4	3.6	V
TRop	Temperature	-40	85	°C
Clop	Load capacitance on digital ports	-	25	pF

3.2.2 Electrical Specifications

The table below gives the electrical specifications of the transceiver under the following conditions: Supply Voltage = 3.3 V, temperature = 25 °C, 2-level FSK without pre-filtering, fc = 915 MHz, Δf = 55 kHz, Bit rate = 4.8 kb/s, BW_{DSB} = 200 kHz, BER = 0.1 % (at the output of the bit synchronizer), matched impedances, environment as defined in section 6, unless otherwise specified.

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.2	1	µA
IDDST	Supply current in standby mode	Quartz oscillator (39 MHz) running	-	0.85	1.10	mA
IDDR	Supply current in receiver mode		-	14	17	mA
IDDT	Supply current in transmitter mode	RFOP = 5 dBm RFOP = 15 dBm	- -	33 62	40 75	mA mA
RFS	RF sensitivity	BR = 4.8 kbit/s Mode A	-	-113	-110	dBm
		BR = 4.8 kbit/s Mode B	-	-100	-97	dBm
		BR = 32.7 kbit/s Mode A	-	-107	-104	dBm
		BR = 32.7 kbit/s Mode B	-	-94	-91	dBm
	(*) Δf = 200 kHz, BW_{DSB} = 600 kHz	BR = 152.3 kbit/s Mode A (*)	-	-100	-97	dBm
		BR = 152.3 kbit/s Mode B (*)	-	-87	-84	dBm
RFSB	RF sensitivity with Barker Coding/decoding	BR = 1154 bit/s Mode A	-	-113	-110	dBm
		BR = 1154 bit/s Mode B	-	-100	-97	dBm
FDA	Frequency deviation	Programmable	1	-	255	KHz
CCR	Co-channel rejection		-13	-10	-	dBc
IIP3	Input intercept point	funw = f_{LO} + 1 MHz and f_{LO} + 1.945 MHz Mode A Mode B	 -43 -28	 -40 -25	 - -	 dBm dBm
ML	Receiver input level		-	-	-5	dBm
BW	Base band filter bandwidth DSB	Programmable	- -	200 600	- -	kHz kHz
ACR	Adjacent channel rejection	funw = f_{LO} + 650 kHz Pw= - 108 dBm (mode A)	45	48	-	dBc
BR	Bit rate	Programmable	1.2		152.3	kb/s
RFOP	RF output power	Programmable. On a 50 Ω load. RFOP10 RFOP1 RFOP20 RFOP2	 -3 +2 +7 +12	 0 +5 +10 +15	 - - - -	 dBm dBm dBm dBm
FR	Synthesizer frequency range	Programmable Each range with its own external components	433 868 902	- - -	435 870 928	MHz MHz MHz
TS_TR	Transmitter wake-up time	From oscillator running	-	200	250	µs
TS_RE	Receiver Baseband wake-up time	From oscillator running	-	1.5	1.8	ms

Symbol	Description	Conditions	Min	Typ	Max	Unit
TS_RSSI	RSSI wake-up time	From receiver running	-	-	1	ms
TS_OS	Quartz oscillator wake-up time	Fundamental	-	1	2	ms
		3rd overtone	-	7	-	ms
TS_FEI	FEI wake-up time		-	-	2/BR	ms
TS_SYNC_AQ	Time for synchronization of the barker decoder	Input power of –106 dBm Data rate = 1154 bps Chip rate = 12.7 kcps From Rx running	-	5	-	ms
XTAL	Quartz oscillator frequency	Fundamental or 3rd overtone	-	39	-	MHz
FSTEP	Frequency synthesizer step	Exact step is XTAL / 77'824	-	500	-	Hz
VTHR	Equivalent input thresholds of the RSSI	Mode A				
		Low range:VTHR1	-	-100	-	dBm
		VTHR2	-	-95	-	dBm
		VTHR3	-	-90	-	dBm
		High range:VTHR1	-	-85	-	dBm
		VTHR2	-	-80	-	dBm
		VTHR3	-	-75	-	dBm
SPR	Spurious emission in receiver mode		-	-55	-50	dBm
VIH	Digital input level high	in % VDD	75	-	-	%
VIL	Digital input level low	in % VDD	-	-	25	%
VOH	Digital output level high	in % VDD	75	-	-	%
VOL	Digital output level low	in % VDD	-	-	25	%

4 GENERAL DESCRIPTION

The XE1203 is a direct conversion (Zero-IF) half-duplex data transceiver. It includes a receiver, a transmitter, a frequency synthesizer and some service blocks. The circuit operates in three frequency ranges (433 MHz, 868MHz and 915MHz) and uses 2-level FSK modulation. In a typical application, the XE1203 is programmed by a microcontroller through the 3-wire serial bus SI, SO, SCK to write to and read from the configuration registers.

The XE1203 consists of 4 main functional blocks.

The receiver converts the incoming 2-level FSK modulated signal into a synchronized bit stream. The receiver is composed of a low-noise amplifier, down-conversion mixers, base band filters, base band amplifiers, limiters, demodulator and bit synchronizer. The bit synchronizer transforms the data output of the demodulator into a glitch-free bit stream DATA and generates a synchronized clock DCLK to be used to sample the DATA signal easily without loading an external processor with heavy signal processing. In addition, the receiver includes a Received Signal Strength Indicator function (RSSI), a Frequency Error Indicator function (FEI) that gives indication about the frequency error of the local oscillator, and pattern recognition function to detect programmable reference word in the incoming bit stream. A user-selectable Barker coding/decoding block can be activated to spread the data with an 11-bit Barker code upon transmission and decode the data upon reception by making a correlation between the spread data and the same 11-bit Barker code. The bandwidth of the base-band filters, the frequency deviation of the expected incoming FSK signal as well as the bit rate of this bit stream are programmable.

The transmitter performs the modulation of the carrier by an input bit stream and the transmission of the modulated signal. The modulation is made directly through the frequency synthesizer. An on-chip power amplifier then amplifies the signal. The output power is programmable among 4 possible values. The frequency deviation and the bit rate for the transmit signal are the same as those programmed for the receiver section.

The frequency synthesizer generates the local oscillator (LO) signal for the receiver section as well as the FSK modulated signal for the transmitter section. The core of the synthesizer is implemented with a Delta-Sigma PLL architecture. The frequency is programmable with a step of 500 Hz in 3 frequency bands, 433-, 868-, and 915-MHz. This section includes a crystal oscillator whose signal is the reference for the PLL. This reference frequency can also be used as a reference clock for the external microcontroller through CLKOUT pin with a user selectable division ratio of 4,8,16 or 32.

The control block generates the control signals according to the setting in its set of configuration registers.

The service block performs all the necessary functions for the circuit to work properly, including the internal voltage and current sources.

4.1 DETAILED DESCRIPTION

4.1.1 Introduction

The pin DATA is used in both transmitter and receive sections and by default it is set to bidirectional mode. In receiver mode, DATA holds the recovered information. In transmitter mode, the information to be sent applied to this pin. If a unidirectional mode is required, the user has to set ADParam_disable_data_bidir to ‘1’. In this case, pin DATA in an output mode used by receiver section and pin DATAIN is used for transmit data.

4.1.2 Receiver

The receiver section has two output signals indicating recovered clock (pin DCLK) and recovered NRZ data (pin DATA). The bit synchronizer controls the recovered clock DCLK pin. If the bit synchronizer is enabled by setting the bit “RTParam_Bitsync” to “1” the DCLK pin outputs the clock recovered from the incoming data stream. Disabling bit synchronizer holds the DCLK pin at low level and connects the demodulator output to DATA pin.
The function of bit synchronizer is to remove the glitches from the bit stream DATA and to provide the synchronous output clock at DCLK. The output DATA is valid at the rising edge of the DCLK.

4.1.3 Demodulation chain

The demodulation part is composed of an FSK demodulator, a bit synchronizer, a barker decoder and a Pattern Recognition block. The next figure shows the interaction between each block.

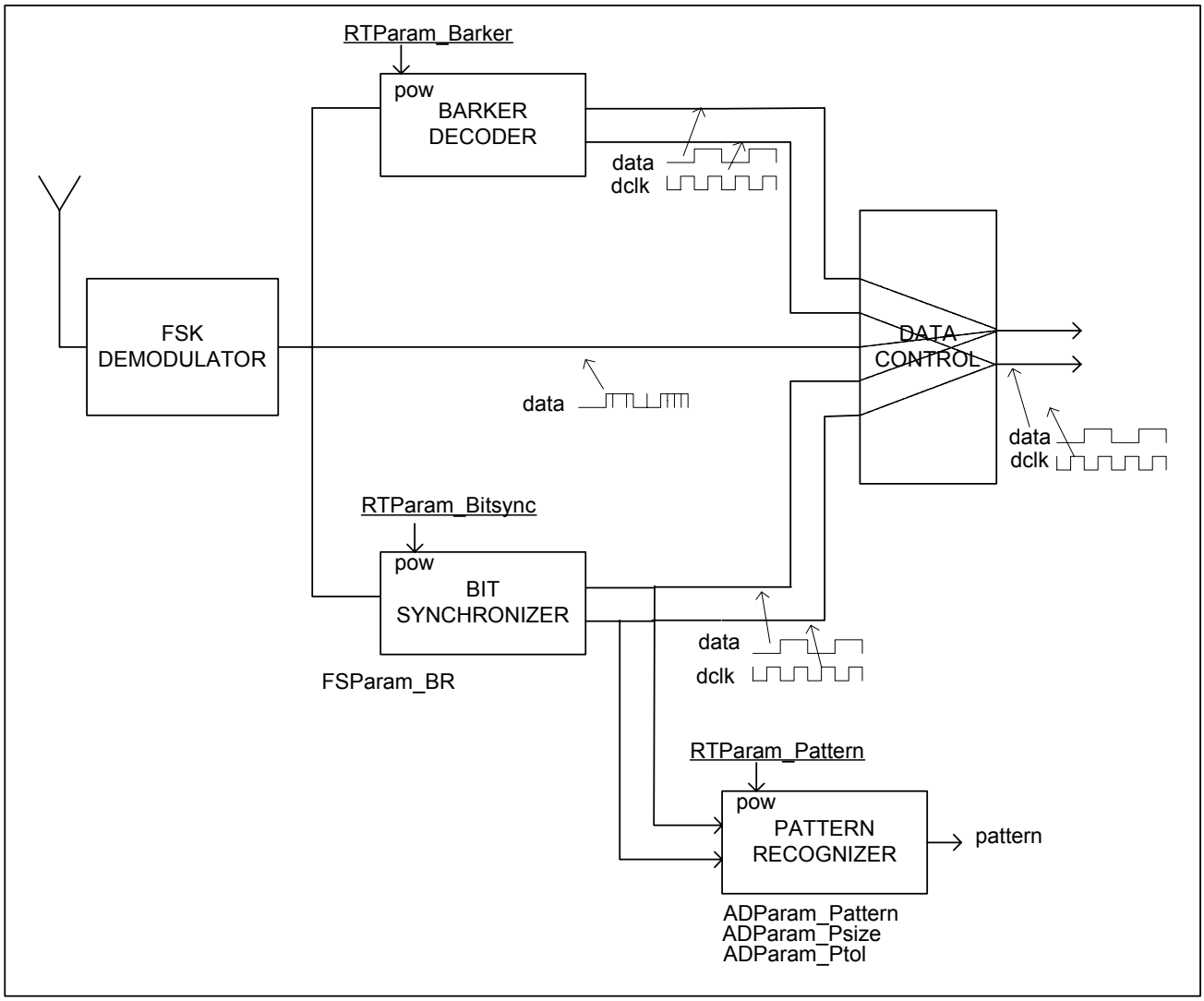


Figure 1 Demodulation architecture.

4.1.4 Demodulator

The demodulator provides a bit stream from the received FSK modulated base band limited signals, I_lim and Q_lim. If RTParam_bsync and RTParam_Barker bits are set low, i.e disabled, then the demodulator output is directly connected to the DATA pin and the DCLK pin is set to low.

The modulation index required for proper operation of the demodulator is:

$$\beta = \frac{2 \cdot \Delta f}{BR} \geq 2,$$

where Δf corresponds to the frequency deviation and BR corresponds to the bit rate.

4.1.5 Bit synchronizer

The output of the demodulator has glitches and jitters. The bit synchronizer transforms the data output of the demodulator into a glitch-free bit stream DATA and generates a synchronized clock DCLK to be used for sampling the DATA output (see below).

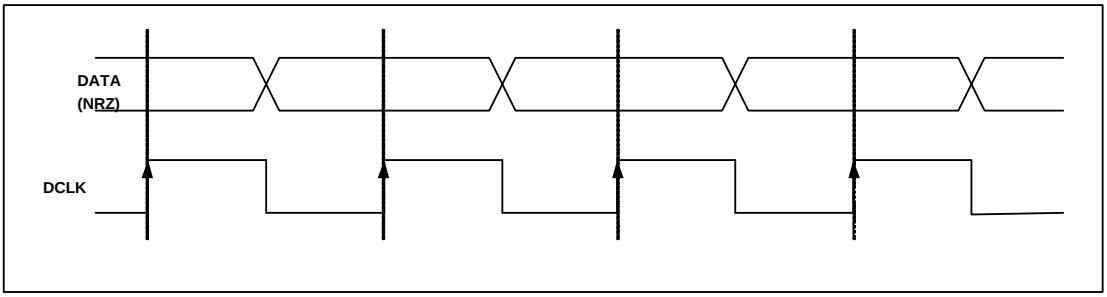


Figure 2. Bit synchronizer timing diagram.

To ensure proper behaviour of the bit synchronizer, three conditions have to be satisfied: A preamble of 24 bits is required for the synchronization; this preamble must be a sequence of “0” and “1” sent alternatively, during transmission of data, the bit stream must have at least one transition from “0” to “1” or from “1” to “0” every 8 bits. The accuracy of the bit rate must be better than ± 5 %. The bit synchronizer is on when RTParam_Bsync is high. FSParam_BR defines the bit rate in the following way.

$$\text{Bit rate} = \frac{152.34e3}{\text{int}(\text{FSParam\_BR}(6:0))+1},$$

where int(x) is the integer value of the unsigned binary representation of x.

If the Konnex standard is used then the bit rate is fixed and equal to 32.77 Kbps. The register FSParam_OSR (address “00101”) has to be set to “00011110” , the register FSParam_BR(6:0) has to be set to “000X0000” and the bit FSPARAM_Change_Osr has to be set to ‘1’.^

4.1.6 Barker decoder

The Barker decoder is an alternative to the bit synchronizer for a **fixed data rate of 1154 bps**. The barker block is selected in receiver mode when RTParam_Barker is high. In transmission, the information data at a bit rate of 1154 bps is spread using an 11 bits barker code. The result is a bit stream at 12.7 Kilo chips per second (Kcps), which is applied to the frequency synthesizer. At the receiver part, the signal is demodulated using the FSK demodulator (at 12.7 Kcps) and fed to the Barker decoder that provides a information data stream (1154 bps) and a synchronized clock to sample it.
The following figure describes the coding/decoding process.

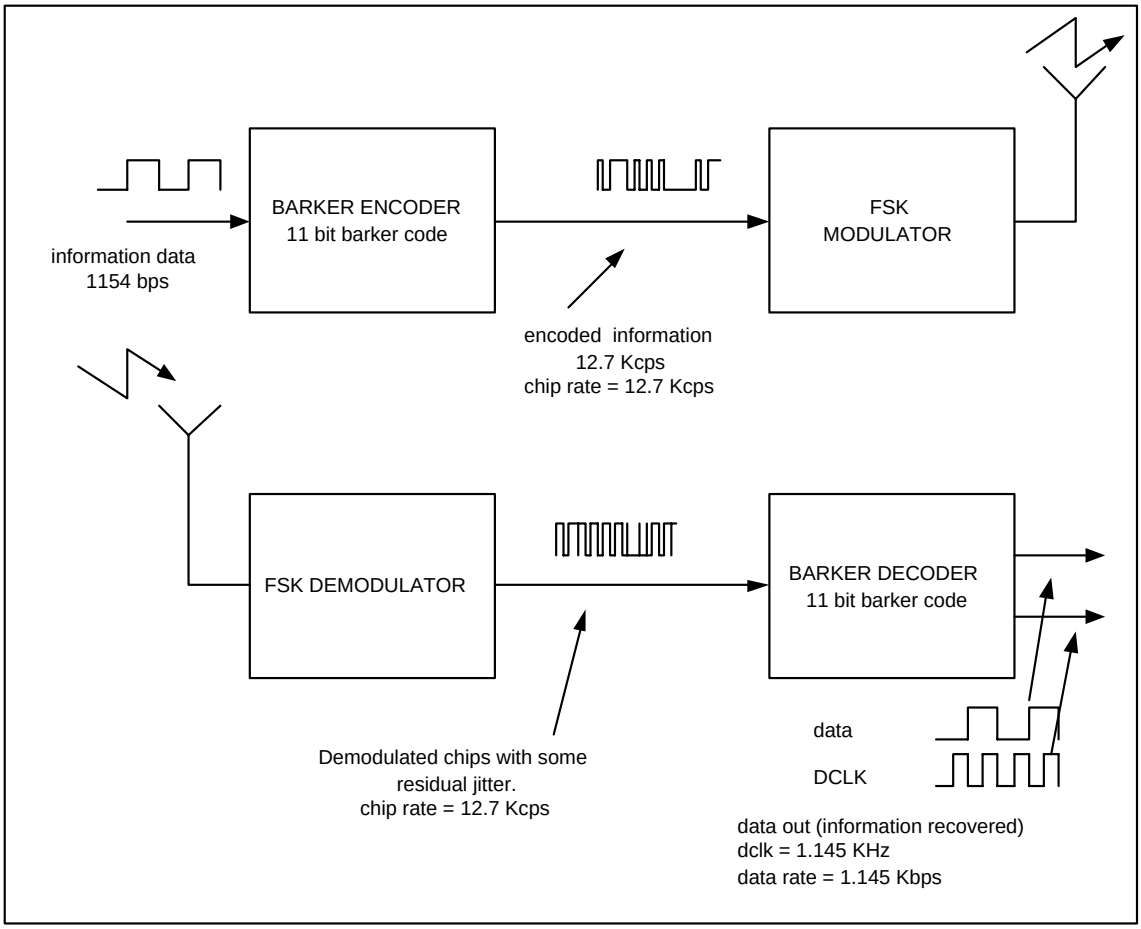


Figure 3. Data encoding decoding channel.

In reception mode, the chip provides a clock (DCLK) to a microcontroller. The data can be sampled at the rising edge of the clock. When using the barker coding decoding process, DCLK is used to detect the sync acquisition. If there is no valid data, DCLK remains high. The first falling edge of the clock means that the sync acquisition phase is reached and the data has became available. The next figure shows the data exchange during the reception mode.

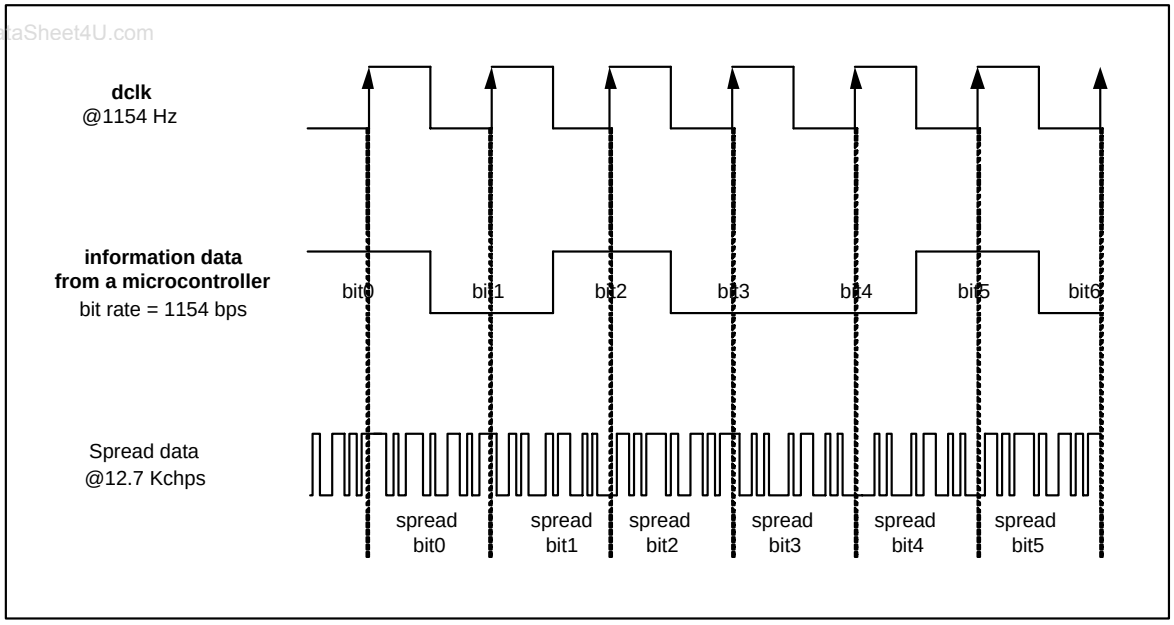


Figure 4 Data exchange during reception mode when barker scheme is used.

4.1.7 Pattern recognition block

This feature can be activated by setting RTParam_Pattern to high while in receiver mode. The incoming NRZ bit stream is compared with a pattern stored in PATParam_Pattern registers. The PATTERN output is driven by the output of this comparator and is synchronized by DCLK. It is set to high when a matching condition is detected, otherwise set to low. PATTERN output is updated at the rising edge of DCLK. The number of bits used for comparison is defined in ADParam_Psize register and the number of tolerated errors for the pattern recognition is defined in ADParam_Ptol register. The next figure shows the pattern matching operation.

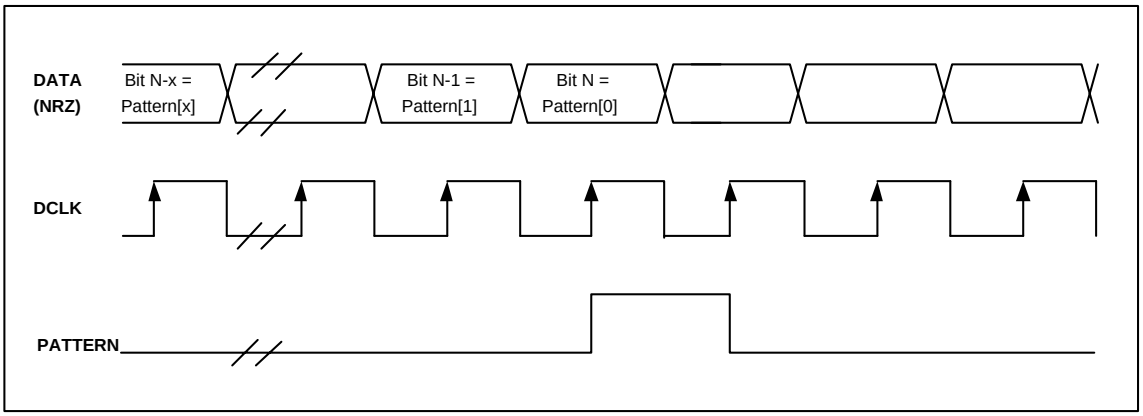


Figure 5. Pattern matching operation.

4.1.8 High sensitivity vs. high linearity: A-mode, B-mode

The receiver can be operated in two different modes that provide the highest sensitivity or the highest linearity. Two operating mode is selectable via the registers "SWParam_Rmode1" or "SWParam_Rmode2" (see the Configuration register section). In A-mode, the receiver has the highest sensitivity (see RFS parameter) and in B-mode, the receiver has the highest linearity (see IIP3 parameter)

4.1.9 RSSI

This function provides a Received Signal Strength Indication based on the signal level at the output of the base-band filter. To activate this function, the bit "RTParam_RSSI" (see the Configuration register section) must be set to "1". When activated, the 2-bits status information is stored in register "DataOut_RSSI" and can be read through the serial control interface. The meaning of this status information is given in the table below, where V_{RFFIL} is the differential amplitude of the equivalent input RF signal when the receiver is operated in A-mode. The thresholds VTHRi are the thresholds at the output of the base-band filter divided by the gain between the input of the receiver and this output.

DataOut_RSSI	Description
0 0	$V_{RFFIL} \leq$ VTHR1
0 1	VTHR1 < $V_{RFFIL} \leq$ VTHR2
1 0	VTHR2 < $V_{RFFIL} \leq$ VTHR3
1 1	VTHR3 < V_{RFFIL}

Table 1 RSSI status description

The operating range of RSSI measurement can be changed by programming RTParam_RSSIR register, this way two ranges with three VTHRi values can be selected. The time diagram of an RSSI measurement is given in the next figure. When the RSSI function has been activated the signal strength is periodically measured and the result is stored in the register "DataOut_RSSI" each time "DataOut_RSSI" is read via the 3 wires interface. TS_RS is the wake-up time required after the function has been activated to get a valid result.

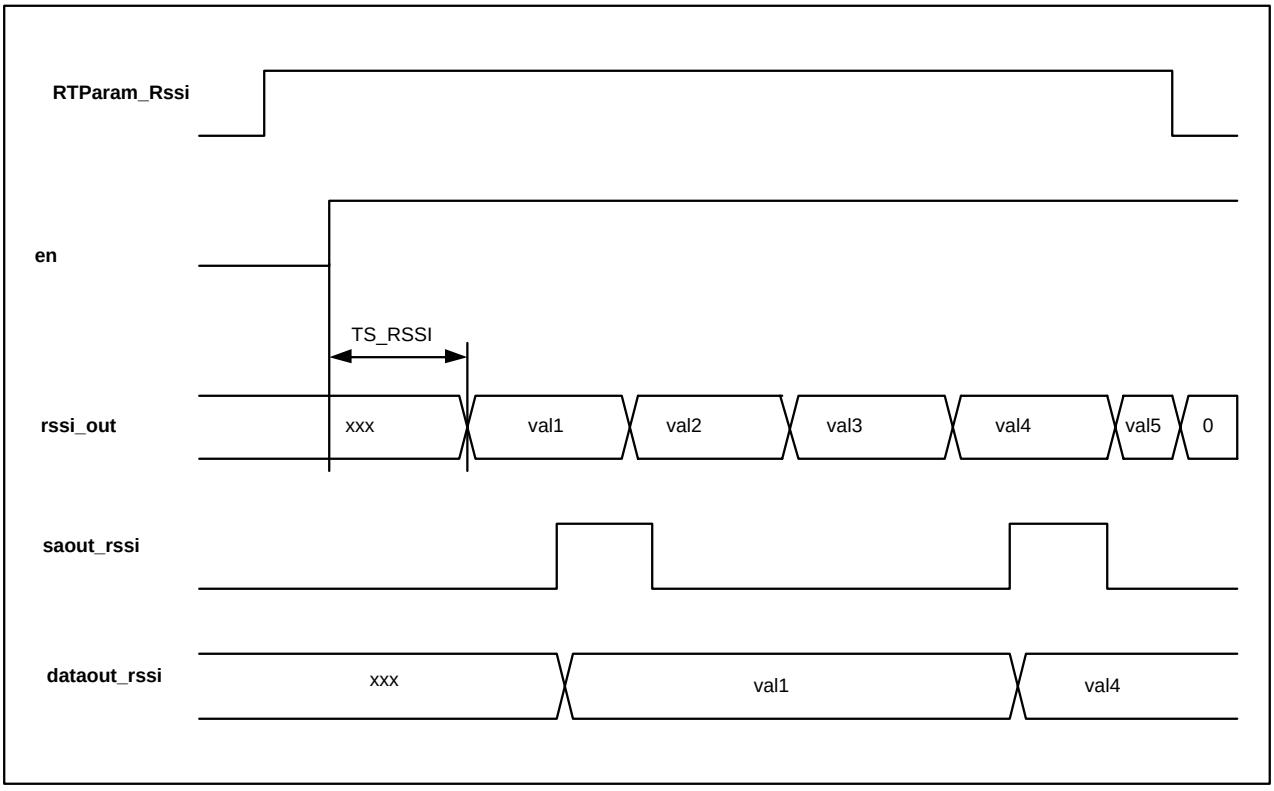


Figure 6. RSSI measurement timing diagram

Saout_rssi is internally generated signal during a read sequence of DATAOUT_RSSI register and used for updating Dataout_RSSI register. The next figure shows the timing diagram of the saout_rssi generation.

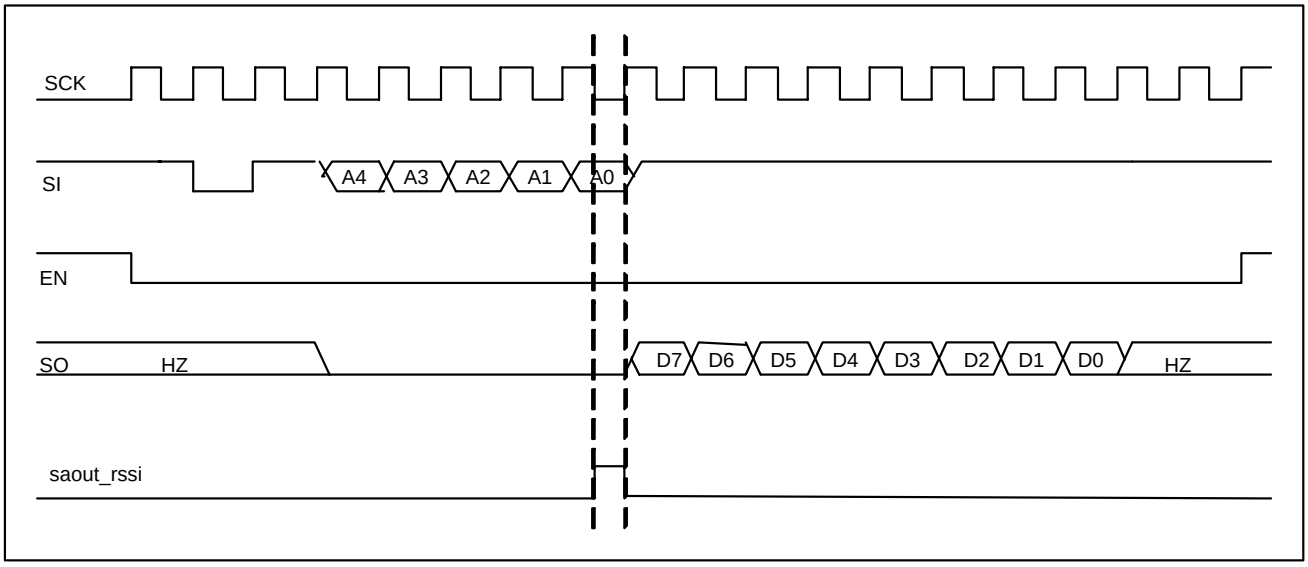


Figure 7. Generation of saout_rssi

The maximum frequency of SCK during the read operation of the RSSI value is 100 KHz.

4.1.10 Frequency Error Indicator - FEI

This function provides information about the frequency error of the local oscillator compared with the input carrier frequency and can be used to implement AFC. The condition on the modulation index for proper behaviour of the FEI function is:

$$\beta = \frac{2 \cdot \Delta f}{BR} \geq 2,$$

where Δf is the frequency deviation and BR is the bit rate.

IMPORTANT NOTE

The time diagram of an FEI measurement is given in the next figure. When the FEI block has been woken up and is ready, and as long as the block is kept on, the frequency error is measured and the current result of the measurement is loaded in the register “Dataout_MSB_fei” and “Dataout_LSB_fei ‘’ each time the “Dataout_LSB_fei ‘’ register is read. TS_FEI is the time required for the first evaluation to be completed after the block has been started up and its value is given in section 3.2. Since the contents of the configuration register is validated at the rising edge of the enable signal “en”, the FEI block is actually started up at this time.

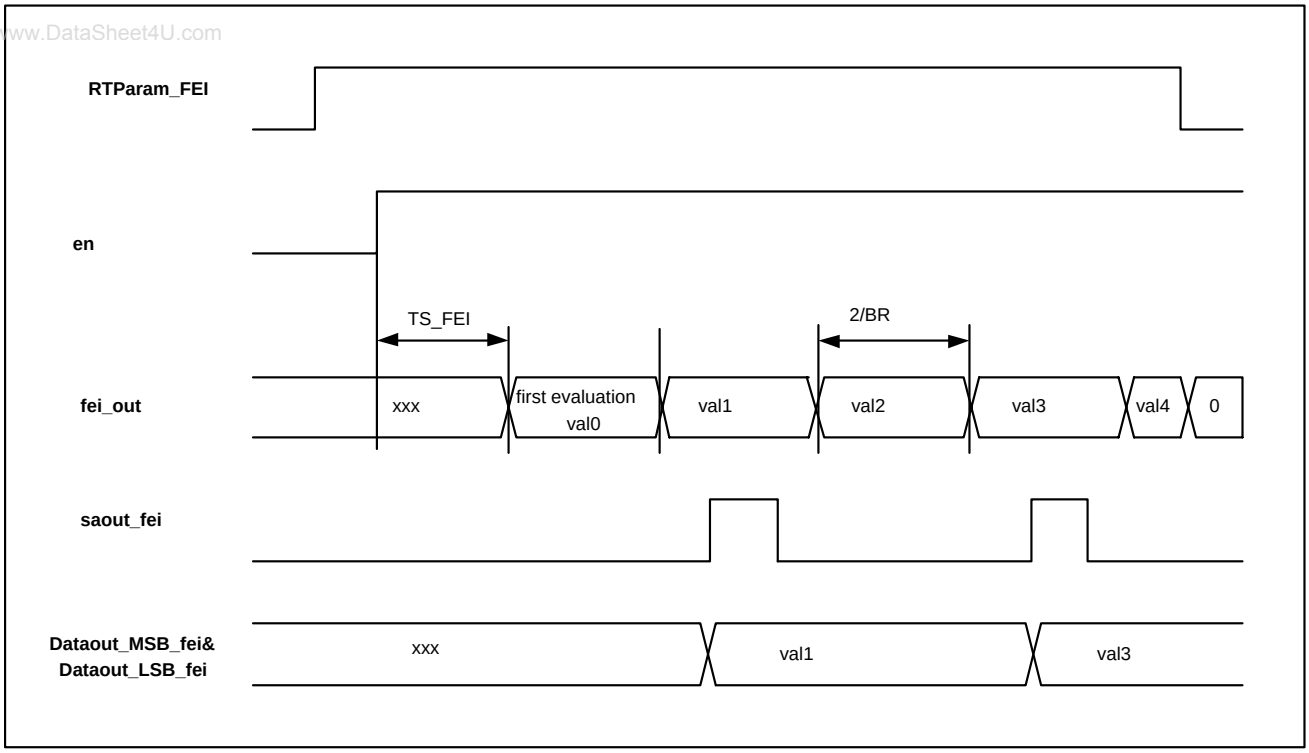


Figure 8 Time diagram of an FEI measurement.

To guarantee proper behaviour of the FEI, the sum of the frequency offset and the signal bandwidth (single sided) should be lower than the baseband filter bandwidth (single sided). That is:

$$F_{offset} + SignalBW < Baseband\_filterBW.$$

Where f_{offset} is the difference between the carrier frequency and the LO frequency, SignalBW is the signal bandwidth (single side) equal to the sum of the bit rate divided by 2 and the frequency deviation (BR/2 + DF), and Baseband_filterBW is the channel filter bandwidth defined by RTParam_BW parameters.

The **frequency error** can be calculated by the following formula:

The frequency error = (BR/8)*int(Dataout_FEI(11:0)),

Where Dataout_FEI(11:0) = Dataout_MSB_fei(3:0) & Dataout_LSB_fei(7:0) and int(x) is the integer value of the **signed binary** representation of x.

Saout_fei is internally generated during a read sequence of “Dataout_LSB_fei ‘’ register in the same way as saout_rssi. The maximum frequency of SCK during the read operation of the RSSI value is 100 KHz.

When using the Konnex standard, the bit ADParam_enable_konnex (address “01111”) has to be set to ‘1’.

4.1.11 Transmitter

The transmit data should be applied to DATA or DATAIN pins depending on the ADParam_disable_data_bidir register setting. If it is set to high (“1”) the DATAIN pin is used otherwise bidirectional pin DATA is used for transmit data. The modulation of LO with the data applied can be performed with pre-filtering or without. The pre-filtering can be selected by setting RTParam_Filter register to high (“1”). So, the modulation of the LO frequency by the bit stream can be made in two ways:

- The input bit stream is directly applied to the frequency synthesizer without any pre-filtering,
- The input bit stream is pre-filtered before being applied to the frequency synthesizer; with this filtering, each edge of the bit stream is linearly smoothed with a staircase transition.

The two possible ways of modulation are shown in figure 4-9, where “datain” is the input bit stream.

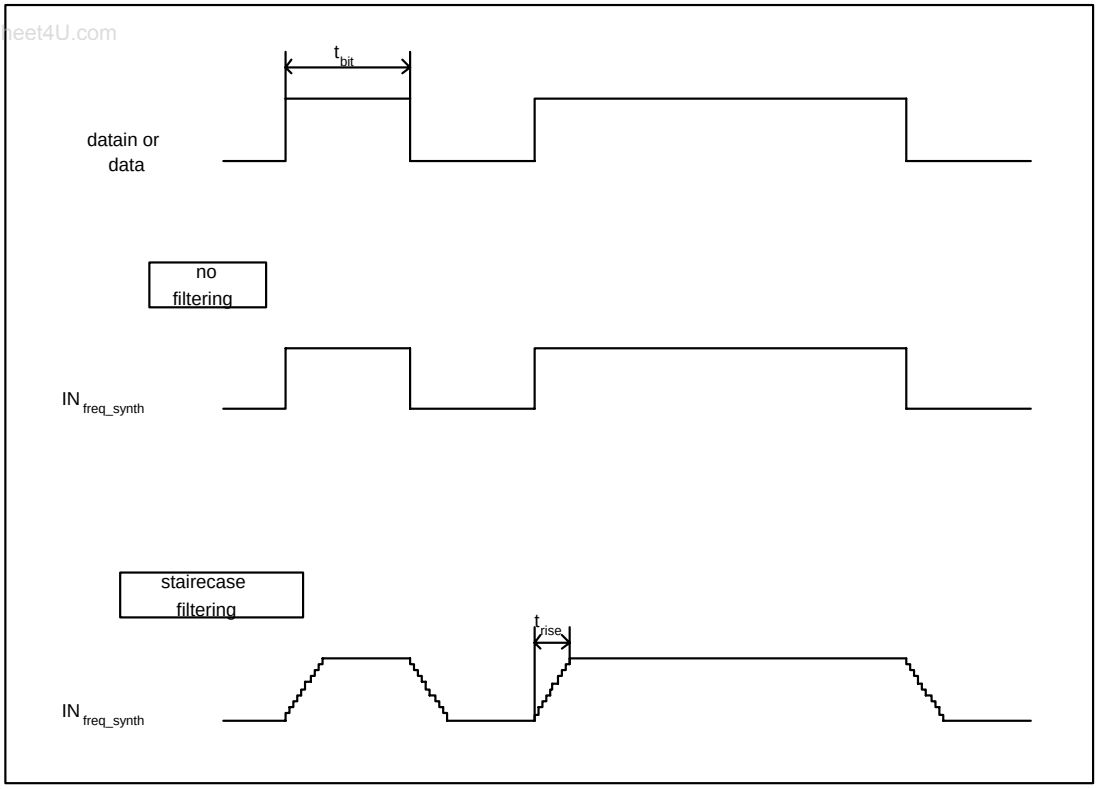


Figure 9. Modulation with and without pre-filtering

The characteristic of the filtering is the ratio t_{rise}/t_{bit}. The value of this ratio is programmable on two values with the register “RTParam_Stair”, as shown in the following table.

RTParam_Stair	t_{rise}/t_{bit}
0	10 %
1	20 %

When using the filtering option i.e. “RTParam_Filter” set “1”, only the following bit rates and frequency deviations can be used.

FSParam_Dev	Frequency deviation
00101000	40 kHz
00110111	55 kHz
01010000	80 kHz
10100000	160 kHz
11001000	200 kHz

FSParam_Br	Bit rate (bps)
1111110	1200
0111111	2400
0011111	4800
0001111	9600
0000111	19200
0000011	38400
0000001	76800
others	153000

If ADParam_enable_konex is high, then the filtering option is available for a bit rate of 32.7 kbps and one of the frequency deviations defined above.

4.1.12 Barker encoding.

When using the barker encoding in transmitter mode, the RTParam_barker parameter has to be set to “1” and the information data stream at 1154 bps is applied through the pin DATA or DATAIN according to the ADParam_disable_data_bidir parameter. This data is spread into a chip stream at 12.7 Kchps into the barker encoder. This chip stream is directly applied to the frequency synthesizer without any pre-filtering.

The DCLK pin is used for data clock in the transmission mode and this clock is generated by XE1203. The DCLK is applied to the microcontroller, at the falling edge of the each clock a new data bit is supplied by microcontroller. The data is sampled by XE1203 at the rising edge of DCLK and spread by using an 11-bit length Barker code. The following figure shows the data exchange during the transmission mode when barker option is used.

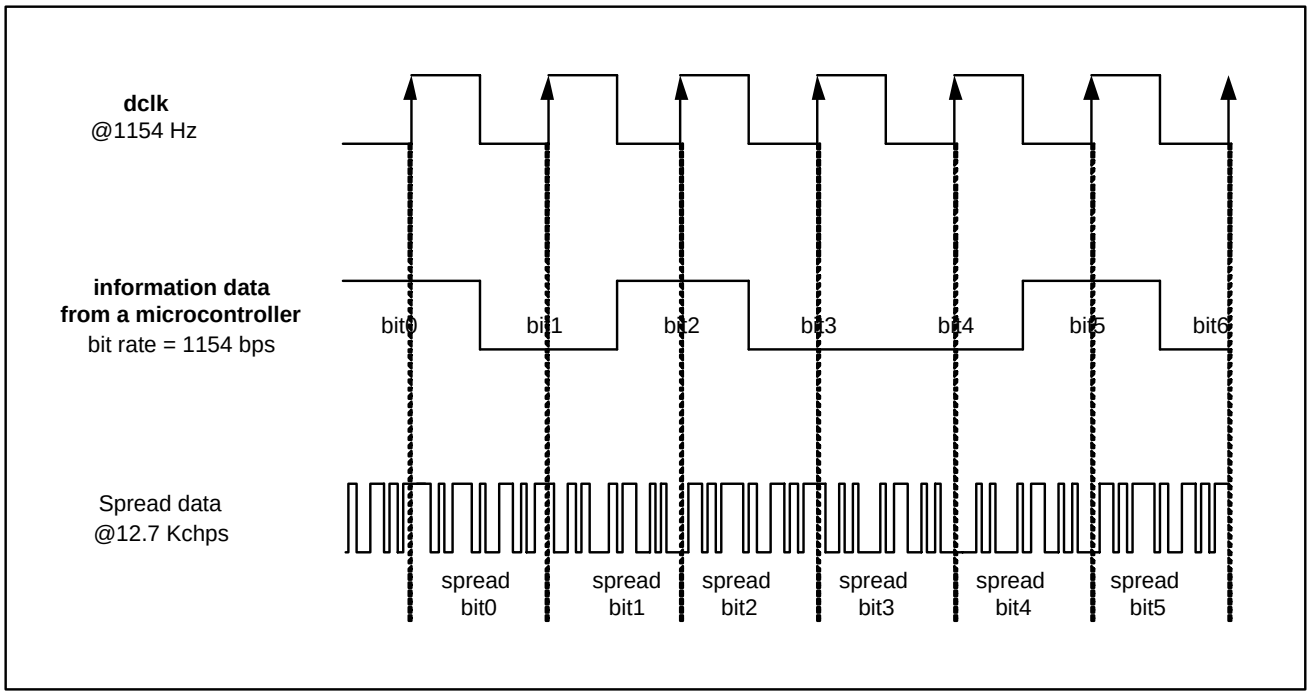


Figure 10 Data exchange during transmission mode.

4.1.13 Clock Output for external processor

A reference clock could be generated by XE1203 to the external microcontroller. RTParam_Clkout register controls the CLKOUT pin. When it is set to high then CLKOUT is activated. The generated clock can be 1/4, 1/8, 1/16 or 1/32 of the XE1203 reference oscillator. The different divider ratios can be selected by programming “ADParam_Clkfreq” register (see the Configuration register section below). The reference oscillator frequency of 39MHz can result 1.22, 2.44, 4.87 or 9.75MHz clock at the CLKOUT pin. This clock is stopped in Sleep Mode.

5 INTERFACE DEFINITION, PRINCIPLES OF OPERATION

5.1 SERIAL CONTROL INTERFACE

A 3-wire bi-directional bus (SCK, SI, SO) is used to communicate with XE1203. SCK and SI are input signals supplied externally, for example by the microcontroller. The XE1203 configures the SO signal as an output pin during read operation, and it is tri-stated in other modes. The falling edge of the SCK signal is used to sample the SI pin to write data into the internal shift register of the XE1203. The rising edge of the SCK signal is used to output data to SO pin by XE1203, so the microcontroller should sample data at the falling edge of SCK.

The signal EN must be low during the whole write and read sequences. In write mode the actual content of the configuration register is updated at the rising edge of the EN signal. Before this, the new data is stored in temporary registers whose content does not affect the transceiver settings.

The timing diagram of a write sequence is given in the figure below. The sequence is initiated when a Start condition is detected, that is when the SI signal is set to “0” during a period of SCK. The next bit is a read/write (R/W) bit which should be “0” to indicate a write operation. The next 5 bits are the address of the control register A[4:0] to be accessed, MSB first. Then, the next 8 bits are the data to be written in the register. The sequence ends with 2 stop bits set to “1”. The data on SI should change at the rising edges of SCK, and is sampled at the falling edge of SCK. After the 2 stop bits, the data transfer is terminated. The SI line should be at “1” for at least one clock cycle on SCK before a new write or read sequence can start. In doing this, users can do multiple registers write without rising EN signal in between. The duty cycle of SCK must be between 40 % and 60 % and the maximum frequency of this signal is 1 MHz except when reading the RSSI output and FEI output where the maximum frequency of SCK is limited to 100 KHz. Over the operating supply and temperature range, set-up and hold time for SI on the falling edge of SCK are 200ns.

The register at address 0 is one bit length and used to define the configuration of the chip. When writing in this register, the sequence described above is valid except that only one bit data is needed instead of 8 bits. If a unique write procedure is used for all registers then, when writing at address 0, 8 data bit are sent but only the MSB is valid and written at address 0. The remaining 7 data bits must be all ones.

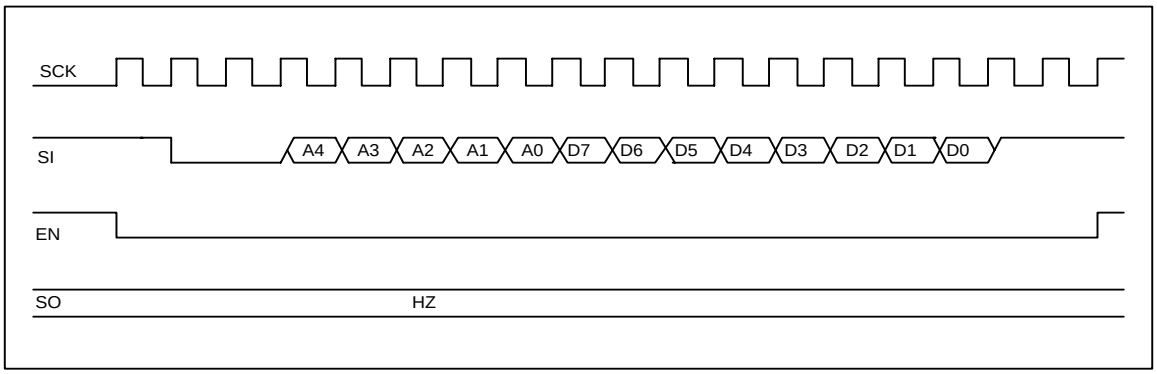


Figure 11 Write sequence into configuration register

The following figure shows a write sequence at address zero.

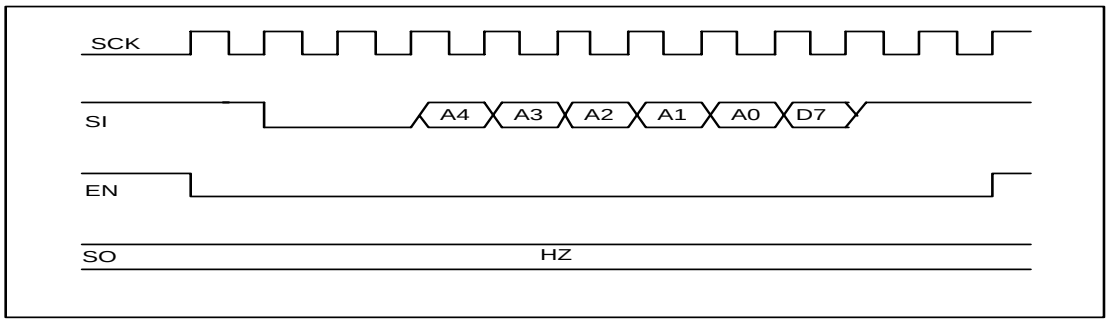


Figure 12 Write sequence into configuration register at address zero.

The time diagram of a read sequence is given in figure below. The sequence is initiated when a Start condition is detected, that is when the SI signal is set to “0” during a period of SCK. The next bit is a read/write (R/W) bit which should be “1” to indicate a read operation. The next 5 bits are the address of the control register A[4:0] to be accessed, MSB first. Then the data from the register are transmitted on the SO pin. The data become valid at the rising edges of SCK and should be sampled at the falling edge of SCK. After this, the data transfer is terminated. The SI line must stay high for at least one clock cycle on SCK to start a new write or read sequence. The maximum current drive on SO is 2mA @ 2.7V, the maximum load is CLop.

When the serial interface is not used for read or write operations, both SCK and SI should be set to “1”. Except in read mode, SO is set to “HZ”.

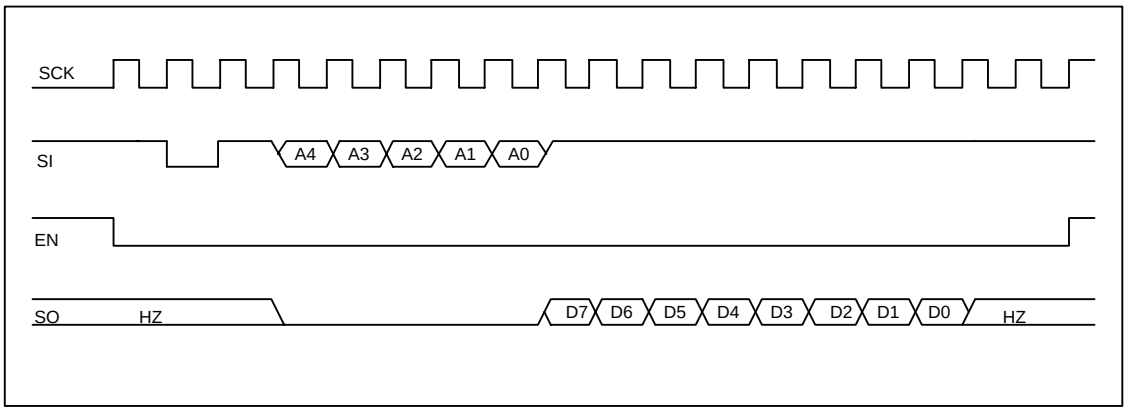


Figure 13 Read sequence of configuration register.

When reading the register at address zero, the timing diagram is the following one.

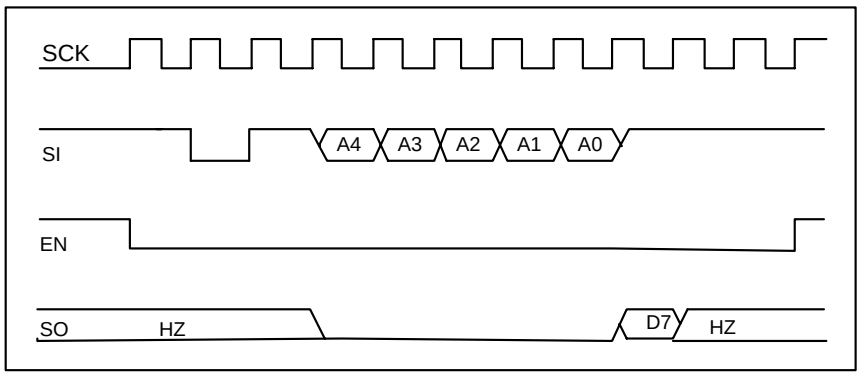


Figure 14 Read sequence of configuration register at address 0.

5.2 CONFIGURATION AND STATUS REGISTERS

The transceiver has several operating modes and parameters, which can be selected by the user. Some of these modes and all the parameters are stored in an internal configuration register that can be accessed by the microcontroller through a 3-wires serial interface. The switching option allows some parameters to be changed rapidly; defined in SWParam registers, by using the 3-wire interface in a reduced sequence or by using a single input pin SWITCH.

The configuration is defined by the Chip_Config parameter (address 0) when RTParam_Switch_ext is low or by the pad SWITCH when RTParam_Switch_ext is high. Using Chip_config or SWITCH allows switching between a set of two predefined parameters of the transceiver. If a parameter must not change then it must be set at the same value in the two registers used to define it. To switch between configurations, the new value of Chip_config or SWITCH should be modified when the EN signal is low. The actual change will be applied to the transceiver upon the rising edge of the EN signal. The following table summarizes the chip configuration programming.

Chip_config Address 0	SWITCH (pad)	RTParam_switch_ext	Registers used
0	Pad SWITCH is an output : '1' in transmitter mode '0' in the other mode	0	SWParam_mode_1 SWParam_Power_1 SWParam_Rmode_1 SWParam_t_delsig_in_1 SWParam_freq_1
1	Pad SWITCH is an output : '1' in transmitter mode '0' in the other mode	0	SWParam_mode_2 SWParam_Power_2 SWParam_Rmode_2 SWParam_t_delsig_in_2 SWParam_freq_2
X	0	1	SWParam_mode_1 SWParam_Power_1 SWParam_Rmode_1 SWParam_t_delsig_in_1 SWParam_freq_1
X	1	1	SWParam_mode_2 SWParam_Power_2 SWParam_Rmode_2 SWParam_t_delsig_in_2 SWParam_freq_2

By default Configuration 1 is used and RTParam_switch_ext is set to '0'.

5.2.1 Configuration register: general description

Name	Size	Address	Description
CONFIG	1 x 1	0	Switch configuration
RTParam	2 x 8	00001 - 00010	Parameters of the receiver and transmitter
FSParam	3 x 8	00011 - 00101	Frequency parameters
SWParam	6 x 8	00110 - 01011	Switching parameters
DataOut	2 x 8	01100 - 01101	Data provided by internal blocks of the transceiver
ADParam	5 x 8	01110 - 10010	Additional parameters
Pattern	4 x 8	10011 - 10110	Reference pattern for the "pattern recognition" function

In addition, 9 bytes at addresses 10011 to 11 100 are reserved for test purposes.

Name	Size	Address	Description
Test	9 x 8	10 011 – 11 100	Test of the circuit (reserved)

All the bits that are referred as "reserved" in the table above and in the following ones should be set to "0".

5.2.2 RTParam configuration register

The detailed description of the “RTParam” register is given in the next table.

Name	Bits	Address	Description
Chip_config	0	00000	Chip configuration: 0 -> config 1 1 -> config 2
RTParam_Bitsync	7	00001	Bit synchronizer on/off: 0 -> off 1 -> on
RTParam_Barker	6	00001	BARKER on/off: 0 -> off 1 -> on
RTParam_Rssi	5	00001	RSSI_on/off: 0 -> off 1 -> on
RTParam_Rssir	4	00001	Range of the RSSI: 0 -> low range 1 -> high range
RTParam_Fei	3	00001	FEI on/off 0 -> off 1-> on
RTParam_Bw	2	00001	Bandwidth of the BB filter 0 -> 200 KHz (DSB) 1 -> 600 KHz (DSB)
RTParam_Osc	1	00001	Source of reference frequency 0 -> internal quartz oscillator 1 -> external signal
RTParam_Clout	0	00010	Enable of clkout: 0 -> no signal provided on pad clkout 1 -> signal at quartz frequency divided by 4,8,16,or 32 provided on pad clkout (9.75MHz down to 1.22 MHz)
RTParam_Stair	7	00010	Rising and falling times in case of pre-filtering in transmitter mode: 0 -> 10 % of bit duration 1 -> 20 % of bit duration

Name	Bits	Address	Description
RTParam_Filter	6	00010	Pre-filtering of the bit stream in transmitter mode 0 -> no filtering 1 -> filtering The filtering function is available only for the following bit rates and frequency deviations: FSPanam_Br = "1111110" -> BR = 1200 bps FSPanam_Br = "0111111" -> BR = 2400 bps FSPanam_Br = "0011111" -> BR = 4800 bps FSPanam_Br = "0001111" -> BR = 9600 bps FSPanam_Br = "0000111" -> BR = 19200 bps FSPanam_Br = "0000011" -> BR = 38400 bps FSPanam_Br = "0000001" -> BR = 76800 bps FSParam_Dev = "00101000" -> Δf = 40 kHz FSParam_Dev = "00110111" -> Δf = 55 kHz FSParam_Dev = "01010000" -> Δf = 80 kHz FSParam_Dev = "10100000" -> Δf = 160 kHz FSParam_Dev = "11001000" -> Δf = 200 kHz
RTParam_Modul	5	00010	Inhibition of the modulation in transmitter mode: 0 -> modulation 1 -> no modulation
RTParam_IQAMP	4	00010	IQ amplifiers on/off: 0 -> off 1 -> on
RTParam_Switch_ext	3	00010	Mode of switch: 0 -> configuration defined by Chip_config and pad SWITCH is an output that indicates the RX or TX mode of the chip 1 -> configuration defined by the pad SWITCH used as an input
RTParam_Pattern	2	00010	Pattern recognition on/off: 0 -> off 1 -> on

5.2.3 FSParam configuration register

The detailed description of the “FSParam” register is given in the next table.

Name	Bits	Address	Description
FSParam_Band	1-0	00010	Frequency band: 00 -> 216 – 218 MHz 01 -> 433 – 435 MHz 10 -> 868 – 870 MHz 11 -> 902 – 928 MHz
FSParam_Dev	7-0	00011	Frequency deviation: Δf =int(FSParan_Dev) * 1 kHz, where int(x) = integer value of the binary representation of x. Example: 00000001 -> Δf = 1 kHz 11111111 -> Δf = 255 kHz
FSParam_Change_Osr	7	00100	Change OSR 0 -> default Bit rate defined by FSParam_Br 1 -> used with Konnex standard
FSParam_Br	6-0	00100	Bit rate: Br = 152.34e3/(int(FSParam_Br)+1), where int(x) = integer value of the binary representation of x. Example: 0000000 -> Br = 152.34 kbps 1111111 -> Br = 1.19 kbps 0000100 -> Br = 32.7 kbps used in Konnex mode
FSParam_OSR	7-0	00101	“00011101” with Konnex standard and FSParam_Change_Osr = ‘1’ else “00000000”

5.2.4 Switching parameters

The detailed description of the “SWParam” register is given in the next table.

Name	Bits	Address	Description
SWParam_mode_1	7-6	00110	Chip mode configuration 1: 00 -> Sleep mode 01 -> Stand by mode 10 -> Receiver mode 11 -> Transmitter mode
SWParam_Power_1	5-4	00110	Transmitter output power configuration 1: 00 -> 0 dBm 01 -> 5 dBm 10 -> 10 dBm 11 -> 15 dBm
SWParam_Rmode_1	3	00110	Receiver Mode configuration 1: 0 -> Mode A (high sensitivity) 1 -> Mode B (high linearity)
SWParam_t_delsig_in_1	2-0	00110	Extension of the input vector of the sigma-delta modulator configuration 1
SWParam_Freq_1	7-0 7-0	00111 01000	LO frequency in 2’s complement representation configuration 1: 00…0 -> Flo = middle of the range 0X…X-> Flo = higher than the middle of the range 1X…X-> Flo = lower than the middle of the range
SWParam_node_2	7-6	01001	Chip mode configuration 2: 00 -> Sleep mode, 01 -> Stand by mode, 10 -> RX mode, 11 -> TX mode,
SWParam_Power_2	5-4	01001	Transmitter output power configuration 2: 00 -> 0 dBm 01 -> 5 dBm 10 -> 10 dBm 11 -> 15 dBm
SWParam_Rmode_2	3	010001	Receiver Mode configuration 2: 0 -> Mode A (high sensitivity) 1 -> Mode B (high linearity)
SWParam_t_delsig_in_2	2-0	01001	Extension of the input vector of the sigma-delta modulator configuration 2
SWParam_Freq_2	7-0 7-0	01010 01011	LO frequency in 2’s complement representation configuration 2: 00…0 -> Flo = middle of the range 0X…X-> Flo = higher than the middle of the range 1X…X-> Flo = lower than the middle of the range

Here are examples of LO frequency settings in FSParam_Freq when mode 2 is used.

Byte Address 01010 Bit 7 Bit 0	Byte Address 01011 Bit 7 Bit 0	Resulting LO setting Note: reference frequency = 39.0 MHz
00000000	00000000	F0, where F0 depends on the selected frequency band (see FSParam_Band) F0 = 434.0 MHz for the 433-435 MHz band F0 = 869.0 MHz for the 868-870 MHz band F0 = 915.0 MHz for the 902-928 MHz band
00000000	00000001	F0 + 500 Hz
00000000	00000010	F0 + 2 * 500 Hz
11111111	11111111	F0 – 500 Hz
11111111	11111110	F0 – 2 * 500 Hz

5.2.5 DataOut register

The detailed description of the “DataOut” register is given in the next table.

Name	Bits	Address	Description
DataOut_Rssi	7-6	01100	RSSI output: 0 0 -> lowest level 0 1 -> 2nd level 1 0 -> 3rd level 1 1 -> highest level
Reserved	5-4	01100	Set to zero
DataOut_MSB_fei	3-0	01100	Fei output (MSB)
DataOut_LSB_fei	7-0	01101	Fei output (LSB) Ferror = (Br/8)*int(DataOut_MSB_fei & DataOut_LSB_fei) Where int(x) = integer value of the binary representation of x.

5.2.6 ADParam configuration register

The detailed description of the “ADParam” register is given in the next table.

Name	Bits	Address	Description
ADParam_Psize	7-6	01110	Size of the reference pattern: 0 0 -> 8 bits 0 1 -> 16 bits 1 0 -> 24 bits 1 1 -> 32 bits
ADParam_Ptol	5-4	01110	Number of tolerated errors for the pattern recognition: 00 -> 0 error 01 -> 1 error 10 -> 2 errors 11 -> 3 errors
ADParam_Clk_freq	3-2	01110	Frequency of clkout 00 -> 1.22 MHz (div ratio :32) 01 -> 2.44 MHz (div ratio :16) 10 -> 4.87 MHz (div ratio :8) 11 -> 9.75 MHz (div ratio :4)
ADParam_Invert	1	01110	Inversion of the output data of the receiver: 0 -> default data 1 -> inverted data
ADParam_RegBW	0	01110	Regulation of the bandwidth of the base-band filter on/off: 0 -> on 1 -> off
ADParam_Regfreq	7	01111	Periodicity of regulation of the bandwidth of the base-band filter: 0 -> only at start-up of the receiver 1 -> each minute (by default) or every 7 sec (test mode) as long as the receiver is on.
ADParam_Regcond	6	01111	Regulation process of the bandwidth of the base-band filter according to the selected bandwidth: 0 -> regulation restarted each time the bandwidth is changed 1 -> no regulation started when the bandwidth is changed
ADParam_Xsel	5	01111	Selection of the XOSC modes: 0 -> CL+C0 = 7 pF 1 -> CL+ C0 = 11 pF, lower consumption

Name	Bits	Address	Description
ADParam_Resxosc	4-1	01111	Selection of the value of the resistor put between TKA and TKB in order to use a crystal operating on its third overtone 0000 -> Resistance = 3800 KΩ 0001 -> Resistance = 2.55 KΩ 0010 -> Resistance = 4.65 KΩ 0011 -> Resistance = 1.78 KΩ 0100 -> Resistance = 8.79 KΩ 0101 -> Resistance = 2.07 KΩ 0110 -> Resistance = 3.22 KΩ 0111 -> Resistance = 1.56 KΩ 1000 -> Resistance = 16.55 KΩ 1001 -> Resistance = 2.26 KΩ 1010 -> Resistance = 3.79 KΩ 1011 -> Resistance = 1.66 KΩ 1100 -> Resistance = 6.04 KΩ 1101 -> Resistance = 1.91 KΩ 1110 -> Resistance = 2.81 KΩ 1111 -> Resistance = 1.48 KΩ
ADParam_enable_konnex	0	01111	Use of the Konnex standard when using the FEI 0 -> normal mode 1 -> Konnex standard => Br = 32.7 kbps This modifies OSR
ADParam_Chge_thres	7	10000	Make the sync and acquisition threshold programmable, and allow the change of the barker code: 0 -> threshold are hard-coded and sync loss counter is 50 bits 1 -> threshold are defined by BParam_Sync_thres and BParam_Trac_thres Sync loss counter is variable and defined by ADParam_Sync_loss
ADParam_Sync_thres	6:0	10000	Threshold for sync acquisition in baker mode
ADParam_disable_data_bidir	7	10001	Disable data bidir 0 -> Pad Data used in bidirectional mode. 1 ->Pad Data used as output and Pad datain used as input.
ADParam_Trac_thres	6-0	10001	Threshold for tracking baker mode
Reserved	7	10010	
ADParam_Sync_loss	6-0	10010	Number of bits before sync loss for barker decoding algorithm.

5.2.7 Pattern register

This register holds the user supplied reference pattern of 8, 16, 24, or 32 bits (see ADParam_Psize parameter). The first byte of this pattern is always stored in the byte at address A[4:0] = 10011. Depending on the pattern size the pattern values stored in addresses 10011, 10100, 10101 and 10110. The addresses 10011, 10100, 10101 and 10110 hold the first, second, third and fourth bytes of the reference pattern value respectively. The MSB bit of the reference pattern is always the bit 7 of the address 10011.
When compared to the demodulated bit stream, the last bit received is compared to the LSB bit in the Pattern register. The “oldest” bit received (the first of the last 8, 16, 24, or 32 received bits, depending on ADParam_Psize) is compared with the bit 7 of byte address 10011 (the MSB).

Name	Bits	Byte Address	Description
PATParam_Pattern	7-0	10011 10100 10101 10110	1st byte of the reference pattern 2nd byte 3rd byte 4th byte

Example of pattern recognition with a 32-bit pattern:

Byte Address 10011 Bit 7 Bit 0	Byte Address 10100 Bit 7 Bit 0	Byte Address 10101 Bit 7 Bit 0	Byte Address 10110 Bit 7 Bit 0
10010011	10101010	10010011	10101010
101 10010011	10101010	10010011	10101010
previous bits from demodulator			last bit received

Example of pattern recognition with an 8-bit pattern:

Byte Address 10011 Bit 7 Bit 0	Byte Address 10100 Bit 7 Bit 0	Byte Address 10101 Bit 7 Bit 0	Byte Address 10110 Bit 7 Bit 0
10010011	Xxxxxxxx	Xxxxxxxx	Xxxxxxxx
101 10010011			
previous bits from demodulator	last bit received		

5.3 OPERATING MODES

The XE1203 has 4 main operating modes illustrated in table below. These modes are defined in register SWParam_mode_1 when the configuration 1 is chosen or SWParam_mode_2 when the configuration 2 is chosen. The configuration is defined by the Chip_Config parameter (address 0) when RTParam_Switch_ext is low or by the pad SWITCH when RTParam_Switch_ext is high. Using Chip_config or SWITCH allows switching between any modes of the transceiver. To switch between modes, the new value of Chip_config or SWITCH should be modified when the EN signal is low. The changes will be applied to the transceiver upon the rising edge of the EN signal.

Mode	SWParam_mode1(1:0) or SWParam_mode_2(1:0)	Running blocks of the transceiver
Sleep mode	0 0	-
Standby mode	0 0	Quartz oscillator
Receiver mode	1 0	Quartz oscillator, Frequency synthesizer, Receiver
Transmitter mode	1 1	Quartz oscillator, Frequency synthesizer, Transmitter

5.3.1 Standard power up sequence for the receiver and transmitter

The chip is able to switch between every configuration by using the 3 wires interface (Chip_config) or by using the pad SWITCH. This section describes the switching sequence of the chip. The first diagram shows the sequence from sleep mode to receiver mode via stand by mode.

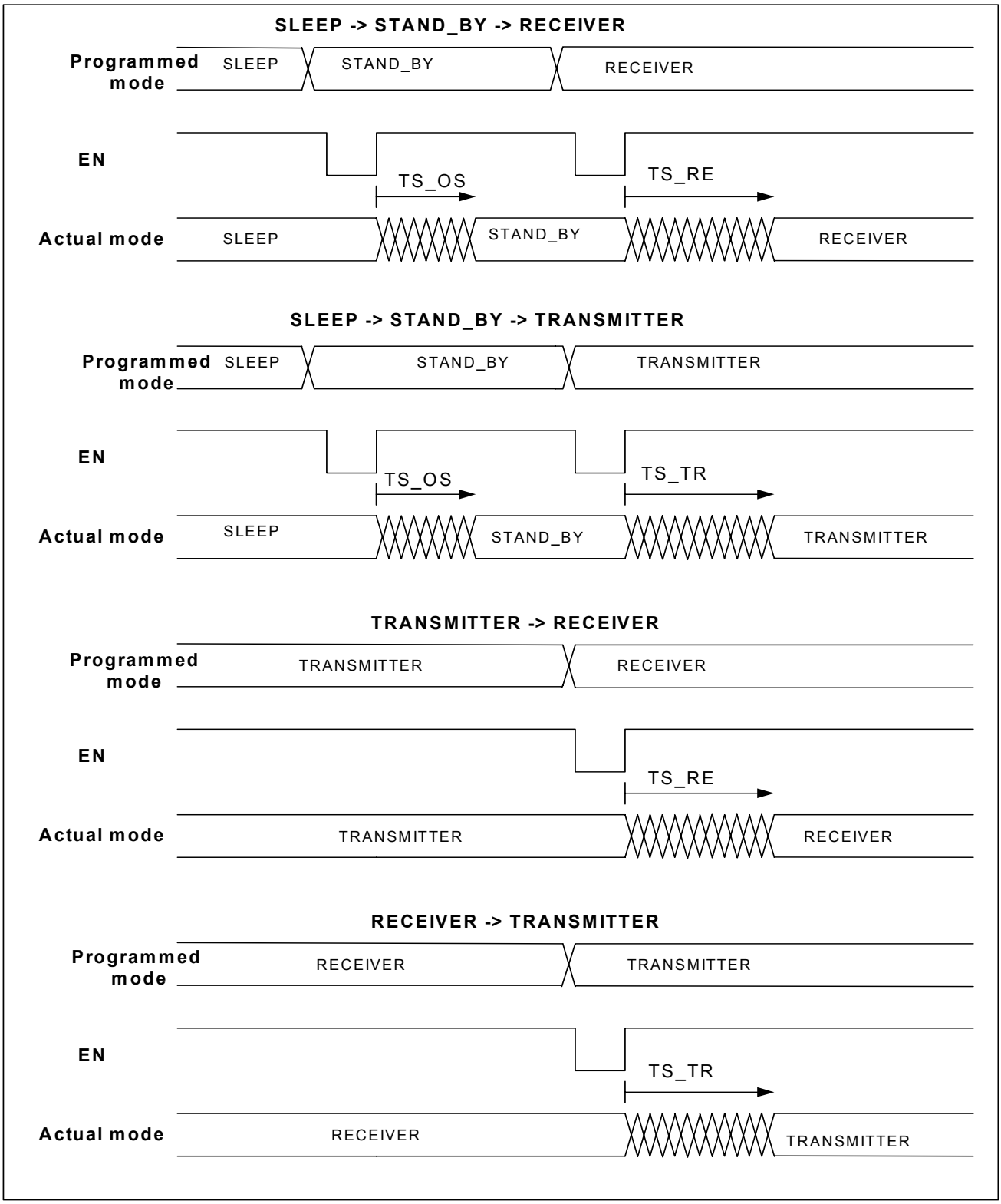


Figure 15.Switching between modes.

5.4 SELECTION OF THE REFERENCE FREQUENCY

The reference clock used for the frequency synthesizer and internal digital circuit can be generated internally using internal amplifier and external quartz crystal or provided by an external oscillator. In the case of external oscillator, the register “RTParam_Osc” has to be set high, and the external clock signal at 39 MHz has to be applied to the pin “XTA”.

The chip can be used with a 39 MHz quartz crystal running on its fundamental frequency or with 3rd overtone frequency. The third overtone operation requires a resistor in parallel to the quartz. This resistor can be selected by programming the register ADParam_Resxosc(3:0). The required value depends on the crystal used. ADParam_Resxosc(3:0) is set to ”0000’’ by default, which imposes a resistor of 3.8 MOhms in parallel to the crystal. This default value is used with a 39 MHz crystal running on its fundamental frequency. In the case of overtone operation of the quartz crystal, where the microcontroller uses the XE1203 as a clock source, user should be aware that during power up the XE1203 oscillator starts at fundamental frequency and after programming the oscillator switch to overtone operation. Therefore, a wait can be required for the oscillator to settle down before doing time sensitive operations.

5.5 CLOCK OUTPUT INTERFACE

When RTParam_Clkout is set high, a frequency divider by 4, 8, 16, 32, depending on ADParam_Clkfreq is embedded in the chip and provides the CLKOUT clock signal for an MCU or an external circuitry. The input frequency of this divider is the 39.0 MHz reference frequency, so the possible output frequencies are listed in the next table.

ADParam_Clkfreq	CLKOUT frequency
00	1.22 MHz
01	2.44 MHz
10	4.87 MHz
11	9.75 MHz

When the XE1203 is in sleep mode, then this clock is stopped even if RTParam_Clkout remains high.

5.6 DEFAULT SETTINGS AT POWER-UP

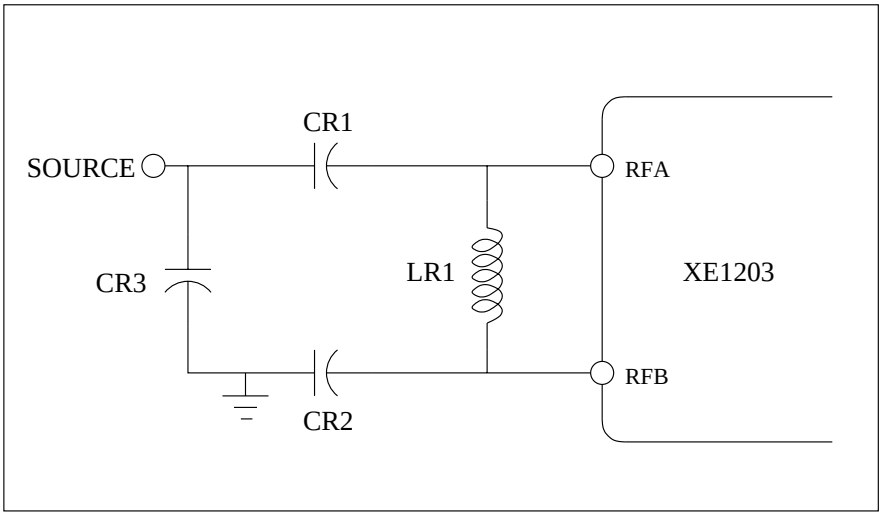
The internally generated power on reset signal sets the RTParam, FSParam, ADParam and Pattern registers to 00hex. Only exception is CLKOUT generation, although RTPAram_CLkout is set to low, i.e disabled, the XE1203 generates a CLKOUT signal in order to let the microcontroller operate.

The first rising edge on EN pin causes the registers to be updated and this will result CLKOUT to be disabled. For this reason the first programming sequence should be enabling CLKOUT by setting RTPAram_CLkout register to high for applications using CLKOUT. Initializing the XE1203 registers immediately after power-up according to the application needs is strongly recommended.

6 APPLICATION INFORMATION

6.1 MATCHING NETWORK OF THE RECEIVER

The schematic of the matching network at the input of the receiver is given below

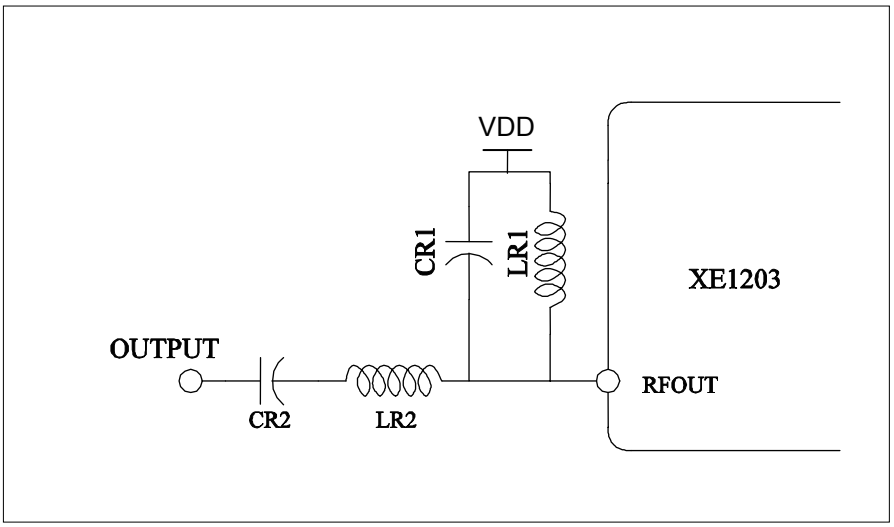


The typical component values of the matching circuit are given below.

Name	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CR1	3.3 pF	1.2 pF	± 5 %
CR2	1.5 pF	1.2 pF	± 5 %
CR3	6.8 pF	NC	± 5 %
LR1	22 nH	27 nH	± 5 %

6.2 MATCHING NETWORK OF THE TRANSMITTER

The schematic of the matching network at the output of the transmitter is given below.



The typical component values of the matching circuit are given below.

Name	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CR1	3.3 pF	2.2 pF	± 5 %
CR2	3.3 pF	3.3 pF	± 5 %
LR1	27 nH	27 nH	± 5 %
LR2	12 nH	10 nH	± 5 %

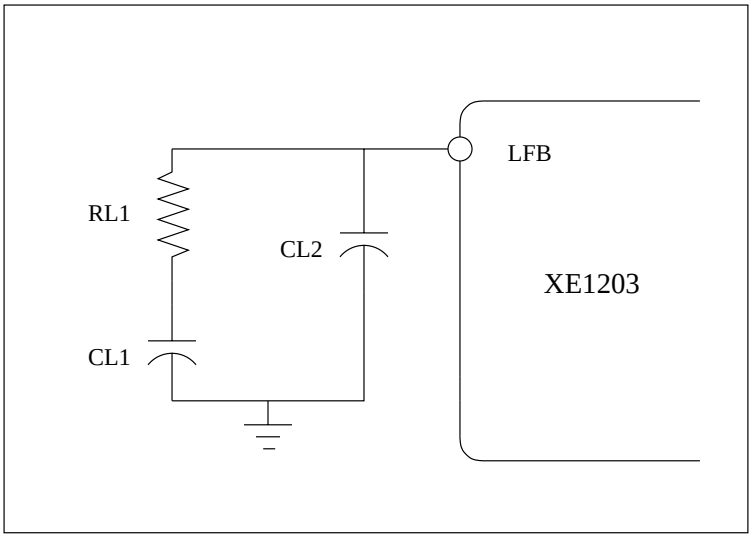
6.3 VCO TANK

The tank of the VCO will be implemented with one inductor in parallel with one capacitor. The characteristics of these two components must be as follows:

Name	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CV1	0.5 pF	NC	± 5 %
LV1	12 nH	12 nH	± 2 %

6.4 LOOP FILTER OF THE FREQUENCY SYNTHESIZER

The loop filter of the frequency synthesizer is shown below.



The typical component values of the filter are given below.

Name	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CL1	22 nF	22 nF	± 5 %
CL2	220 pF	220 pF	± 5 %
RL1	2.7 k	2.2 k	± 5 %

6.5 REFERENCE CRYSTAL FOR THE FREQUENCY SYNTHESIZER

For narrow band applications, where users select the lowest frequency deviation and the narrowest baseband filter, the crystal for reference oscillator of the frequency synthesizer must have the following characteristics:

Name	Description	Min. value	Typ. value	Max. value
Fs	Nominal frequency	-	39.0 MHz (fundamental)	-
CL	Load capacitance for fs (on-chip)	-	8 pF (*)	-
Rm	Motional resistance	-	-	40 Ω
Cm	Motional capacitance	-	-	30 fF
C0	Shunt capacitance	-	-	7 pF (*)
Δfs(Δ0)	Calibration tolerance at 25 °C	-	-	10 ppm
Δfs(ΔT)	Stability over temperature range (-40 °C to 85 °C)	-	-	10 ppm
Δfs(Δt)	Aging tolerance in first 5 years	-	-	5 ppm

Table 5 Crystal characteristics

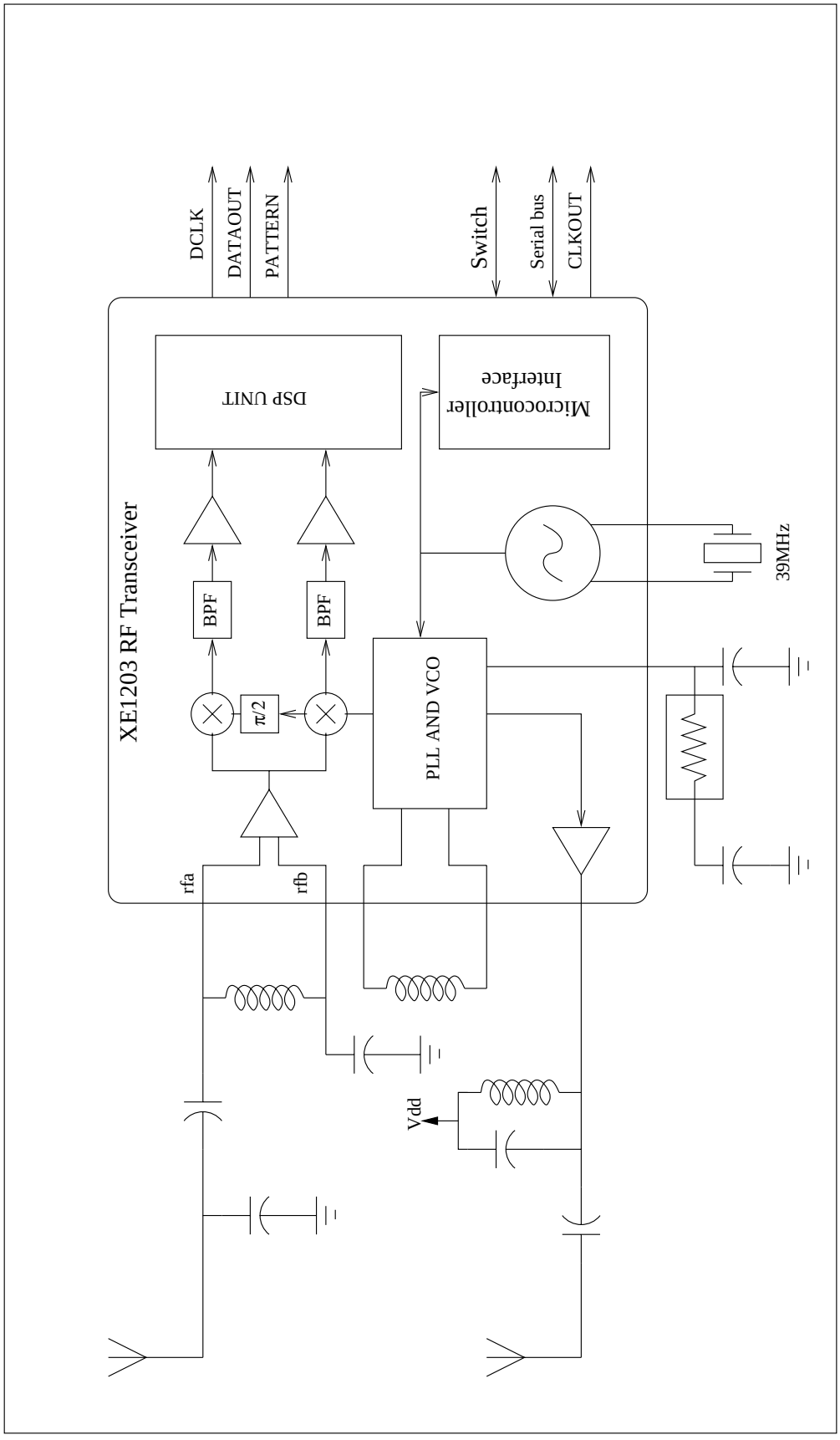
(*) The on-chip oscillator mode is user-defined by programming ADParam_Xsel: the first for CL = 8 pF and C0 = 7 pF, and the second for CL = 8 pF and C0 = 3 pF; the latter will allow higher amplitude for the internal signal with a slightly lower consumption.

The electrical specifications given in section 3.2.2 are valid for a crystal having the specifications given in table 5. For applications requiring less frequency stability in terms of signal bandwidth and/or temperature range, it is possible to use a crystal with larger values for Δfs(Δ0), Δfs(ΔT), and/or Δfs(Δt). In this case foffset + BWssb should be lower than BWfilter, where foffset is the offset (error) on the carrier frequency (the sum of Δfs(Δ0), Δfs(ΔT), and/or Δfs(Δt)), BWssb is the single side-band bandwidth of the signal, and BWfilter is the single side-band bandwidth of the base-band filter.

The overtone crystal usage can result higher oscillator start-up time than fundamental mode. The overtone crystal should be designed for Cload = 8 to 10pF and has parameters of Rm < 60 ohm, C0 < 7pF.

6.6 TYPICAL APPLICATION

The simplified circuit diagram for a typical application is shown below.



7 PACKAGING INFORMATION

XE1203 comes in a 48-lead VQFN package