| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Changes in table I: Page 4, input offset voltage should read $+V_{CC}$ = 3.5 V, $-V_{CC}$ = -32.5 V. Page 5, gain error, reference subgroups 4, 5, 6, as separate tests. Temperature limits $+V_{CC}$ = 32.5 V should be .06 instead of .02. Page 6, changes acquisition parameters. Page 10, add replacement military specification part number. Inactivate drawing for new design. Editorial changes throughout. | 88-05-11 | M. A. FRYE |
| B | Changes in accordance with N.O.R. 5962-R313-92. | 92-10-08 | M. A. FRYE |
| C | Add generic part number 5537 as device type 02. Add vendor CAGE 18324. Add case outline letter P. Make changes to 1.2.1, 1.2.2, 1.3, TABLE I, and FIGURE 1. Redrawn. | 94-04-19 | M. A. FRYE |
| D | Add device class level Q and V devices. Add case outline letter Z. Make changes to 1.2.2, 1.3, figure 1, table II, and the gain error test as specified in table I. - ro | 01-05-25 | R. MONNIN |

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | D | D | | | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | | | | | | | | | | | | | | | | | | |

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV STATUS | REV | D | D | D | D | D | D | D | D | D | D | D | D | D | D |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

PMIC N/A

PREPARED BY
MARCIA B. KELLEHER

CHECKED BY
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APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
87-06-17

REVISION LEVEL
D

**DEFENSE SUPPLY CENTER COLUMBUS**
**COLUMBUS, OHIO 43216**
**http://www.dscc.dla.mil**

# STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, LINEAR, SAMPLE AND HOLD, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **67268** | **5962-87608** |

SHEET 1 OF 16

DSCC FORM 2233
APR 97

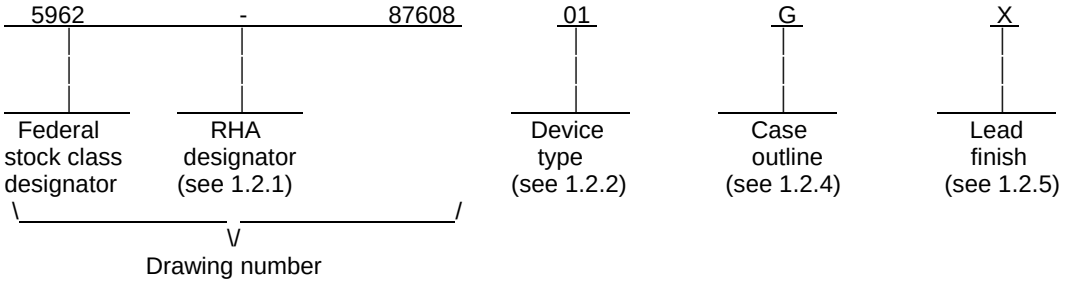
5962-E445-01

1. SCOPE

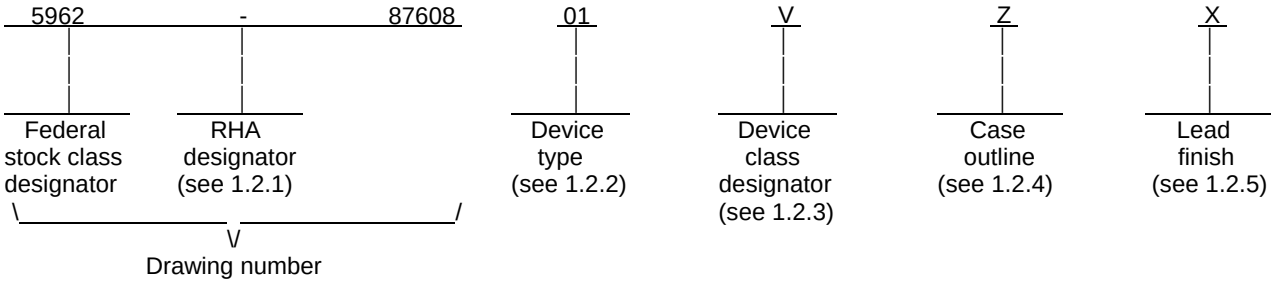
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:




For device class V:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | LF198 | Sample and hold |
| 02 | 5537 | Sample and hold |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing for devices 01GA and 02PA, the device classes M and Q designators will not be included in the PIN and will not be marked on the device.

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| G | MACY1-X8 | 8 | Can |
| P | GDIP1-T8 or CDIP2-T8 | 8 | Dual-in-line |
| Z | GDFP1-G14 | 14 | Flat pack with gullwing leads |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage ($\pm V_{CC}$) ..... ±18 V
Power dissipation ($P_D$) ..... 500 mW 2/
Input voltage ($V_{IN}$) ..... ±18 V 3/
Logic to logic differential voltage ..... +7 V, -30 V 4/
Output short circuit duration ..... Indefinite
Hold capacitor short circuit duration ..... 10 seconds
Lead temperature (soldering, 10 seconds) ..... 300°C
Storage temperature range ..... -65°C to +150°C
Junction temperature ($T_J$) ..... +150°C
Thermal resistance, junction-to-case ($\theta_{JC}$):
Case G ..... 48°C/W
Case P ..... See MIL-STD-1835
Case Z ..... 20°C/W
Thermal resistance, junction-to-ambient ($\theta_{JA}$):
Case G ..... 160°C/W, still air at 0.5 W
84°C/W, 500 LFPM air flow 0.5 W
Case P ..... 120°C/W
Case Z ..... 140°C/W, still air at 0.5 W
95°C/W, 500 LFPM air flow 0.5 W

1.4 Recommended operating conditions.

Supply voltage ($\pm V_{CC}$) ..... ±15 V
Ambient operating temperature range ($T_A$) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ The maximum power dissipation must be derated at elevated temperatures and is dicated by $T_{JMAX}$, $\theta_{JA}$ and $T_A$.
The maximum allowable power dissipation at any temperature is $P_{DMAX} - (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in the absolute maximum ratings, whichever is lower.
3/ The maximum input voltage shall not exceed the power supply voltage.
4/ Although the differential voltage may not exceed the limits given, the common-mode voltage the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at 2 V below the positive supply and 3 V above the negative supply.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 2.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 60 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits 2/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Input offset voltage | $V_{OS}$ | $+V_{CC}$ = 3 V, $-V_{CC}$ = -7 V | 1 | 01 | -3 | 3 | mV |
| | | | 2,3 | | -5 | 5 | |
| | | $\pm V_{CC}$ = 15 V | 1 | | -3 | 3 | |
| | | | 2,3 | | -5 | 5 | |
| | | $+V_{CC}$ = 3.5 V, $-V_{CC}$ = -26.5 V | 1 | | -3 | 3 | |
| | | | 2,3 | | -5 | 5 | |
| | | $\pm V_{CC}$ = ±18 V | 1 | | -3 | 3 | |
| | | | 2,3 | | -5 | 5 | |
| | | $+V_{CC}$ = 3.5 V, $-V_{CC}$ = -32.5 V | 1 | | -3 | 3 | |
| | | | 2,3 | | -5 | 5 | |
| | | $+V_{CC}$ = 26.5 V, $-V_{CC}$ = -3.5 V | 1 | | -3 | 3 | |
| | | | 2,3 | | -5 | 5 | |
| | | $+V_{CC}$ = 32.5 V, $-V_{CC}$ = -3.5 V | 1 | | -3 | 3 | |
| | | | 2,3 | | -5 | 5 | |
| | | $+V_{CC}$ = 7 V, $-V_{CC}$ = -3 V | 1 | | -3 | 3 | |
| | | | 2,3 | | -5 | 5 | |
| | | $\pm V_{CC}$ = ±5 V to ±18 V | 1 | 02 | -3 | 3 | |
| | | | 2,3 | | -5 | 5 | |
| Positive supply current | $+I_{CC}$ | $V_{CC}$ = ±15 V | 1,2 | 01 | | 5.5 | mA |
| | | | 3 | | | 6.5 | |
| | | $V_{CC}$ = ±18 V | 1,2 | 02 | | 6.5 | |
| | | | 3 | | | 7.5 | |
| | | $V_{CC}$ = ±18 V, mode = sample | 1,2 | 01 | | 5.5 | |
| | | | 3 | | | 6.5 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits 2/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Positive supply current | $+I_{CC}$ | $V_{CC} = \pm 18$ V, mode = hold | 1,2 | 01 | | 5.5 | mA |
| | | | 3 | | | 6.5 | |
| Negative supply current | $-I_{CC}$ | $V_{CC} = \pm 15$ V | 1,2 | 01 | -5.5 | | mA |
| | | | 3 | | -6.5 | | |
| | | $V_{CC} = \pm 18$ V | 1,2 | 02 | -6.5 | | |
| | | | 3 | | -7.5 | | |
| | | $V_{CC} = \pm 18$ V, mode = sample | 1,2 | 01 | -5.5 | | |
| | | | 3 | | -6.5 | | |
| | | $V_{CC} = \pm 18$ V, mode = hold | 1,2 | | -5.5 | | |
| | | | 3 | | -6.5 | | |
| Input bias current | $I_{IB}$ | $+V_{CC} = 3$ V, $-V_{CC} = -7$ V | 1 | 01 | -25 | 25 | nA |
| | | | 2,3 | | -75 | 75 | |
| | | $\pm V_{CC} = 15$ V | 1 | | -25 | 25 | |
| | | | 2,3 | | -75 | 75 | |
| | | $+V_{CC} = 3.5$ V, $-V_{CC} = -32.5$ V | 1 | | -25 | 25 | |
| | | | 2,3 | | -75 | 75 | |
| | | $+V_{CC} = +32.5$ V, $-V_{CC} = -3.5$ V | 1 | | -25 | 25 | |
| | | | 2,3 | | -75 | 75 | |
| | | $+V_{CC} = 7$ V, $-V_{CC} = -3$ V | 1 | | -25 | 25 | |
| | | | 2,3 | | -75 | 75 | |
| | | $\pm V_{CC} = \pm 5$ V to $\pm 18$ V | 1 | 02 | -25 | 25 | |
| | | | 2,3 | | -75 | 75 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits 2/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Leakage current into hold capacitor 3/ | $I_{LEAK}$ | $+V_{CC}$ = 3 V, $-V_{CC}$ = -7 V, $T_A$ = +25°C | 1 | 01 | -100 | 100 | pA |
| | | $+V_{CC}$ = 3.5 V, $-V_{CC}$ = -32.5 V, $T_A$ = +25°C | | | -100 | 100 | |
| | | $+V_{CC}$ = 32.5 V, $-V_{CC}$ = -3.5 V, $T_A$ = +25°C | | | -100 | 100 | |
| | | $+V_{CC}$ = 7 V, $-V_{CC}$ = -3 V, $T_A$ = +25°C | | | -100 | 100 | |
| | | Hold mode | 1 | 02 | | .05 | nA |
| | | | 2,3 | | | 25 | |
| Hold step 4/ | $V_{HS}$ | $\pm V_{CC}$ = 15 V | 1 | 01 | -2 | 2 | mV |
| | | | 2,3 | | -5.6 | 5.6 | |
| | | $+V_{CC}$ = 3.5 V, $-V_{CC}$ = -26.5 V | 1 | | -2.5 | 2.5 | |
| | | | 2,3 | | -5.6 | 5.6 | |
| | | $+V_{CC}$ = 26.5 V, $-V_{CC}$ = -3.5 V | 1 | | -2.5 | 2.5 | |
| | | | 2,3 | | -5.6 | 5.6 | |
| | | $V_{OUT}$ = 0 V, $T_A$ = +25°C, $C_H$ = 0.01 µF | 1 | 02 | | 2.0 | |
| Input impedance | $Z_{IN}$ | $+V_{CC}$ = 8 V, $-V_{CC}$ = -28 V | 1 | 01 | 10 | | GΩ |
| | | | 2,3 | | 0.8 | | |
| | | $+V_{CC}$ = 28 V, $-V_{CC}$ = -8 V | 1 | | 10 | | |
| | | | 2,3 | | 0.8 | | |
| Output impedance | $Z_{OUT}$ | $\pm V_{CC}$ = ±18 V | 1 | 01 | | 2 | GΩ |
| | | | 2,3 | | | 4 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/<br>$-55°C \le T_A \le +125°C$<br>unless otherwise specified | Group A subgroups | Device type | Limits 2/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Output impedance | $Z_{OUT}$ | Hold mode | 1 | 02 | | 2 | Ω |
| | | | 2,3 | | | 4 | |
| Capacitor charging current | $I_{CHRG}$ | $+V_{CC}$ = 8 V, | 1 | 01 | -25 | -4.5 | mA |
| | | $-V_{CC}$ = -28 V | 2,3 | | -25 | -3 | |
| | | $+V_{CC}$ = 28 V, | 1 | | 4.5 | 25 | |
| | | $-V_{CC}$ = -8 V | 2,3 | | 3 | 25 | |
| Logic pin current | LOGIC | $\pm V_{CC} = \pm 18$ V,<br>mode = sample | 1,2,3 | 01 | 10 | | µA |
| | | $\pm V_{CC} = \pm 18$ V, | 1 | | | 1 | |
| | | mode = hold | 2,3 | | | 0.5 | |
| Input offset voltage | $V_{OS}$ / $\Delta V_{OS}$ | $\pm V_{CC} = \pm 15$ V, | 1 | 01 | -3.5 | 3.5 | mV |
| | | 1Drive = +1 mA | 2,3 | | -6 | 6 | |
| | | $\pm V_{CC} = \pm 15$ V, | 1 | | -1.1 | 1.1 | |
| | | 1Drive = +1 mA to –1 mA | 2,3 | | -2 | 2 | |
| Output short circuit current | $+I_{OS}$ | $\pm V_{CC} = \pm 18$ V,<br>$T_A$ = +25°C | 1 | 01 | 7 | 20 | mA |
| | $-I_{OS}$ | $\pm V_{CC} = \pm 18$ V,<br>$T_A$ = +25°C | | | -25 | 7 | |
| Logic reference pin current | $I_{LOG}$ | $\pm V_{CC} = \pm 18$ V, | 1 | 01 | -1 | 1 | µA |
| | | mode = sample | 2,3 | | -0.5 | 5 | |
| | | $\pm V_{CC} = \pm 18$ V,<br>mode = hold | 1,2,3 | | | 10 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified | Group A subgroups | Device type | Limits 2/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Logic and logic reference input current | $I_{LOG}$ | $V_{IN}$ = 2.4 V | 1 | 02 | | 10 | µA |
| | | | 2,3 | | | 20 | |
| | | $V_{IN}$ = 0 V | 1 | | -10 | | |
| | | | 2,3 | | -20 | | |
| Power supply rejection ratio | PSRR | $+V_{CC}$ = 10 V, $-V_{CC}$ = -15 V | 1 | 01 | 80 | | dB |
| | | | 2,3 | | 74 | | |
| | | $+V_{CC}$ = 15 V, $-V_{CC}$ = -10 V | 1 | | 80 | | |
| | | | 2,3 | | 74 | | |
| | | $+V_{CC}$ = 15 V, $V_{OUT}$ = 0 V, $-V_{CC}$ = -10 V | 1,2,3 | 02 | 80 | | |
| Feed through rejection ratio | FTRR | $+V_{CC}$ = 3.5 V, $-V_{CC}$ = -32.5 V | 1 | 01 | 86 | | dB |
| | | | 2,3 | | 74 | | |
| | | $+V_{CC}$ = 32.5 V, $-V_{CC}$ = -3.5 V | 1 | | 86 | | |
| | | | 2,3 | | 74 | | |
| Feed through attenuation ratio | FTAR | $C_H$ = 0.01 µF, $T_A$ = +25°C | 1 | 02 | 86 | | dB |
| Differential logic level 5/ | $V_{TH}$ | $T_A$ = +25°C | 1 | All | 0.8 | 2.4 | V |
| Second stage $V_{OS}$ | $V_{OS}$ (2 nd stage) | $+V_{CC}$ = 3.5 V, $-V_{CC}$ = -32.5 V | 1 | 01 | -35 | 35 | mV |
| | | | 2,3 | | -50 | 50 | |
| | | $+V_{CC}$ = 3.0 V, $-V_{CC}$ = -7 V | 1 | | -35 | 35 | |
| | | | 2,3 | | -50 | 50 | |
| | | $+V_{CC}$ = 32.5 V, $-V_{CC}$ = -3.5 V | 1 | | -35 | 35 | |
| | | | 2,3 | | -50 | 50 | |
| | | $+V_{CC}$ = 7 V, $-V_{CC}$ = -3 V | 1 | | -35 | 35 | |
| | | | 2,3 | | -50 | 50 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test | Symbol | Conditions 1/<br>$-55°C \le T_A \le +125°C$<br>unless otherwise specified | Group A subgroups | Device type | Limits 2/ | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Acquisition time 6/ | $t_{AQ}$ | $\Delta V_{OUT}$ = 10 V,<br>$T_A$ = +25°C,<br>$C_{HOLD}$ = 1000 pF | 4 | 01 | | 6 | µs |
| | | $\Delta V_{OUT}$ = 10 V,<br>$T_A$ = +25°C,<br>$C_{HOLD}$ = 0.01 µF | | | | 25 | |
| Gain error | $A_E$ | $+V_{CC}$ = 7 V,<br>$-V_{CC}$ = -3 V | 1<br>2,3 | 01 | | .02<br>.06 | % |
| | | $+V_{CC}$ = 3.5 V,<br>$-V_{CC}$ = -26.5 V | 1<br>2,3 | | | .005<br>.02 | |
| | | $+V_{CC}$ = 32.5 V,<br>$-V_{CC}$ = -3.5 V | 1<br>2,3 | | | .005<br>.06 | |
| | | $+V_{CC}$ = 26.5 V,<br>$-V_{CC}$ = -3.5 V | 1<br>2,3 | | | .005<br>.02 | |
| | | $V_{IN}$ = -10 V to 10 V,<br>$R_L$ = 2 kΩ | 1<br>2,3 | 02 | | .007<br>.01 | |
| | | $V_{IN}$ = -11.5 V to 11.5 V,<br>$R_L$ = 10 kΩ | 1<br>2,3 | | | .007<br>.01 | |

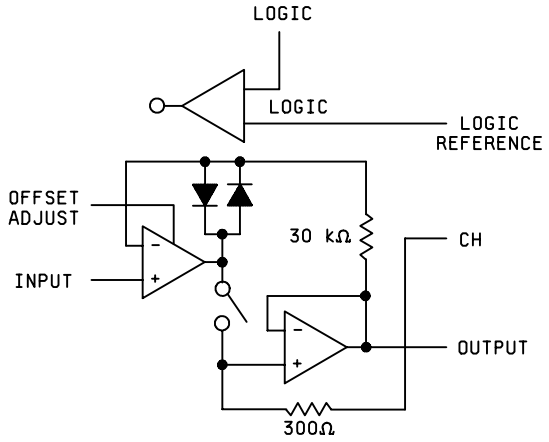
1/ Unless otherwise specified, $V_{CC} = \pm 15$ V, $C_{HOLD}$ = 0.01 µF, and logic reference pin = 0 V. For device type 01, $R_L$ = 10 kΩ and $V_{IN}$ = 0 V. For device type 02, $R_L$ = 2 kΩ, $V_{IN}$ = -11.5 V to +11.5 V and logic voltage = 2.5 V.
2/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
3/ Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation of elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4/ Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. One pF, for instance, will create an additional 0.5 mV step with 5 V logic swing and a 0.01 µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
5/ Parameter tested go-no-go only.
6/ If not tested, shall be guaranteed to the limits specified in table I herein.

| Device types | 01 | | 02 |
|---|---|---|---|
| Case outlines | G | Z | P |
| Terminal number | Terminal symbol | | |
| 1 | $+V_{CC}$ | INPUT | $+V_{CC}$ |
| 2 | OFFSET ADJUST | NC | OFFSET ADJUST |
| 3 | +INPUT | $-V_{CC}$ | +INPUT |
| 4 | $-V_{CC}$ | NC | $-V_{CC}$ |
| 5 | OUTPUT | NC | OUTPUT |
| 6 | $C_H$ | NC | $C_H$ |
| 7 | LOGIC REFERENCE | OUTPUT | LOGIC REFERENCE |
| 8 | LOGIC | $C_H$ | LOGIC |
| 9 | --- | NC | --- |
| 10 | --- | LOGIC REFERENCE | --- |
| 11 | --- | LOGIC | --- |
| 12 | --- | $+V_{CC}$ | --- |
| 13 | --- | NC | --- |
| 14 | --- | OFFSET ADJUST | --- |

NC = No connection

FIGURE 1. Terminal connections.

DEVICE TYPE 01




DEVICE TYPE 02

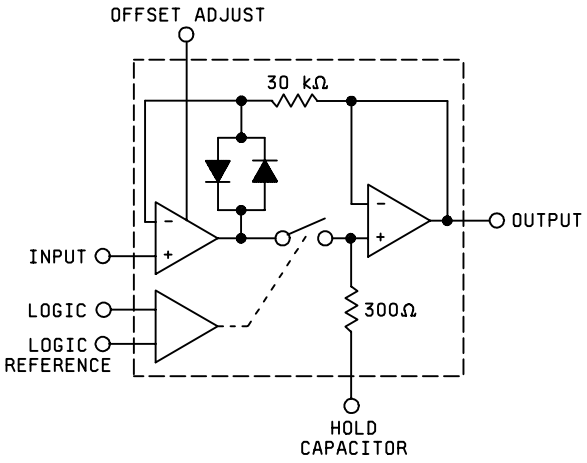



FIGURE 2. Logic diagram.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE IIA. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | 1 | 1 | 1 |
| Final electrical parameters (see 4.2) | 1,2,3,4 1/ | 1,2,3,4 1/ | 1,2,3,4 1/ |
| Group A test requirements (see 4.4) | 1,2,3,4 | 1,2,3,4 | 1,2,3,4 |
| Group C end-point electrical parameters (see 4.4) | 1 | 1 | 1,2,3 2/ |
| Group D end-point electrical parameters (see 4.4) | 1 | 1 | 1,2,3 |
| Group E end-point electrical parameters (see 4.4) | 1 | 1 | 1 |

1/ PDA applies to subgroup 1.
2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the previous endpoint electrical parameters.

Table IIB. Group C end-point electrical parameters. $T_A$ = 25°C

| Parameter | Device type 01 | Delta limit | |
|---|---|---|---|
| | Conditions | Min | Max |
| $V_{IO}$ | $+V_{CC}$ = 15 V, $-V_{CC}$ = -15 V | -0.5 mV | 0.5 mV |
| $I_{IB}$ | $+V_{CC}$ = 15 V, $-V_{CC}$ = -15 V | -2.5 nA | 2.5 nA |

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-05-24

Approved sources of supply for SMD 5962-87608 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ | Reference military specification PIN |
|---|---|---|---|
| 5962-8760801GA | 27014 | LF198H/883 | M38510/12501BGA |
| 5962-8760802PA | 3/ | 5537/BPA | M38510/12502BPA |
| 5962-8760801QZA | 27014 | LF198WG/883 | --- |
| 5962-8760801VZA | 27104 | LF198WG-QMLV | --- |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 27014 | National Semiconductor Corporation<br>2900 Semiconductor Drive<br>P.O. Box 58090<br>Santa Clara, CA 95052-8090 |