

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 02 and 03. Add vendor CAGE 61772 for device types 02 and 03. Delete vendor CAGE 61772 for device type 01. Add vendor CAGE 75569 for device types 02 and 03. Technical and editorial changes throughout.	92-03-06	<i>M.A. Rye</i>

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	A																			
SHEET	15																			

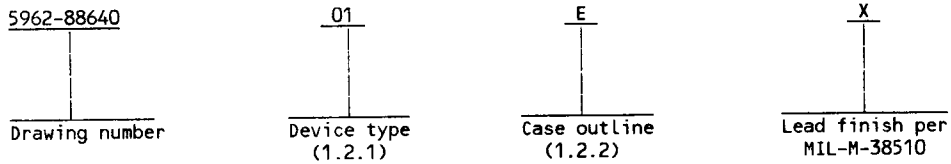
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A	PREPARED BY Jeffery Tunstall	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444					
<p align="center">STANDARDIZED MILITARY DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p>AMSC N/A</p>	CHECKED BY Ray Monnin			MICROCIRCUITS, DIGITAL, FAST CMOS SYNCHRONOUS PRESETTABLE BINARY, COUNTER, TTL COMPATIBLE, MONOLITHIC SILICON			
	APPROVED BY D. R. Cool	<table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-88640</td> </tr> </table>				SIZE A	CAGE CODE 67268
	SIZE A	CAGE CODE 67268	5962-88640				
	DRAWING APPROVAL DATE 88-09-30	<table border="1"> <tr> <td>SHEET</td> <td>1</td> <td>OF</td> <td>15</td> <td align="right">1</td> </tr> </table>		SHEET	1	OF	15
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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01 ^{1/}	54FCT161	Presetable binary counter, synchronous, TTL compatible
02	54FCT161	Presetable binary counter, synchronous, TTL compatible
03	54FCT161A	Presetable binary counter, synchronous, TTL compatible

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

<u>Outline letter</u>	<u>Case outline</u>
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
F	F-5 (16-lead, .440" x .285" x .085"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings. ^{2/}

Supply voltage (V_{CC})	- - - - -	-0.5 V dc to +7.0 V dc
Input voltage range	- - - - -	-0.5 V dc to V_{CC} + 0.5 V dc ^{3/}
Output voltage range	- - - - -	-0.5 V dc to V_{CC} + 0.5 V dc ^{3/}
DC input diode current (I_{IK})	- - - - -	-20 mA
DC output diode current (I_{OK})	- - - - -	-50 mA
DC output current	- - - - -	±100 mA
Power dissipation (P_D) ^{4/}	- - - - -	500 mW
Thermal resistance (θ_{JC})	- - - - -	See MIL-M-38510, appendix C
Storage temperature	- - - - -	-65°C to +150°C
Junction temperature (T_J)	- - - - -	+175°C
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C

^{1/} Due to internal noise problems, device type 01 does not meet the minimum V_{IH} threshold limit characteristic of the FCT family or the limits specified on this drawing. This device type is no longer available for acquisition.

^{2/} All voltage referenced to GND.

^{3/} For $V_{CC} > 6.5$ V dc, the upper bound is limited to V_{CC} .

^{4/} Must withstand the added P_D due to short circuit test e.g., I_{OS} .

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1.4 Recommended operating conditions.

Supply voltage (V_{CC})	-----	+4.5 V dc to +5.5 V dc
Maximum logic low voltage (V_{LL})	-----	0.8 V dc
Minimum logic high voltage (V_{IH})	5/ -----	2.0 V dc
Case operating temperature (T_C)	-----	-55°C to +125°C
Minimum setup time, high or low (P_n to CP) (t_{s1}):		
Device types 01 and 02	-----	5.5 ns
Device type 03	-----	4.5 ns
Minimum setup time, high or low (PE to CP) (t_{s2}):		
Device types 01 and 02	-----	13.5 ns
Device type 03	-----	11.5 ns
Minimum setup time, high or low (CEP, CET to CP) (t_{s3}):		
Device types 01 and 02	-----	13.0 ns
Device type 03	-----	11.0 ns
Minimum hold time, high or low (P_n to CP) (t_{h1})	-----	2.0 ns
Minimum hold time, high or low (PE to CP) (t_{h2})	-----	1.5 ns
Minimum hold time, high or low (CEP, CET to CP) (t_{h3})	-----	0.0 ns
Minimum CP pulse width, high, low (load) (t_{w1}):		
Device types 01 and 02	-----	5.0 ns
Device type 03	-----	4.0 ns
Minimum CP pulse width, high, low (count) (t_{w2}):		
Device types 01 and 02	-----	8.0 ns
Device type 03	-----	7.0 ns
Minimum MR pulse width, low (t_{w3}):		
Device types 01 and 02	-----	5.0 ns
Device type 03	-----	4.0 ns
Minimum recovery time MR to CP (t_{REC}):		
Device types 01 and 02	-----	6.0 ns
Device type 03	-----	5.0 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

5/ For dynamic operation of device type 01, a V_{IH} level between 2.0 V and 3.0 V may be recognized by this device as a high logic level input. For static operation of device type 01, a $V_{IH} \geq 2.0$ V will be recognized by these devices as a high logic level input. Users are cautioned to verify that this change will not affect their system.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connection(s). The terminal connection(s) shall be as specified on figure 1 herein.

3.2.2 Truth table. The truth table shall be as specified on figure 2 herein.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3 herein.

3.2.4 Counting sequence. The counting sequence shall be as specified on figure 4.

3.2.5 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5.0 V dc ±10%	Device type	Group A subgroups	Limits		Unit	
					Min	Max		
High level output voltage	V _{OH} 1/	V _{CC} = 4.5 V V _{IL} = 0.8 V V _{IH} = 2.0 V	I _{OH} = -300 μA	ALL	1, 2, 3	4.3	V	
			I _{OH} = -12 mA	ALL	1, 2, 3	2.4		
Low level output voltage	V _{OL} 1/	V _{CC} = 4.5 V V _{IL} = 0.8 V V _{IH} = 2.0 V	I _{OL} = 300 μA 2/	ALL	1, 2, 3		0.2	V
			I _{OH} = 32 mA	ALL	1, 2, 3		0.5	
Input clamp voltage	V _{IK}	V _{CC} = 4.5 V, I _N = -18 mA	ALL	1, 2, 3		-1.2	V	
High level input current	I _{IH}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	ALL	1, 2, 3		5.0	μA	
Low level input current	I _{IL}	V _{CC} = 5.5 V, V _{IN} = GND	ALL	1, 2, 3		-5.0		
Short circuit output current	I _{OS}	V _{CC} = 5.5 V 3/ V _{OUT} = GND	ALL	1, 2, 3	-60		mA	
Quiescent power supply current (CMOS inputs)	I _{CCQ}	V _{CC} = 5.5 V, V _{IN} ≤ 0.2 V or V _{IN} ≥ 5.3 V, f _I = 0 MHz	ALL	1, 2, 3		1.5	mA	
Quiescent power supply current (TTL inputs)	ΔI _{CC}	V _{CC} = 5.5 V, V _{IN} = 3.4 V 4/	ALL	1, 2, 3		2.0		
Dynamic power supply current	I _{CCD}	V _{CC} = 5.5 V, V _{IN} ≥ 5.3 V or V _{IN} ≤ 0.2 V, MR = V _{CC} , outputs open, one bit toggling, 50 percent duty cycle 5/	ALL			0.25	mA/MHz	
Total power supply current 6/	I _{CC}	V _{CC} = 5.5 V, f _{CP} = 10 MHz, outputs open, V _{IN} ≥ 5.3 V or V _{IN} ≤ 0.2 V, one bit toggling at f _I = 5 MHz, 50 percent duty cycle	ALL	1, 2, 3		4.0	mA	
		V _{CC} = 5.5 V, f _{CP} = 10 MHz, outputs open, V _{IN} = 3.4 V or V _{IN} = GND, one bit toggling at f _I = 5 MHz, 50 percent duty cycle	ALL	1, 2, 3		6.0		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C V _{CC} = 5.0 V dc ±10%	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Functional tests	7/	See 4.3.1d	All	7, 8			
Input capacitance	C _{IN}	See 4.3.1c	All	4		10	pF
Output capacitance	C _{OUT}	See 4.3.1c	All	4		12	pF
Propagation delay time CP to Q _n (PE input high)	t _{PLH1} t _{PHL1}	C _L = 50 pF minimum R _L = 500Ω 8/ See figure 5	01,02	9,10,11	2.0	11.5	ns
			03	9,10,11	2.0	7.5	
Propagation delay time CP to Q _n (PE input low)	t _{PLH2} t _{PHL2}		01,02	9,10,11	2.0	10.0	ns
			03	9,10,11	2.0	6.5	
Propagation delay time CP to TC	t _{PLH3} t _{PHL3}		01,02	9,10,11	2.0	16.5	ns
			03	9,10,11	2.0	10.8	
Propagation delay time CET to TC	t _{PLH4} t _{PHL4}		01,02	9,10,11	1.5	9.0	ns
			03	9,10,11	1.5	5.9	
Propagation delay time MR to TC	t _{PHL5}		01,02	9,10,11	2.0	12.5	ns
			03	9,10,11	2.0	8.2	
Propagation delay time MR to Qn	t _{PHL6}		01,02	9,10,11	2.0	14.0	ns
			03	9,10,11	2.0	9.1	

- 1/ For dynamic operation of device type 01, a V_{IH} level between 2.0 V and 3.0 V may be recognized by this device as a high logic level input. For static operation of device type 01, a V_{IH} ≥ 2.0 V will be recognized by this device as a high logic level input. Users are cautioned to verify that this change will not affect their system.
- 2/ Guaranteed by testing at worst case condition of V_{CC} = 3 volts.
- 3/ Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed 1 second.
- 4/ In accordance with TTL driven input (V_{IN} = 3.4 V dc); all other outputs at V_{CC} or GND.
- 5/ This parameter is not directly testable, but is derived for use in total power supply calculations.
- 6/ $I_{CC} = I_{CCQ} + (\Delta I_{CC} \times D_H \times N_I) + I_{CCD} (f_{cp}/2 + f_I \times N_I)$.
Where D_H = Duty cycle for TTL inputs high.
N_I = Number of TTL inputs at D_H.
f_I = Input frequency in MHz.
N_I = Number of inputs at f_I.
- 7/ Due to internal noise problems, device type 01 cannot meet the threshold limits required in accordance with MIL-STD-883, test method 5004, for the V_{IH} minimum limit (2.0 V) of this technology family. For device types 02 and 03, use a V_{IH} limit of 3.0 V. The V_{IL} limit (0.8 V) remains unchanged. Users are cautioned to verify that this change will not affect their system.
- 8/ Minimum limits are guaranteed, if not tested, on propagation delays.

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Device types	01, 02, 03	
Case outline	E and F	2
Terminal number	Terminal symbol	
1	\overline{MR}	NC
2	CP	\overline{MR}
3	P_0	CP
4	P_1	P_0
5	P_2	P_1
6	P_3	NC
7	CEP	P_2
8	GND	P_3
9	PE	CEP
10	CET	GND
11	Q_3	NC
12	Q_2	PE
13	Q_1	CET
14	Q_0	Q_3
15	TC	Q_2
16	V_{CC}	NC
17	---	Q_1
18	---	Q_0
19	---	TC
20	---	V_{CC}

PIN description	
Terminal symbol	Description
CEP	Count enable parallel input
CET	Count enable trickle input
CP	Clock pulse input (active rising edge)
\overline{MR}	Asynchronous master reset input (active low)
P_{0-3}	Parallel data inputs
\overline{PE}	Parallel enable input (active low)
Q_{0-3}	Flip-flop outputs
TC	Terminal count output

FIGURE 1. Terminal connections.

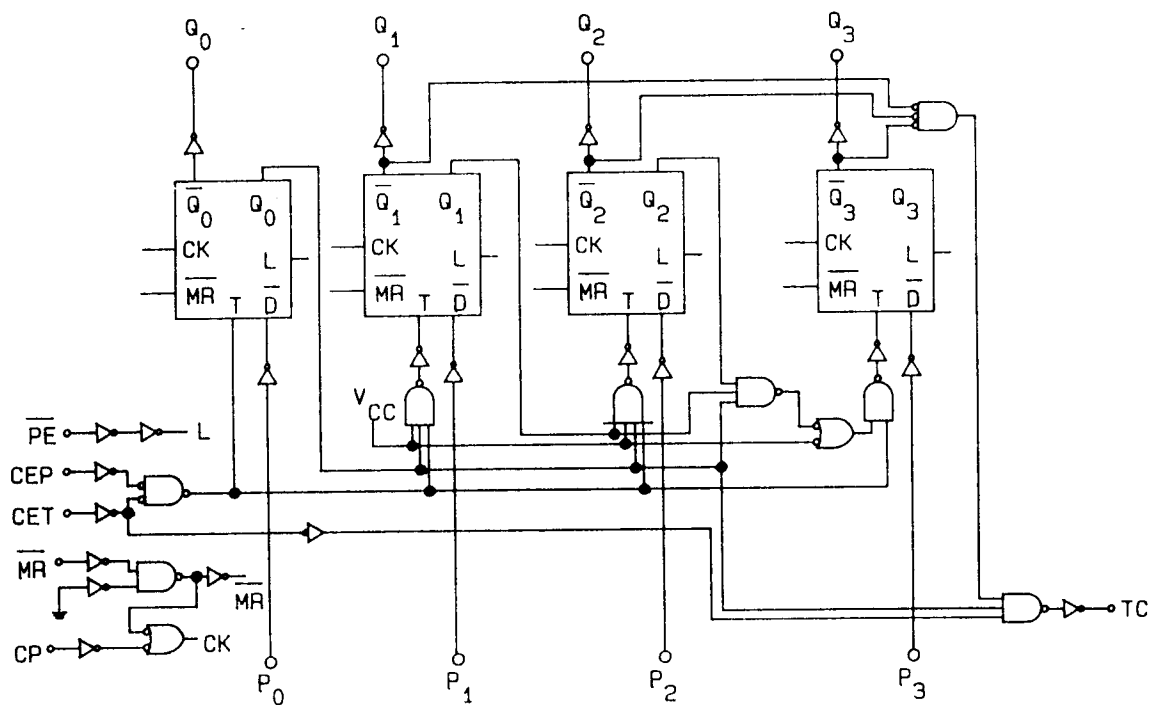
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\overline{MR}	\overline{PE}	CET	CEP	Function
L	X	X	X	Reset (clear)
H	L	X	X	Load (P_n to Q_n) (See note)
H	H	H	H	Count (increment) (See note)
H	H	L	X	No change (hold) (See note)
H	H	X	L	No change (hold) (See note)

H = High voltage level steady-state.
L = Low voltage level steady-state.
X = Irrelevant.

NOTE: Action on the rising clock edge.

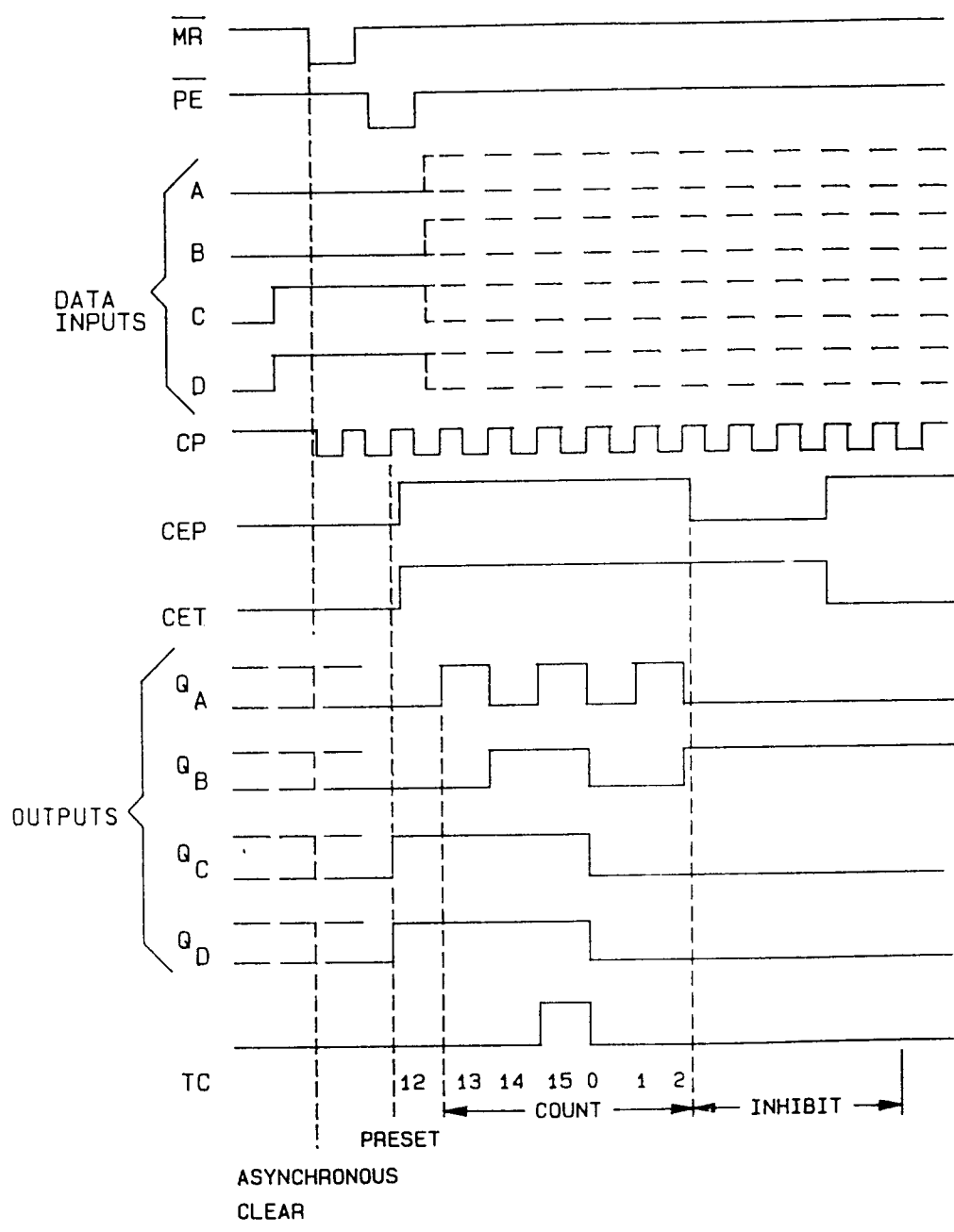
FIGURE 2. Truth table.



CK = INTERNAL CLOCK

FIGURE 3. Logic diagram.

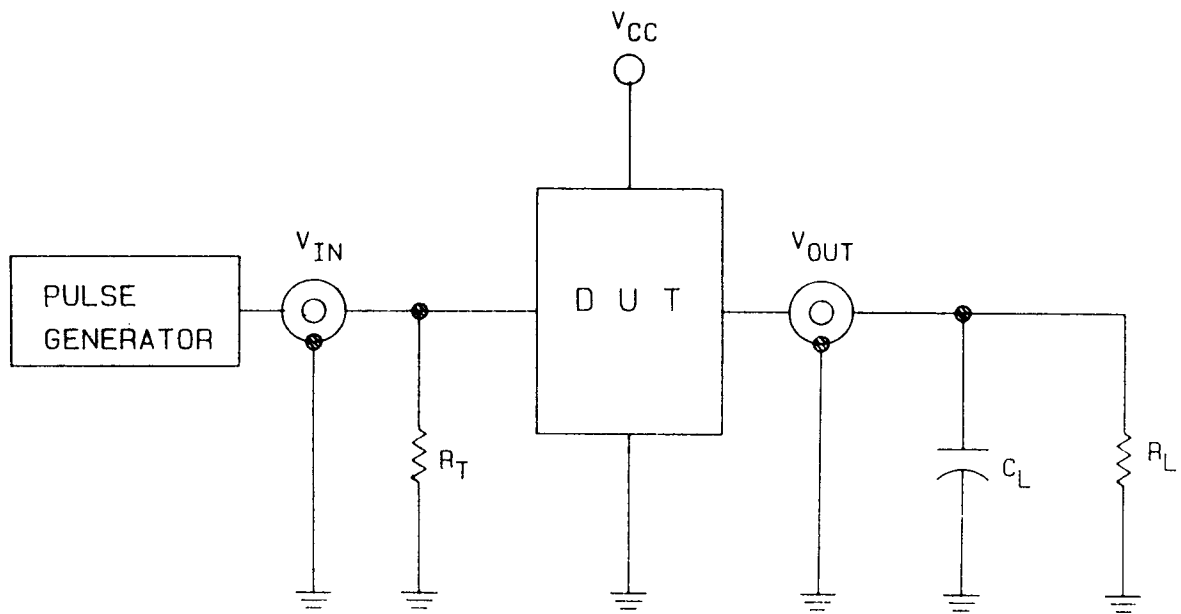
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- SEQUENCE AS FOLLOWS:
1. Clear outputs to zero.
 2. Preset to binary 12.
 3. Count to 13, 14, 15, 0, 1, and 2.
 4. Inhibit.

FIGURE 4. Counting sequence.

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Definitions:

- R_L = Load resistor = 500 Ω .
- C_L = Load capacitance = 50 pF minimum, includes jig and probe capacitance.
- R_T = Termination should be equal to Z_{OUT} of pulse generators.

FIGURE 5. Switching waveforms and test circuit.

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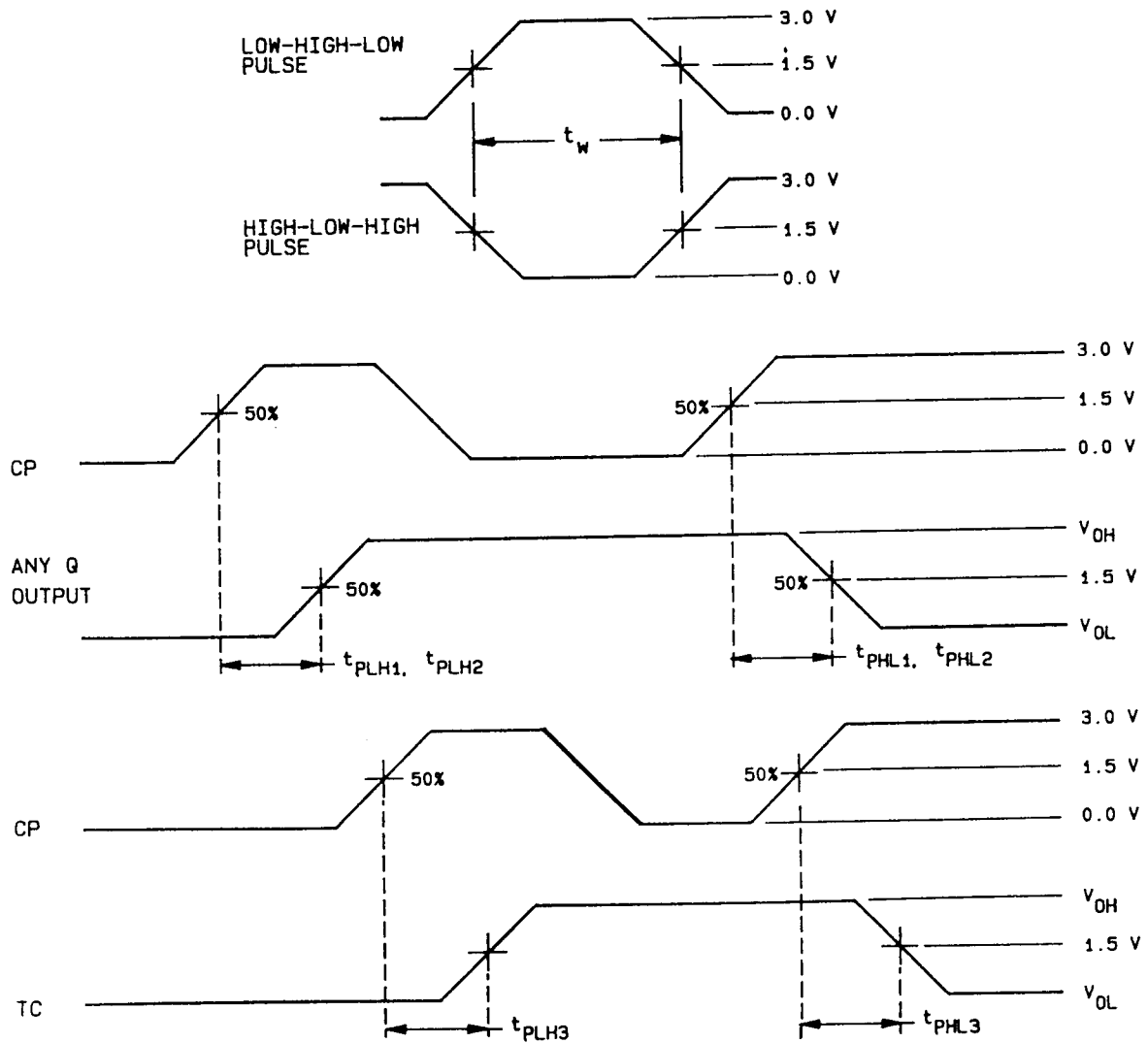


FIGURE 5. Switching waveforms and test circuit - Continued.

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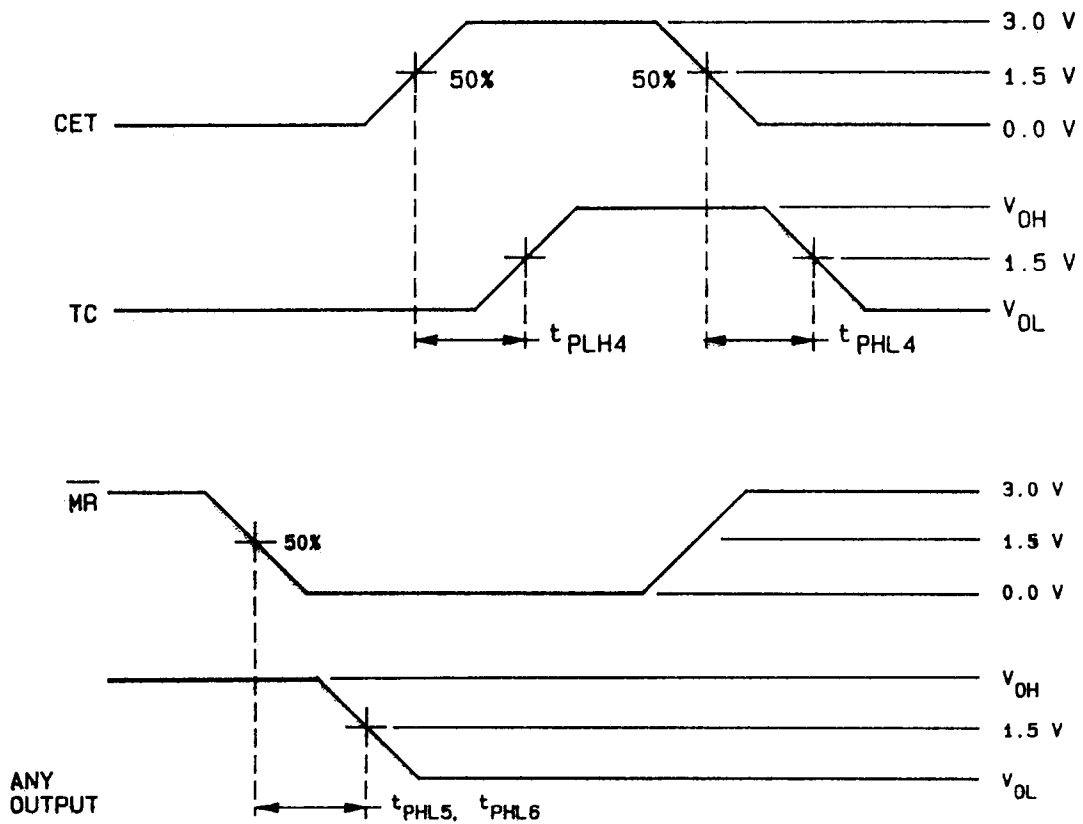


FIGURE 5. Switching waveforms and test circuit - Continued.

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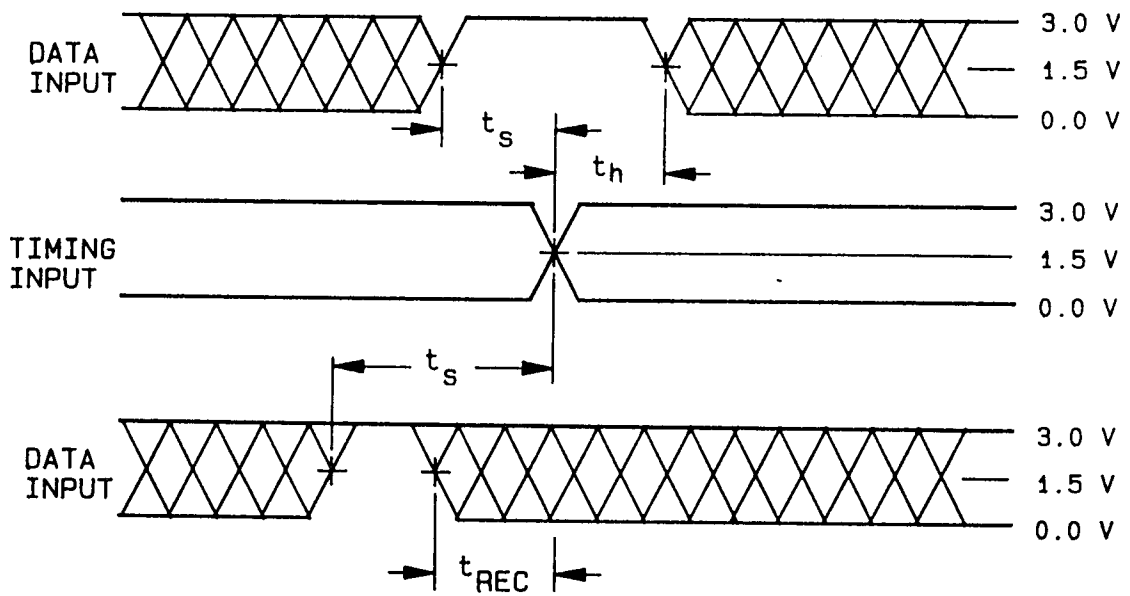


FIGURE 5. Switching waveforms and test circuit - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only initial test and after process or design changes which may affect capacitance.
- d. Subgroups 7 and 8 tests shall verify the truth table as specified on figure 2.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

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