REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added vendor CAGE 1ES66 to devices 03 and 04. Made changes to table I. Editorial changes throughout.	90 DEC 03	M.A. Frye

REV																								
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REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A									A	A	A					
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18					

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Rick Officer

CHECKED BY: Ray Monnin

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 12 JULY 1989

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, CMOS 8-BIT A/D CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89616
A	67268	

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E050

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89616	01	V	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADC-908A	CMOS microprocessor-compatible FAST 8-bit A/D converter
02	ADC-908B	CMOS microprocessor-compatible FAST 8-bit A/D converter
03	PM-7574A	CMOS microprocessor-compatible 8-bit A/D converter
04	PM-7574B	CMOS microprocessor-compatible 8-bit A/D converter

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
V	D-6 (18-lead, .960" x .310" x .200"), dual-in-line package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

V_{DD} to AGND	0 V dc, +7 V dc
V_{DD} to DGND	0 V dc, +7 V dc
AGND to DGND	±0.3 V dc
Digital input voltage ($\overline{RD}$, $\overline{CS}$ pins) to DGND	-0.3 V dc, V_{DD}
Digital output voltage (D_{B0}-D_{B7}, $\overline{BUSY}$ pins) to DGND	-0.3 V dc, V_{DD}
Clock input voltage to (CLK pins) DGND	-0.3 V dc to V_{DD}
Voltage at V_{REF}	-0 V dc, -20 V dc
Voltage at V_{BOFS}	±20 V dc
Voltage at V_{AIN}	±20 V dc
Power dissipation:	
To +75°C	450 mW
Derate above +75°C (cases V and 2)	6.0 mW/°C
Ambient operating temperature range (T_A)	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambeint (θ_{JA}):	
Cases V and 2	35°C/W

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1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+5 V dc
Reference voltage (V_{REF})	-10 V dc
Ground	AGND = DGND = 0 V dc
Clock resistance (R_{CLK}):	
Devices 01 and 02	43 kΩ
Devices 03 and 04	150 kΩ
Clock capacitance (C_{CLK})	100 pF

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{DD} = +5 V, V_{REF} = -10 V AGND = DGND = 0 V Unipolar configuration unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Integral nonlinearity 1/	INL		1,2,3	01,03		±.5	LSB
				02,04		±.75	
Differential nonlinearity 1/	DNL		1,2,3	01,03		±.75	LSB
				02,04		±7/8	
Gain error 2/	AE		1	01,03		±3.0	LSB
				02,04		±5.0	
			2,3	01,03		±4.5	
				02,04		±6.5	
Offset error	VOS		1	01,03		±30.0	mV
				02,04		±60.0	
			2,3	01,03		±50.0	
				02,04		±80.0	
Resistance mismatch B_{OFS} to A_{AIN}	delta R_{AB}		1,2,3	01,02		±1.0	%
				03,04		±1.5	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{DD} = +5 V, V_{REF} = -10 V AGND = DGND = 0 V Unipolar configuration unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input resistance	R_{IN}	V_{REF} pins	1,2,3	All	5	15	kΩ
		B_{OFS} pins			10	30	
		A_{IN} pins			10	30	
Digital input high level	V_{IH}	$\overline{RD}$, $\overline{CS}$ 3/	1,2,3	All	2.4		V
Digital input low level	V_{IL}	$\overline{RD}$, $\overline{CS}$ 3/	1,2,3	All		0.8	V
Digital input current	I_{IN}	V_{IN} = 0 V or V_{DD}	1	All		±1.0	µA
			2,3			±10.0	
Clock input high level	V_{IH}	Clock 3/	1,2,3	01,02	2.4		V
				03,04	3.0		
Clock input low level	V_{IL}	Clock 3/	1,2,3	01,02		0.8	V
				03,04		0.4	
Clock input high current	I_{IH}	Clock, V_{IN} = V_{DD}	1	All		±2.0	mA
Clock input low current	I_{IL}	Clock, V_{IN} = 0 V	1	All		+1.0	µA
			2,3			±10.0	
Digital output high level DB7-DB0; $\overline{BUSY}$	V_{OH}	I_{SOURCE} = 40 µA	1,2,3	All	4.0		V
Digital output low level DB7-DB0; $\overline{BUSY}$	V_{OL}	I_{SINK} = 1.6 mA	1,2,3	All		0.4	V
Floating state leakage current (DB7-DB0)	I_{LKG}	V_O = 0 V or V_{DD}	1	All		±1.0	µA
			2,3			±10.0	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{DD} = +5 V, V_{REF} = -10 V AGND = DGND = 0 V Unipolar configuration unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current from V_{DD}	I_{DD}	A_{IN} = 0 V, $\overline{BUSY}$ and RD high	1,2,3	01,02		2.5	mA
				03,04		5.0	
Digital input capacitance	C_{IN}	See 4.3.1c	4	All		5.0	pF
Floating state output capacitance (DB7-DB0)	C_{OUT}	See 4.3.1c	4	All		7.0	pF
Functional test		See 4.3.1d	7,8	All			
$\overline{CS}$ pulse width 4/	t_{CS}		9	01,02	60		ns
			10,11		90		
			9,10,11	03,04	150		
$\overline{RD}$ to $\overline{CS}$ setup time 5/	t_{WSCS}		9,10,11	All	0		ns
$\overline{CS}$ to $\overline{BUSY}$ propagational delay 5/	t_{CBPD}	$\overline{BUSY}$ load = 20 pF	9	01,02		120	ns
				03,04		180	
			10,11	01,02		150	
				03,04		180	
		$\overline{BUSY}$ load = 100 pF	9	01,02		150	
				03,04		200	
			10,11	All		200	
$\overline{BUSY}$ to $\overline{RD}$ setup time 4/	t_{BSR}		9,10,11	All	0		ns
$\overline{BUSY}$ to $\overline{CS}$ setup time 4/	t_{BSCS}		9,10,11	All	0		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{DD} = +5 V, V_{REF} = -10 V AGND = DGND = 0 V Unipolar configuration unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid propagational delay 4/	t_{RAD}	Load = 20 pF	9	01,02		140	ns
			10,11			200	
			9,10,11	03,04		220	
Data valid propagational delay 5/	t_{RAD}	Load = 100 pF	9	01,02		170	ns
			10,11			230	
			9,10,11	03,04		400	
Data valid hold time 4/	t_{RHD}		9	01,02	30	100	ns
			10,11		40	140	
			9,10,11	03,04	80	180	
$\overline{CS}$ to $\overline{RD}$ hold time 4/	t_{RHCS}		9	01,02		200	ns
			10,11			250	
			9,10,11	03,04		500	
Reset time requirement 4/	t_{RESET}		9	01,02	450		ns
			10,11		500		
			9,10,11	03,04	3.0		µs
$\overline{RD}$ to $\overline{BUSY}$ propagation delay 4/	t_{WBPD}	$\overline{BUSY}$ load = 20 pF	9	01,02		600	ns
			10,11			800	
			9,10,11	03,04		2	µs
Conversion time 1/ 5/	t_C		9,10,11	01,02		6	µs
				03,04		15	

1/ Devices 01 and 02 measured using external clock frequency of 1.35 MHz. Devices 03 and 04 measured using external clock frequency of 550 kHz. See timing waveforms on figure 3.

2/ Gain error is measured after calibration out offset error.

3/ Guaranteed by functional pattern testing in external clock RAM, ROM, and SLOW modes.

4/ Static RAM interface mode.

5/ Guaranteed, if not tested, to the limits specified in table I herein.

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Device types	01, 02, 03, and 04	
Case outlines	V	2
Terminal number	Terminal symbol	
1	V_{DD}	NC
2	V_{REF}	V_{DD}
3	B_{OFS}	V_{REF}
4	A_{IN}	B_{OFS}
5	AGND	A_{IN}
6	D_{B7}	AGND
7	D_{B6}	D_{B7}
8	D_{B5}	D_{B6}
9	D_{B4}	D_{B5}
10	D_{B3}	D_{B4}
11	D_{B2}	NC
12	D_{B1}	D_{B3}
13	D_{BO}	D_{B2}
14	$\overline{BUSY}$	D_{B1}
15	$\overline{RD}$	D_{BO}
16	$\overline{CS}$	$\overline{BUSY}$
17	CLK	$\overline{RD}$
18	DGND	$\overline{CS}$
19	---	CLK
20	---	DGND

FIGURE 1. Terminal connections.

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Device types 01 and 02

Truth table, static RAM mode

Inputs		Outputs		Operation
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	D_{B7} - D_{B0}	
L	H	H	High Z	Start convert (write cycle)
L	↓	H	High Z to Data	Read data (read cycle)
L	↑	H	Data to High Z	Reset converter
H	X (SEE NOTE)	X	High Z	No effect (not selected)
L	H	L	High Z	No effect (converter busy)
L	↓	L	High Z	No effect (converter busy)
L	↑ (SEE NOTE)	L	High Z	Conversion error not allowed

NOTE: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

FIGURE 2. Truth tables.

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Device types 03 and 04

Static RAM mode

Inputs		Outputs		Operation
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	D_{B7} - D_{B0}	
↓	H	↓	High Z	Start convert (write cycle)
L	↓	H	High Z to Data	Read data (read cycle)
L	↑	H	Data to High Z	Reset converter
H	X (SEE NOTE)	X	High Z	No effect (not selected)
L	H	L	High Z	No effect (converter busy)
L	↓	L	High Z	No effect (converter busy)
L	↑ (SEE NOTE)	L	High Z	Conversion error not allowed

NOTE: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

FIGURE 2. Truth tables - Continued.

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Device types 01, 02, 03 and 04

Slow-memory mode

Inputs	Outputs		
$\overline{CS}$ and $\overline{RD}$	$\overline{BUSY}$	D_{B7} - D_{B0}	Operation
H	H	High Z	No effect (not selected)
↓	↓	High Z	Start conversion
L	L	High Z	Conversion in progress µP in WAIT state
L	↑	High Z to Data	Conversion complete read data
↑ (SEE NOTE)	H	Data to High Z	Reset and deselect converter

NOTE: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

FIGURE 2. Truth tables - Continued.

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Device types 01, 02, 03, and 04

ROM mode

Inputs		Outputs		Operation
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	D_{B7} - D_{B0}	
L	↓	H	High Z to Data	Read data
L	↑	↓	Data to High Z	Reset and start new converter
L	↓	L	High Z	No effect (converter busy)
L	↑ (SEE NOTE)	L	High Z	Conversion error not allowed

NOTE: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

FIGURE 2. Truth tables - Continued.

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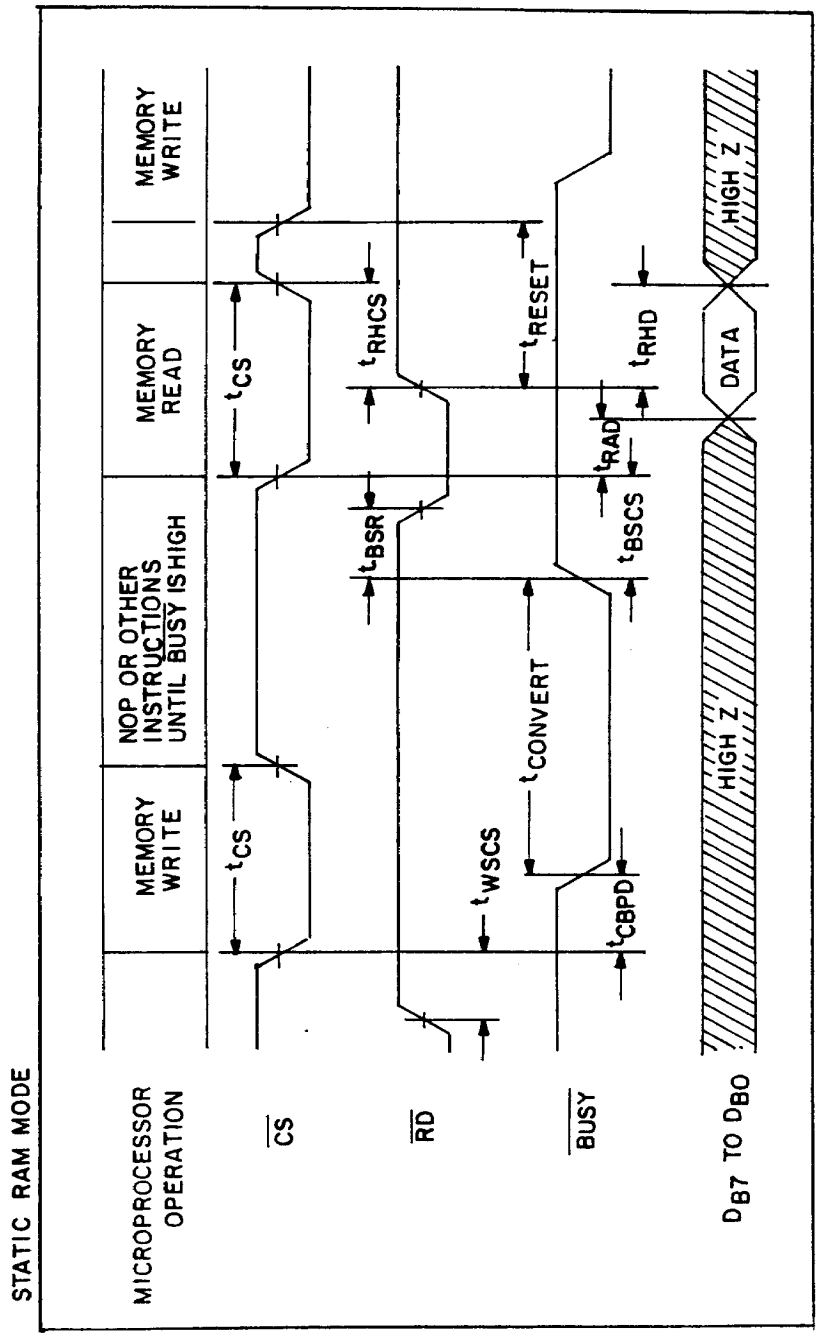

FIGURE 3. Timing waveforms.

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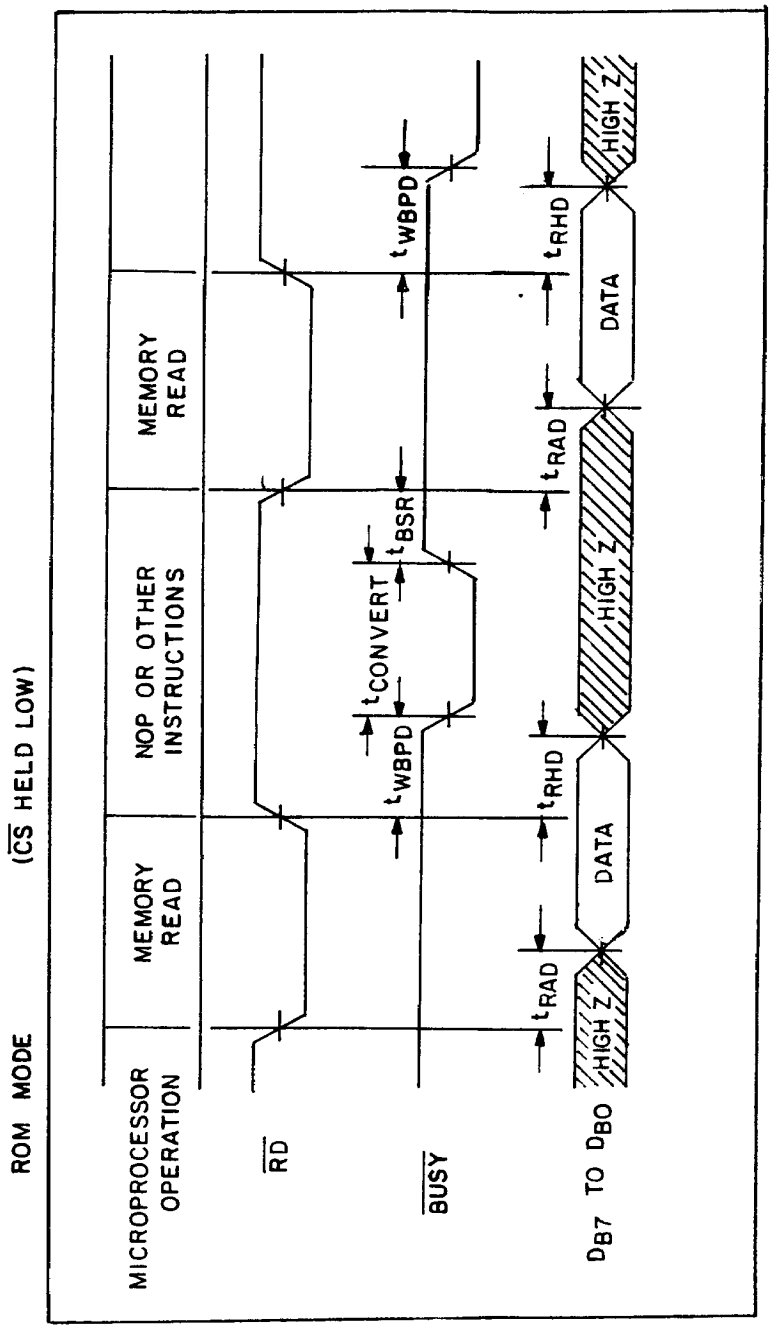

FIGURE 3. Timing waveforms - Continued.

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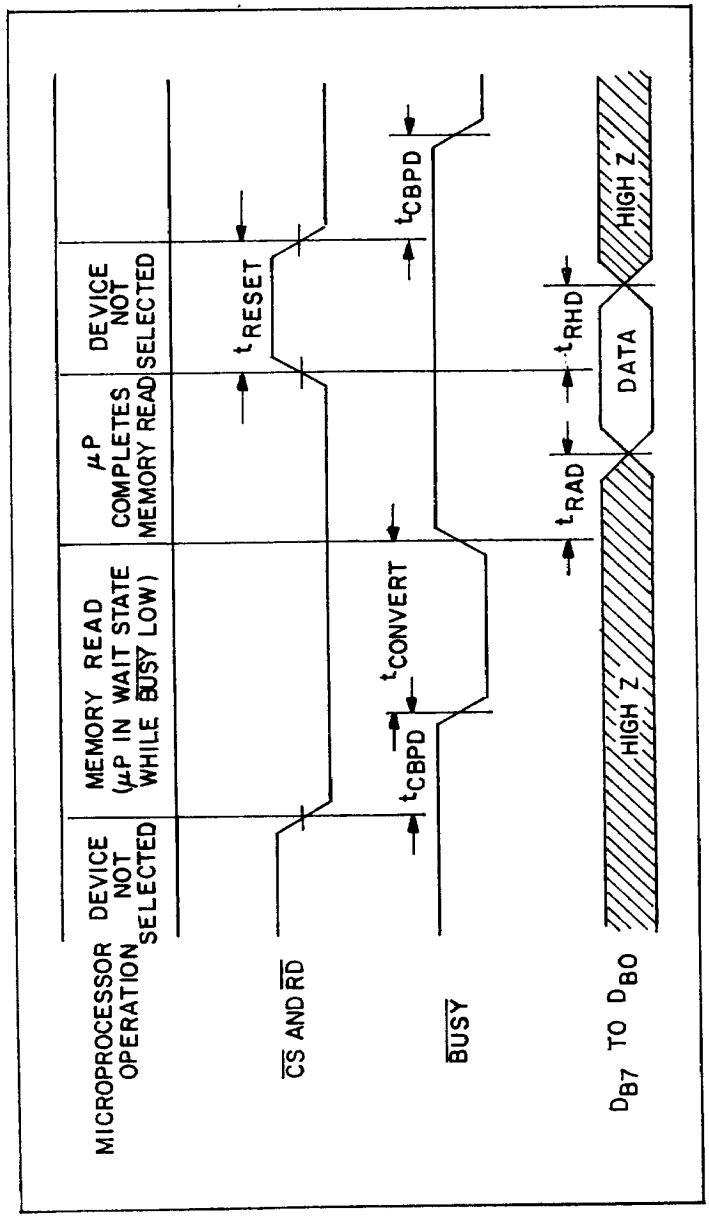

NOTE: For device types 01 and 02, t_{RAD} timing is measured at +2 V and +0.8 V.

FIGURE 3. Timing waveforms - Continued.

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3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3
Group A test requirements (method 5005)	1, 2, 3, 4, 7**, 8**, 9, 10***, 11***
Groups C and D end-point electrical parameters (method 5005)	

* PDA applies to subgroup 1.
** See 4.3.1d.
*** Subgroups 10 and 11 are guaranteed if not tested.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

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6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

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STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 03 DECEMBER 1990

Approved sources of supply for SMD 5962-89616 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-8961601VX	06665	ADC-908AX
5962-8961602VX	06665	ADC-908BX
5962-89616022X	06665	ADC-908RC
5962-8961603VX	06665	PM-7574AX
	1ES66	MX7574TQ/883B
5962-89616032X	1ES66	MX7574TE/883B
5962-8961604VX	06665	PM-7574BX
	1ES66	MX7574SQ/883B
5962-89616042X	06665	PM-7574BRC
	1ES66	MX7574SE/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
06665	Precision Monolithics Incorporated 1500 Space Park Drive P.O. Box 58020 Santa Clara, CA 95052-8020
1ES66	Maxim Integrated Products 120 San Gabriel Drive Sunnyvale, CA 94086

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.

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