



T-5230-08

June 1992

74BCT652 Transceiver/Register

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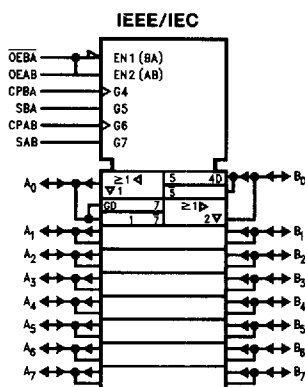
General Description

This device consists of a bus transceiver circuit with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

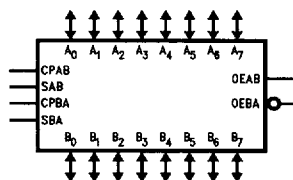
Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Logic Symbols



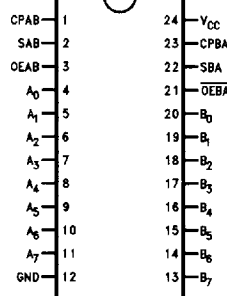
TL/F/10950-1



TL/F/10950-3

Connection Diagrams

Pin Assignment DIP and SOIC



TL/F/10950-2

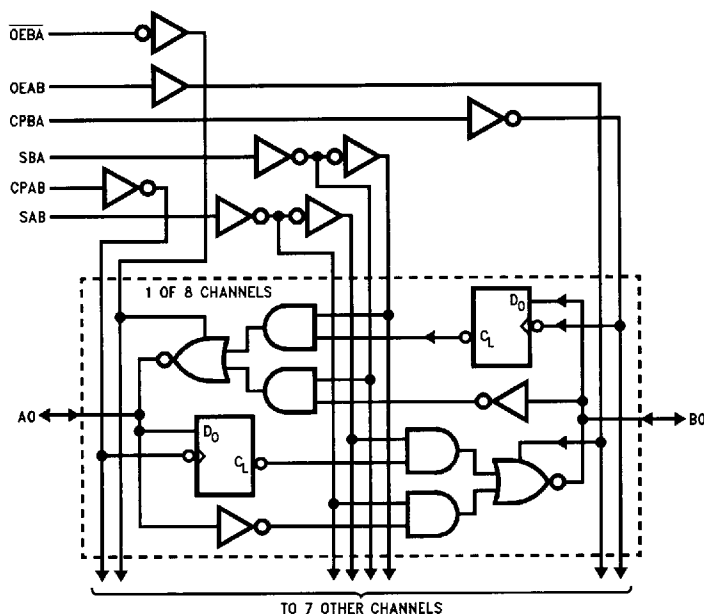
9000-3491

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Pin Names	Description
A ₀ –A ₇ , B ₀ –B ₇	A and B Inputs/ TRI-STATE® Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, OEBA	Output Enable Inputs

Logic Diagram



TL/F/10950-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with this device.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appro-

priate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

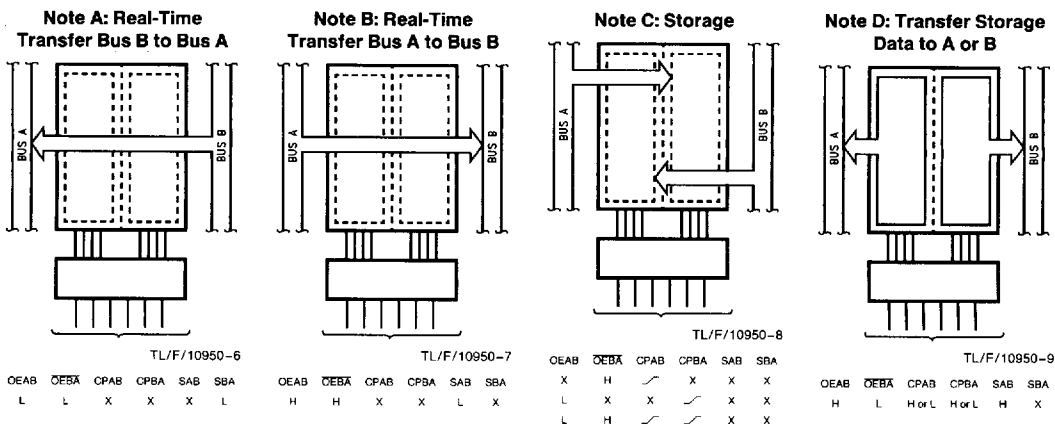


FIGURE 1

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Inputs						Inputs/Outputs (Note 1)		Operating Mode
OEAB	OEBA	CPAB	CPBA	SAB	SBA	A ₀ thru A ₇	B ₀ thru B ₇	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H			X	X			Store A and B Data
X	H		H or L	X	X	Input	Not Specified	Store A, Hold B
H	H			X	X	Input	Output	Store A in Both Registers
L	X	H or L		X	X	Not Specified	Input	Hold A, Store B
L	L			X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L			Real-Time B Data to A Bus
L	L	X	H or L	X	H	Input	Output	Store B Data to A Bus
H	H	X	X	L	X			Real-Time A Data to B Bus
H	H	H or L	X	H	X	Output	Output	Stored A Data to B Bus
H	L	H or L	H or L	H	H			Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
/ = LOW to HIGH Clock Transition

Note 1: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Any Output
in the Disable or Power-Off State
in the HIGH State

-0.5V to +5.5V
-0.5V to V_{CC}

Current Applied to Output
in LOW State (Max)

twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min)

4000V

DC Latchup Source Current

500 mA

Over Voltage Latchup

V_{CC} + 4.5V

Recommended Operating Conditions

Free Air Ambient Temperature
Commercial

0°C to +70°C

Supply Voltage
Commercial

+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I _{OH} = -3 mA I _{OH} = -15 mA
V _{OL}	Output LOW Voltage			0.55	V	Min	I _{OL} = 64 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V (Non I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V (Non I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown (I/O)			100	μA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{IL}	Input LOW Current			-250	μA	Max	V _{IN} = 0.5V (Non I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (A _n , B _n)
I _{IL} + I _{OZL}	Output Leakage Current			-225	μA	Max	V _{OUT} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current	-100		-225	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			100	μA	0.0V	V _{OUT} = 5.25V (A _n , B _n)
I _{COH}	Power Supply Current		15	22	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		40	49	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		15	22	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

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Symbol	Parameter	74BCT			74BCT		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	
f_{max}	Max. Clock Frequency	90	172		90		MHz
t_{PLH}	Propagation Delay	2.8	5.9	8.8	2.8	9.9	ns
t_{PHL}	Clock to Bus	2.8	5.1	8.8	2.8	9.9	
t_{PLH}	Propagation Delay	1.7	4.6	7.5	1.7	8.9	ns
t_{PHL}	Bus to Bus	2.4	5.8	9.2	2.4	9.8	
t_{PLH}	Propagation Delay	3.0	7.0	11.0	3.0	11.3	ns
t_{PHL}	SBA to A or SAB to B	2.4	6.6	11.0	2.4	11.3	
t_{PZH}	Enable Time	2.5	5.5	8.9	2.5	10.6	ns
t_{PZL}	*OEBA to A	3.2	6.3	10.1	3.2	10.6	
t_{PHZ}	Disable Time	1.8	5.4	8.6	1.8	9.5	
t_{PLZ}	*OEBA to A	2.4	5.4	8.6	2.4	9.5	
t_{PZH}	Enable Time	1.5	4.6	7.1	1.5	8.1	
t_{PZL}	OEAB to B	2.3	5.2	8.1	2.3	8.1	
t_{PHZ}	Disable Time	2.2	5.2	9.1	2.2	9.1	ns
t_{PLZ}	OEAB to B	2.2	5.2	8.0	2.2	8.0	

AC Operating Requirements

Symbol	Parameter	74BCT		74BCT		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	
$t_s(\text{H})$	Setup Time, HIGH or LOW, Bus to Clock	5.0		5.0		ns
$t_s(\text{L})$		5.0		5.0		
$t_h(\text{H})$	Hold Time, HIGH or LOW, Bus to Clock	1.0		1.0		ns
$t_h(\text{L})$		1.0		1.0		
$t_w(\text{H})$	Clock Pulse Width HIGH or LOW	5.0		5.0		ns
$t_w(\text{L})$		5.0		5.0		

Extended AC Electrical Characteristics

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Symbol	Parameter	74BCT		74BCT		74BCT		Units
		$T_A = \text{Com}$ $V_{CC} = \text{Com}$ $C_L = 50 \text{ pF}$ 8 Outputs Switching (Note 1)		$T_A = \text{Com}$ $V_{CC} = \text{Com}$ $C_L = 250 \text{ pF}$ 1 Output Switching (Note 2)		$T_A = \text{Com}$ $V_{CC} = \text{Com}$ $C_L = 250 \text{ pF}$ 8 Outputs Switching (Notes 1, 2)		
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	2.8	10.5	3.0	12.0	4.0	15.6	ns
t_{PHL}	Clock to Bus	2.8	10.5	3.0	12.0	4.0	15.6	
t_{PLH}	Propagation Delay	2.0	9.5	2.5	10.9	4.0	15.0	ns
t_{PHL}	Bus to Bus	3.0	11.0	3.0	11.5	4.0	15.0	
t_{PLH}	Propagation Delay	3.0	12.5	3.0	14.2	4.0	18.1	ns
t_{PHL}	SBA to A or SAB to B	3.0	12.5	3.0	14.2	4.0	18.1	

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

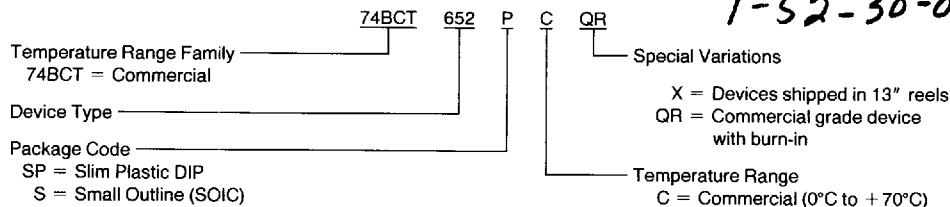
Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitor the standard AC load. This specification pertains to single output switching only.

Capacitance

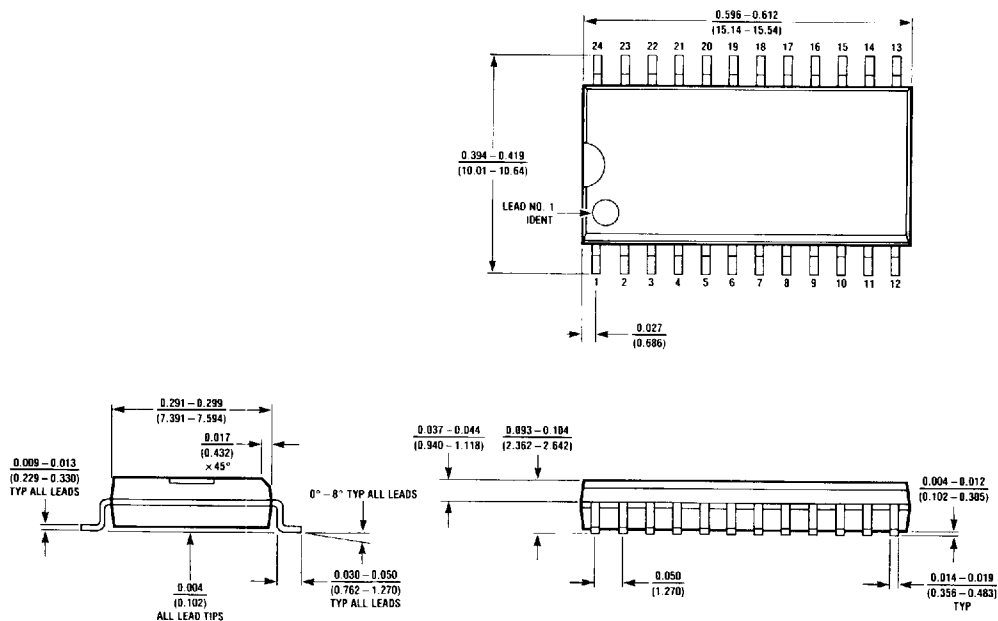
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	6.0	pF	$V_{CC} = 5.0V$ (Control Inputs)
$C_{I/O}$	Input/Output Pin Capacitance	12.5	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

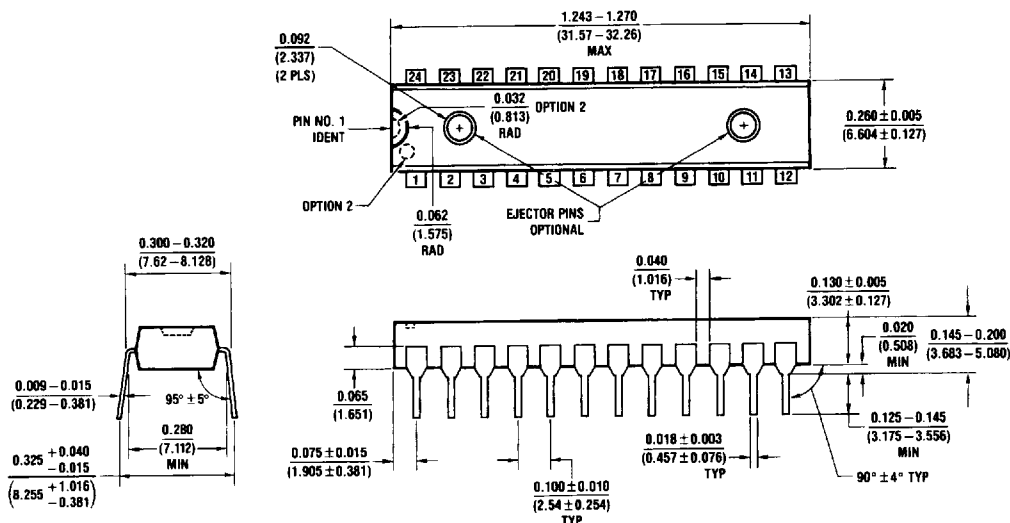


24 Lead Small Outline Integrated Circuit (S)
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)

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Lit # 114868



N24C (REV F)

24 Lead Slim (0.300" Wide) Plastic Dual-In-Line Package (SP)
NS Package Number N24C

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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