

# AKM628128 Series

131072-Word × 8-Bit High Speed CMOS Static RAM

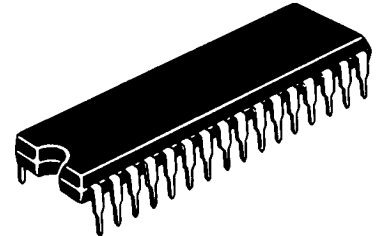
The AKM628128 is a CMOS static RAM organized 128-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525 mil SOP (460-mil body SOP) or a 600-mil plastic DIP, or a 8 × 20mm TSOP with thickness of 1.2 mm is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

## Features

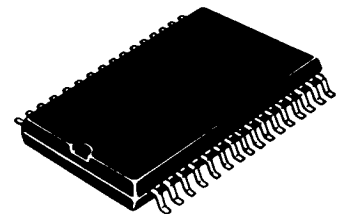
- High speed: Fast access time 70/85/100/120 ns (max.)
- Low power
  - Standby: 10 μW (typ) (L-version)
  - Operation: 75 mW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-version)
  - 2 chip selection for battery back up

AKM628128P Series



(DP-32)

AKM628128FP Series

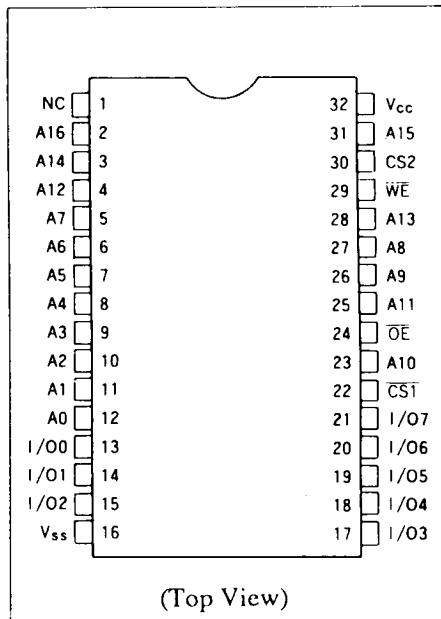


(FP-32D)

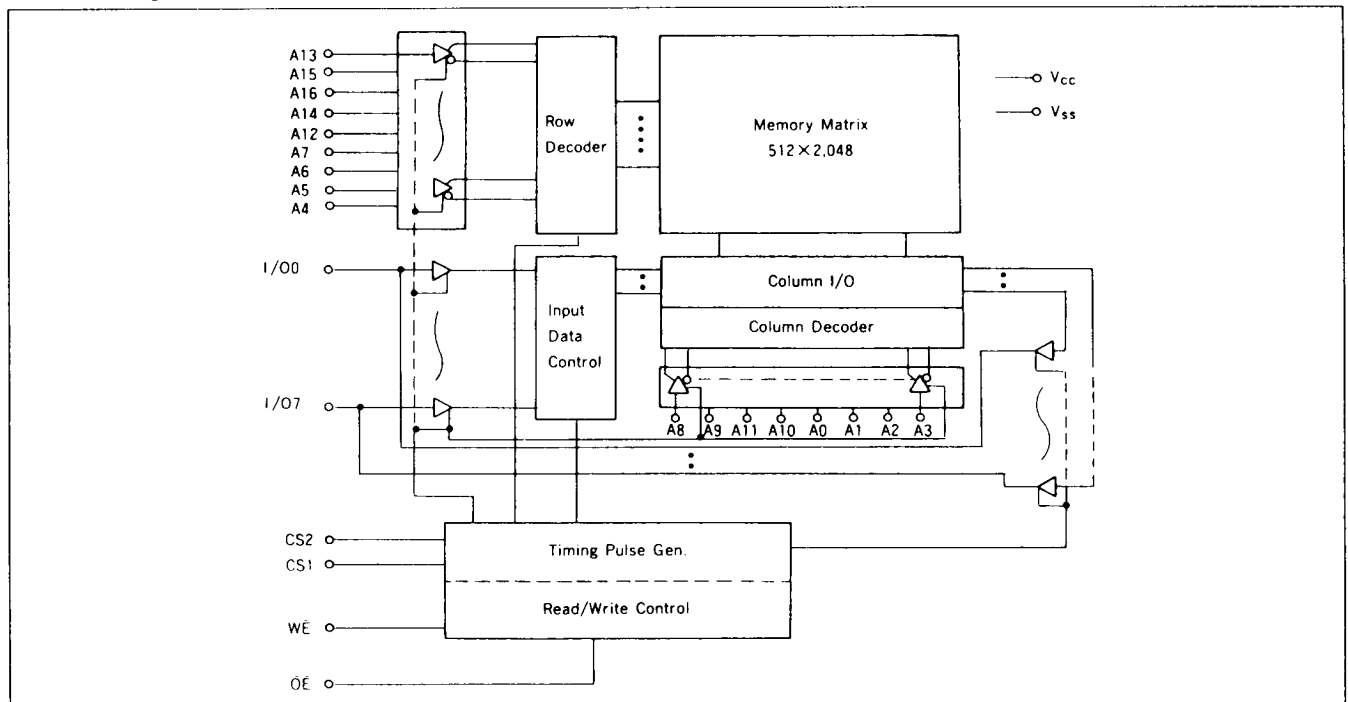
## ORDERING INFORMATION

Type No.	Access Time	Package	Type No.	Access Time	Package		
AKM628128P-7	70ns	600-mil 32-pin plastic DIP (DP-32)	AKM628128T-7	70ns	8mm × 20mm 32-pin TSOP (normal type) (TFP-32D)		
AKM628128P-8	85ns		AKM628128T-8	85ns			
AKM628128P-10	100ns		AKM628128T-10	100ns			
AKM628128P-12	120ns		AKM628128T-12	120ns			
AKM628128LP-7	70ns		AKM628128LT-7	70ns			
AKM628128LP-8	85ns		AKM628128LT-8	85ns			
AKM628128LP-10	100ns		AKM628128LT-10	100ns			
AKM628128LP-12	120ns		AKM628128LT-12	120ns			
AKM628128LP-7SL	70ns		AKM628128LT-7L	70ns			
AKM628128LP-8SL	85ns		AKM628128LT-8L	85ns			
AKM628128LP-10SL	100ns		AKM628128LT-10L	100ns			
AKM628128LP-12SL	120ns		AKM628128LT-12L	120ns			
AKM628128FP-7	70ns		525-mil 32-pin plastic SOP (FP-32D)	AKM628128R-7		70ns	8mm × 20mm 32-pin TSOP (reverse type) (TFP-32DR)
AKM628128FP-8	85ns			AKM628128R-8		85ns	
AKM628128FP-10	100ns			AKM628128R-10		100ns	
AKM628128FP-12	120ns			AKM628128R-12		120ns	
AKM628128LFP-7	70ns	AKM628128LR-7		70ns			
AKM628128LFP-8	85ns	AKM628128LR-8		85ns			
AKM628128LFP-10	100ns	AKM628128LR-10		100ns			
AKM628128LFP-12	120ns	AKM628128LR-12		120ns			
AKM628128LFP-7SL	70ns	AKM628128LR-7L		70ns			
AKM628128LFP-8SL	85ns	AKM628128LR-8L		85ns			
AKM628128LFP-10SL	100ns	AKM628128LR-10L		100ns			
AKM628128LFP-12SL	120ns	AKM628128LR-12L		120ns			

■ PIN CONFIGURATION



Block Diagram



Function Table

WE	CS1	CS2	OE	Mode	Vcc Current	Dout Pin	Ref. Cycle
x	H	x	x	Not selected	IsB, IsB1	High-Z	
x	x	L	x		IsB, IsB1	High-Z	
H	L	H	H	Output disable	Icc	High-Z	
H	L	H	L	Read	Icc	Dout	Read cycle
L	L	H	H	Write	Icc	Din	Write cycle (1)
L	L	H	L		Icc	Din	Write cycle (2)

Note: x : H or L

### Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V <sub>SS</sub>	V <sub>T</sub>	-0.5 <sup>*1</sup> to +7.0	V
Power dissipation	P <sub>r</sub>	1.0	W
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	-55 to +125	°C
Storage temperature under bias	T <sub>bias</sub>	-10 to +85	°C

Note: \*1. -3.0 V for pulse half-width ≤ 30 ns

### Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
	V <sub>SS</sub>	0	0	0	V	
Input high (logic 1) voltage	V <sub>HI</sub>	2.2	—	6.0	V	
Input low (logic 0) voltage	V <sub>IL</sub>	-0.3 <sup>*1</sup>	—	0.8	V	

Note: \*1. -3.0 V for pulse half-width ≤ 30 ns

### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

Item	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test Conditions
Input leakage current	I <sub>LI</sub>	—	—	2	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	—	2	μA	$\overline{CS1} = V_{HI}$ or CS2 = V <sub>IL</sub> or $\overline{OE} = V_{HI}$ or $\overline{WE} = V_{IL}$ , V <sub>IO</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operating power supply current: DC	I <sub>CC</sub>	—	15	35	mA	$\overline{CS1} = V_{IL}$ , CS2 = V <sub>HI</sub> , others = V <sub>HI</sub> /V <sub>IL</sub> . I <sub>VO</sub> = 0 mA
Operating power supply current	I <sub>CC1</sub>	—	45	70	mA	Min cycle, duty = 100%, $\overline{CS1} = V_{IL}$ , CS2 = V <sub>HI</sub> , others = V <sub>HI</sub> /V <sub>IL</sub> . I <sub>VO</sub> = 0 mA
	I <sub>CC2</sub>	—	15	30	mA	Cycle time = 1 μs, duty = 100%, I <sub>VO</sub> = 0 mA $\overline{CS1} \leq 0.2$ V, CS2 ≥ V <sub>CC</sub> - 0.2 V V <sub>HI</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IL</sub> ≤ 0.2 V
Standby power supply current: DC	I <sub>SB</sub>	—	1	3	mA	$\overline{CS1} = V_{HI}$ , CS2 = V <sub>HI</sub> or CS2 = V <sub>IL</sub>
Standby power supply current (1): DC	I <sub>SB1</sub>	—	0.02	2	mA	V <sub>in</sub> ≥ 0 V $\overline{CS1} \geq V_{CC} - 0.2$ V,
		—	2 <sup>*2</sup>	100 <sup>*2</sup>	μA	CS2 ≥ V <sub>CC</sub> - 0.2 V or
		—	2 <sup>*3</sup>	50 <sup>*3</sup>	μA	0 V ≤ CS2 ≤ 0.2 V
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1 mA
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1.0 mA

Notes: \*1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and specified loading.

\*2. This characteristics is guaranteed only for L-version.

\*3. This characteristics is guaranteed only for L-L/L-SL version.

### Capacitance ( Ta = 25°C, f = 1.0 MHz )

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C <sub>in</sub>	—	—	8	pF	V <sub>in</sub> = 0 V
Input/output capacitance	C <sub>io</sub>	—	—	10	pF	V <sub>io</sub> = 0 V

Note: This parameter is sampled and not 100% tested.

### AC Characteristics ( Ta = 0 to +70°C, V<sub>cc</sub> = 5 V ± 10%, unless otherwise noted )

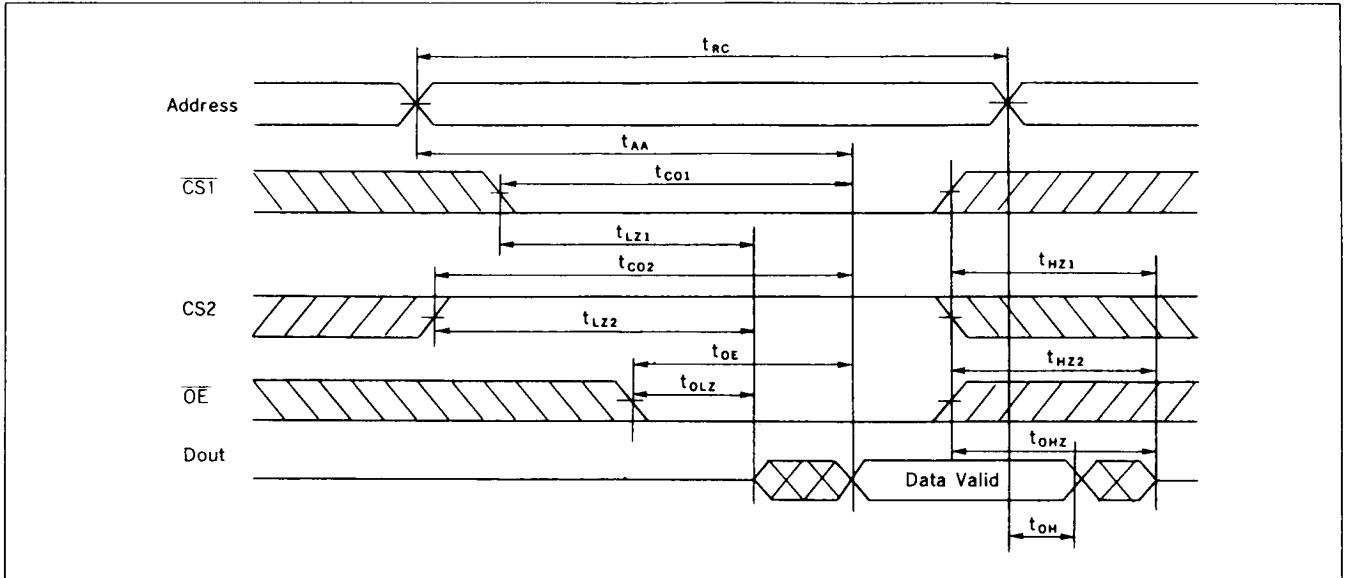
#### Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times : 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and CL (100pF)  
(Including scope & jig)

### Read Cycle

Item	Symbol	AKM628128-7		AKM628128-8		AKM628128-10		AKM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t <sub>RC</sub>	70	—	85	—	100	—	120	—	ns	
Address access time	t <sub>AA</sub>	—	70	—	85	—	100	—	120	ns	
Chip selection (CS1) to output valid	t <sub>CO1</sub>	—	70	—	85	—	100	—	120	ns	
Chip selection (CS2) to output valid	t <sub>CO2</sub>	—	70	—	85	—	100	—	120	ns	
Output enable (OE) to output valid	t <sub>OE</sub>	—	35	—	45	—	50	—	60	ns	
Chip selection (CS1) to output in low-Z	t <sub>LZ1</sub>	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Chip selection (CS2) to output in low-Z	t <sub>LZ2</sub>	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Output enable (OE) to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	5	—	5	—	ns	*1, *2, *3
Chip deselection (CS1) to output in high-Z	t <sub>HZ1</sub>	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Chip deselection (CS2) to output in high-Z	t <sub>HZ2</sub>	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output disable (OE) to output in high-Z	t <sub>OHz</sub>	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output hold from address change	t <sub>OH</sub>	10	—	10	—	10	—	10	—	ns	

### Read Timing Waveform\*4

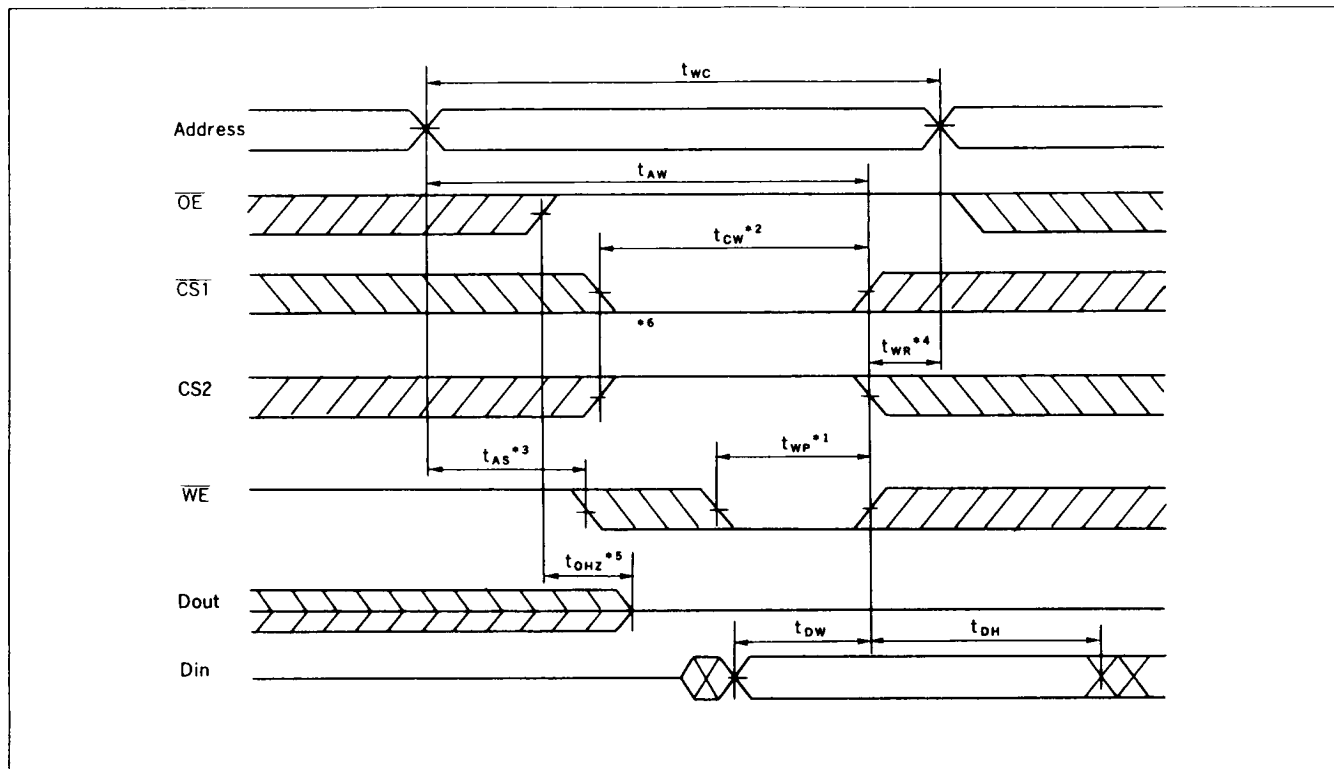


- Notes:
- \*1.  $t_{LZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
  - \*2. At any given temperature and voltage condition,  $t_{LZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  - \*3. This parameter is sampled and not 100% tested.
  - \*4.  $\overline{WE}$  is high for read cycle.

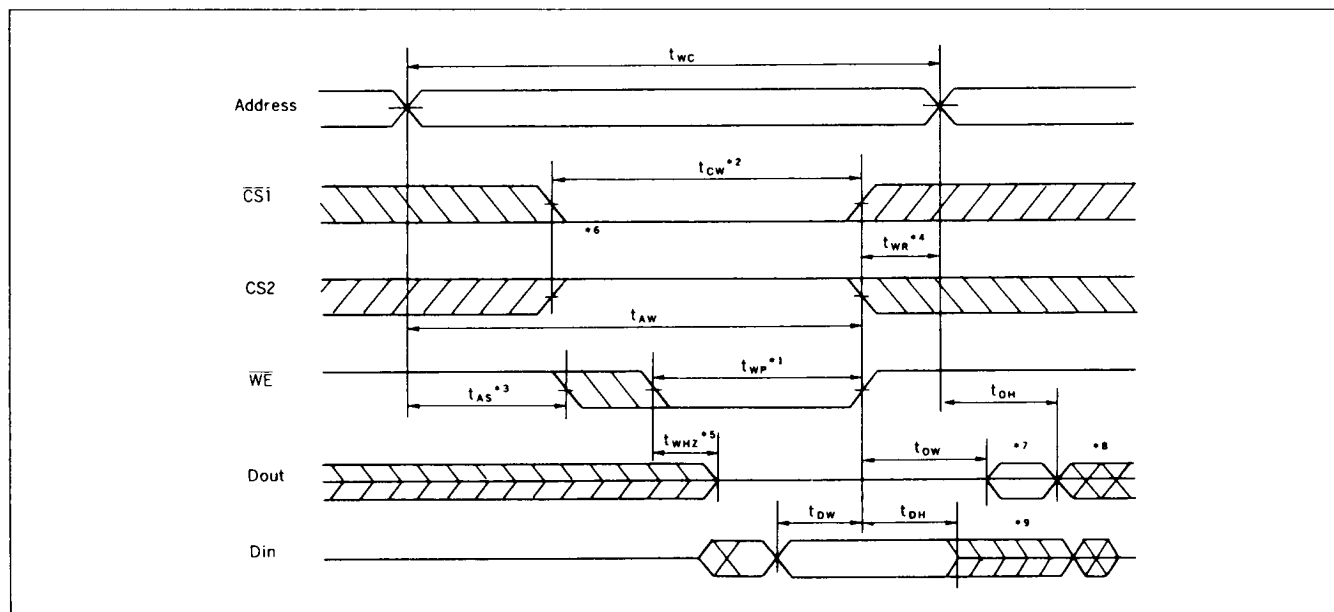
### Write Cycle

Item	Symbol	AKM628128-7		AKM628128-8		AKM628128-10		AKM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	70	—	85	—	100	—	120	—	ns	
Chip selection to end of write	$t_{CW}$	60	—	75	—	90	—	100	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	$t_{AW}$	60	—	75	—	90	—	100	—	ns	
Write pulse width	$t_{WP}$	55	—	65	—	75	—	85	—	ns	
Write recovery time	$t_{WR}$	5	—	5	—	5	—	10	—	ns	
		10	—	10	—	10	—	15	—	ns	*11
Write to output in high-Z	$t_{WHZ}$	0	25	0	30	0	35	0	40	ns	*10
Data to write time overlap	$t_{DW}$	30	—	35	—	40	—	45	—	ns	
Write hold from write time	$t_{DH}$	0	—	0	—	0	—	0	—	ns	
Output active from end of write	$t_{OW}$	5	—	5	—	5	—	5	—	ns	*10

Write Timing Waveform (1) ( $\overline{OE}$  Clock)



Write Timing Waveform (2) ( $\overline{OE}$  Low Fix)



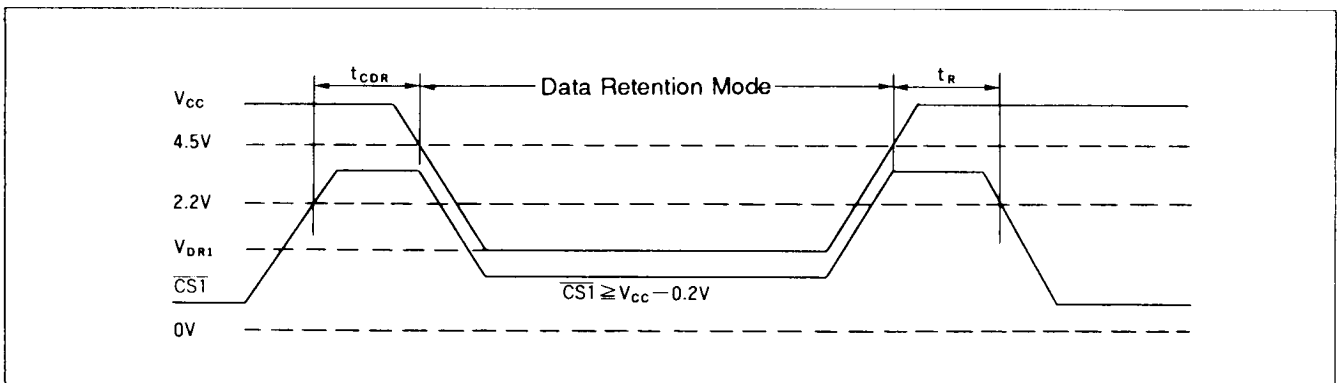
- Notes:
- \*1. A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2 and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low and  $\overline{WE}$  going high.  $t_{WR}$  is measured from the beginning of write to the end of write.
  - \*2.  $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or CS2 going high to the end of write.
  - \*3.  $t_{AS}$  is measured from the address valid to the beginning of write.
  - \*4.  $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going low to the end of write cycle.
  - \*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

- \*6. If  $\overline{CS1}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in high impedance state.
- \*7. Dout is the same phase of the latest written data in this write cycle.
- \*8. Dout is the read data of next address.
- \*9. If  $\overline{CS1}$  is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
- \*10. This parameter is sampled and not 100% tested.
- \*11. This value is measured from CS2 going low to the end of write cycle.

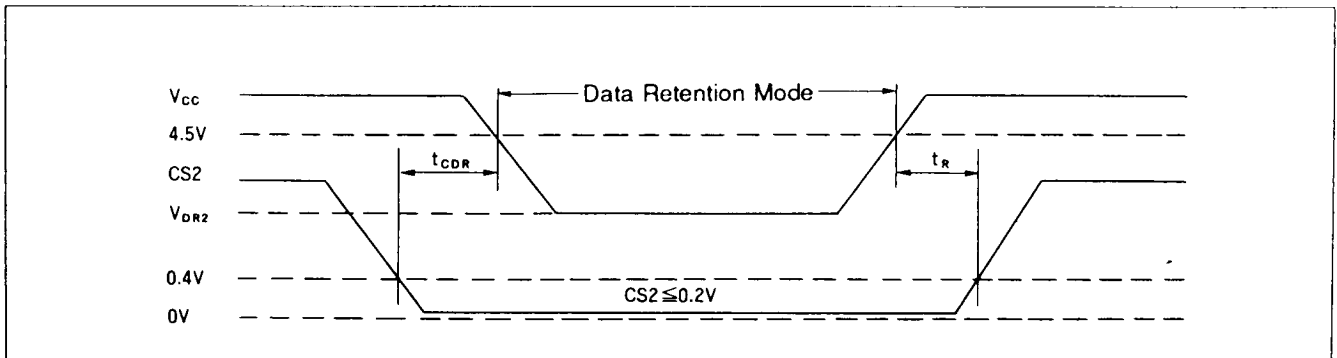
**Low Vcc Data Retention Characteristics ( Ta = 0 to +70°C )**  
 (This characteristics is guaranteed only for L-version.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions*2
Vcc for data retention	V <sub>DR</sub>	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2 V$ , $CS2 \geq V_{CC} - 0.2 V$ or $0 V \leq CS2 \leq 0.2 V$ $V_{in} \geq 0 V$
Data retention current	I <sub>CCDR</sub>	—	1	50*1	μA	$V_{CC} = 3.0 V, V_{in} \geq 0 V$ $\overline{CS1} \geq V_{CC} - 0.2 V$ , $CS2 \geq V_{CC} - 0.2 V$ or $0 V \leq CS2 \leq 0.2 V$
		—	1	30*2		
		—	1	15*3		
Chip deselect to data retention time	t <sub>CDR</sub>	0	—	—	ns	See Retention Waveform
Operation recovery time	t <sub>R</sub>	5	—	—	ms	

**Low Vcc Data Retention Timing Waveform (1) ( $\overline{CS1}$  Controlled)**



**Low Vcc Data Retention Timing Waveform (2) (CS2 Controlled)**



- Notes: \*1. 20 μA max at Ta=0 to 40°C, \*2. 6 μA max at Ta=0 to 40°C, \*3. 3 μA max at Ta=0 to 40°C.  
 \*4. CS2 controls address buffer,  $\overline{WE}$  buffer,  $\overline{CS1}$  buffer and  $\overline{OE}$  buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{CS1}$ , I/O) can be in the high impedance state. If  $\overline{CS1}$  controls data retention mode, CS2 must be  $CS2 \geq V_{CC} - 0.2 V$  or  $0 V \leq CS2 \leq 0.2 V$ . The other input levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.