Am2948/Am2949

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems; PNP inputs reduce input loading
- V_{CC} – 1.15V V_{OH} interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability; Low power – 8mA per bidirectional bit
- Am2948 has inverting transceivers; Am2949 has non-inverting transceivers — both have separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables
- Bus port stays in hi-impedance state during power up/down

GENERAL DESCRIPTION

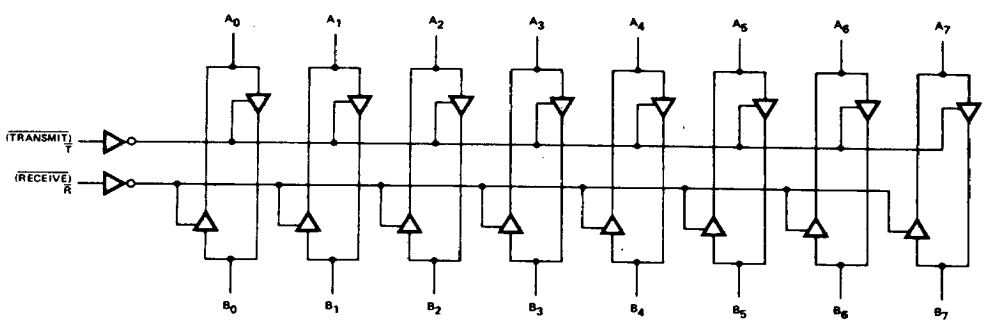
The Am2948 and Am2949 are 8-bit, 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables are provided for microprocessor system with separated read and write control bus lines.

The output high voltage (V_{OH}) is specified at V_{CC} – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

BLOCK DIAGRAM

Am2949



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Am2948 has inverting transceivers.

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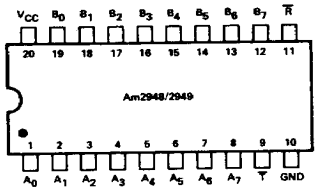
CONNECTION DIAGRAM
Top View

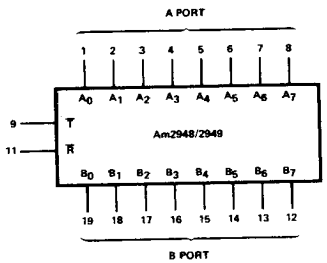
D-20-1



CD004770

Note: Pin 1 is marked for orientation
Am2948 is inverting from Ai to Bi

LOGIC SYMBOL



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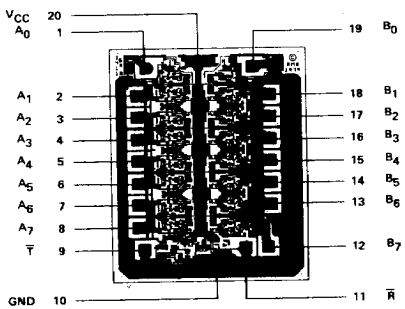
METALLIZATION AND PAD LAYOUT
Am2949



DIE SIZE .069" x .089"
Note: The Am2948 has inverting transceivers

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am2948/2949 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - P – 20-pin plastic DIP
  - X – Dice
- **Am2948/2949** — Device type
  - Bidirectional Bus Transceivers

Valid Combinations	
Am2948 Am2949	PC DC, DCB, DM, DMB XC

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A_0-A_7	I/O	A port inputs/outputs are receiver output drivers when $\overline{\text{Receive}}$ is LOW and $\overline{\text{Transmit}}$ is HIGH, and are transmit inputs when $\overline{\text{Receive}}$ is HIGH and $\overline{\text{Transmit}}$ is LOW.
	B_0-B_7	I/O	B port inputs/outputs are transmit output drivers when $\overline{\text{Transmit}}$ is LOW and $\overline{\text{Receive}}$ is HIGH, and are receiver inputs when $\overline{\text{Transmit}}$ is HIGH and $\overline{\text{Receive}}$ is LOW.
9,11	$\overline{\text{Transmit}}$, $\overline{\text{Receive}}$	I	These controls determine whether A port and B port drivers are in 3-state. With both $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ HIGH both ports are in 3-state. $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ both LOW activate both drivers and may cause oscillations. This is not an intended logic condition. With $\overline{\text{Transmit}}$ HIGH and $\overline{\text{Receive}}$ LOW A port is the output and B port is the input. With $\overline{\text{Transmit}}$ LOW and $\overline{\text{Receive}}$ HIGH B port is the output and A port is the input.

FUNCTION TABLE

Control Inputs		Resulting Conditions	
Transmit	**Receive**	**A Port**	**B Port**
H	L	Out	In
L	H	In	Out
H	H	3-State	3-State
L	L	Both Active*	

*This is not an intended logic condition and may cause oscillations.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage 7.0V
Input Voltage 5.5V
Output Voltage 5.5V
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ	Max	Units
A PORT (A_0-A_7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OH} = −0.4mA	V_{CC} − 1.15	V_{CC} − 0.7		Volts
			I_{OH} = −3.0mA	2.7	3.95		
V_{OL}	Logical "0" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OL} = 12mA		0.3	0.4	Volts
			COM'L I_{OL} = 24mA		0.35	0.50	
I_{OS}	Output Short Circuit Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX; Note 2		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 2.7V			0.1	80	µA
I_I	Input Current at Maximum Input Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 0.4V			−70	−200	µA
V_C	Input Clamp Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V			−200	µA
			V_O = 4.0V			80	
B PORT (B_0-B_7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC} − 1.15	V_{CC} − 0.8		Volts
			I_{OH} = −5.0mA	2.7	3.9		
			I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
			I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current	$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_O = 0V V_{CC} = MAX, Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 2.7V			0.1	80	µA
I_I	Input Current at Maximum Input Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 0.4V			−70	−200	µA
V_C	Input Clamp Voltage	$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V			−200	µA
			V_O = 4.0V			200	

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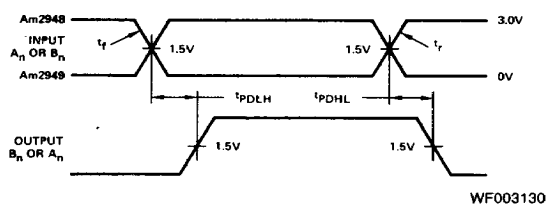
DC CHARACTERISTICS (Cont.)

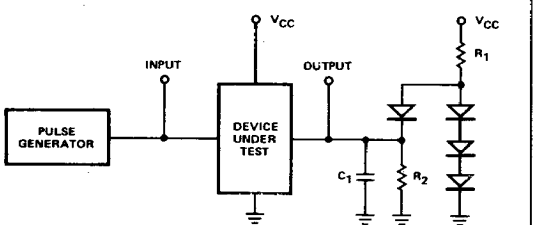
CONTROL INPUTS $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage		COM'L			0.8	Volts
			MIL			0.7	
I_{IH}	Logical "1" Input Current	V_I = 2.7V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX, V_I = V_{CC} MAX				1.0	mA
I_{IL}	Logical "0" Input Current	V_I = 0.4V	$\overline{R}$		−0.1	−0.25	mA
			$\overline{T}$		−0.25	−0.5	
V_C	Input Clamp Voltage	I_{IN} = −12mA			−0.8	−1.5	Volts
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	Am2948	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 2.0V, V_{CC} = MAX		70	100	mA
			$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2.0V, V_{CC} = MAX		100	150	
		Am2949	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 0.4V, V_{CC} = MAX		70	100	mA
			$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2.0V, V_{CC} = MAX		90	140	

SWITCHING TEST WAVEFORM



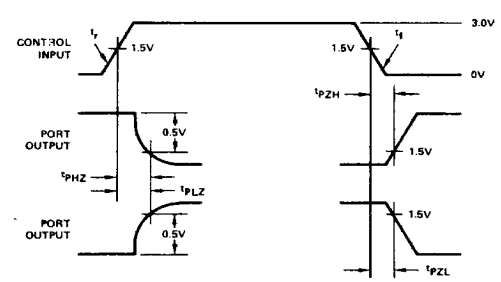
$t_r = t_f < 10ns$
10% to 90%

SWITCHING TEST CIRCUIT

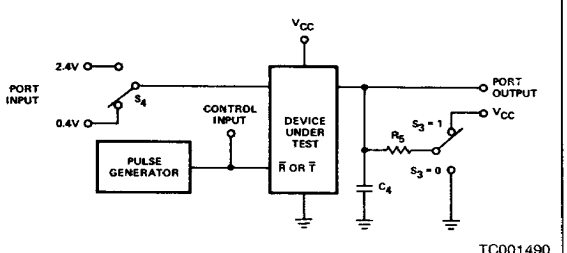


Note: C_1 includes test fixture capacitance.

Figure A. Propagation Delay from A Port to B Port or from B Port to A Port.



$t_r = t_f < 10ns$
10% to 90%



Note: C_4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

Figure B. Propagation Delay to/from Three-State from $\overline{R}$ to A Port and $\overline{T}$ to B Port.

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)
Am2948

Parameter	Description	Test Conditions	Typ	Max	Units
		A PORT DATA/MODE SPECIFICATIONS			
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	27	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 30pF	20	27	ns
		B PORT DATA/MODE SPECIFICATIONS			
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	8	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_1 = 45pF	18	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	25	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	16	25	ns

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SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Am2948

Parameter	Description	Test Conditions	COMMERCIAL Am2948 Max	MILITARY Am2948 Max	Units
		A PORT DATA/MODE SPECIFICATIONS			
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	19	16	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	23	20	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	35	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	35	30	ns
		B PORT DATA/MODE SPECIFICATIONS			
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	29	24	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	19	16	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	30	25	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	19	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	26	23	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	43	38	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	33	28	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	43	38	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	33	28	ns

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SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)
Am2949

Parameter	Description	Test Conditions	Typ	Max	Units
		A PORT DATA/MODE SPECIFICATIONS			
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	27	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 5k, C_4 = 30pF	20	27	ns
		B PORT DATA/MODE SPECIFICATIONS			
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_1 = 45pF	17	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	24	35	ns
		S_3 = 0, R_5 = 5k, C_1 = 45pF	17	25	ns

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SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Am2949

Parameter	Description	Test Conditions	COMMERCIAL Am2949 Max	MILITARY Am2949 Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	24	21	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	24	21	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	35	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	35	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	34	28	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	25	22	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	34	28	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	25	22	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	26	23	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 0.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	43	38	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	33	28	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	43	38	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	33	28	ns

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